Charge Loss Modeling for EPROMs with ONO Interpoly Dielectric

Martin R. Herrmann

Hartung-Gorre Verlag Konstanz
1994
Charge loss modeling for EPROMs with ONO interpoly dielectric / Martin R. Herrmann. - 1. Aufl. - Konstanz : Hartung-Gorre, 1994
(Series in microelectronics ; Vol. 42)
Zugl.: Zürich, Eidgenössische Techn. Hochsch., Diss., 1994
ISBN 3-89191-836-4
NE: GT

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Erste Auflage 1994
HARTUNG-GORRE VERLAG KONSTANZ
ISSN 0936 - 5362
ISBN 3 - 89191 - 836 - 4
Acknowledgments

First of all, I would like to thank Prof. Alessandro Birolini who as project head and supervisor of this work provided outstanding guidance and technical support. I am also grateful to Prof. Wolfgang Fichtner for accepting to co-examine this thesis, for valuable technical discussions and for introducing me to his research assistants.

My thanks go also to Mauro Ciappa for important suggestions during the preparation of this work and for the careful review of the manuscript. I am thankful to Dr. Andreas Schenk whose theoretical understanding of semiconductor physics were important for modeling the charge loss properties. A particular thank you goes to Joachim Reiner for his advice in practical and theoretical questions. I am also grateful to Markus Schönbucher for his help in special computer programming steps.

I wish to thank the SGS-Thomson R&D Technology Group for the access to test modes of the devices and process specific informations, as well as for technical discussions and for providing a large number of devices.

Finally, I would like to thank Dr. Neal Mielke of Intel Corporation in Santa Clara, Prof. Bruno Riccò of DEIS University of Bologna, and Dr. Michel Dutoit of EPFL Lausanne for their critical remarks which improved the work, as well as Harriet Reissenberger for the grammar-proofing of the manuscript.
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Abstract

The investigations presented in this work identify the origin of intrinsic long term charge loss in EPROMs with ONO interpoly dielectric and model the charge transport through the ONO dielectric as a function of electric field and temperature.

The measured drain-source current at different times during bakes at three temperatures is transformed into a current-voltage characteristic of the ONO interpoly dielectric. The floating gate charge and voltage is calculated using a simple floating gate transistor model. The derivative of this charge with respect to the time is the current leaking through the ONO. The electric field is determined by the corresponding floating gate voltage.

From a program-bake-erase-bake cycle it was possible to find out that long term charge loss is not due to mobile ions. A charge loss experiment with two lots of EPROMs, one with ONO, the other with oxide for the interpoly dielectric, identify that charge transport is mainly governed by the conductivity of the oxide layers in the ONO structure. Since hole injection from the control gate into the nitride is blocked by the 70 Å thick top oxide, it can be concluded that for the examined devices charge loss is mainly due to leakage of electrons.

However, the leakage current observed experimentally is too large to be explained by pure electrode limited charge transport (Richardson emission and direct tunneling). Nor can it be explained by bulk limited currents: hopping
conduction and space charge limited current do not have an exponential field dependence, Poole-Frenkel conduction applied to thin dielectrics cannot explain the measured temperature dependence, and field ionization of trapped electrons is not temperature dependent. It was also verified that field gain on asperities and along edges cannot increase the charge loss current to the observed values.

A trap-assisted tunneling mechanism has thus been proposed in this work, where electrons tunnel to oxide traps and are then emitted. The coupling of the trap level to oxide phonons results in virtual energy levels in the oxide which allows for more effective tunneling paths. A quasi-continuous energetic distribution of trap energies is assumed. According to this model, mainly the traps in a small energy interval are active in the steady-state trapping and detrapping process at high temperatures and low electric fields. As a consequence of the electron-phonon coupling the emission occurs close to the oxide conduction band edge at high temperatures. Without the electron-phonon coupling, the mechanism turns into the simple two-step tunneling which cannot explain the strong temperature dependence of the measured charge loss data.
Zusammenfassung

Die Resultate der vorliegenden Arbeit geben eine Erklärung der Ursache für Langzeit-Ladungsverlust bei EPROMs mit ONO Interpoly-Dielektrikum und führen zu einem Modell, dass den Ladungstransport durch ONO Interpoly-Dielektrikum in Abhängigkeit der Temperatur und des elektrischen Feldes beschreibt.


Zusammenfassung

untersuchten Bauteilen im wesentlichen durch Elektronenleitfähigkeit verursacht wird.

Der experimentell ermittelte Leckstrom erwies sich jedoch als zu gross, um mit elektrodenbegrenzten Ladungstransport-Mechanismen (Richardson-Emission und direktes Tunneln) erklärt zu werden. Auch die volumenbegrenzten Ströme können den Leckstrom nicht erklären (Hopping-Leitfähigkeit und raumladungs begrenzter Strom haben nicht die erforderliche exponentielle Feldabhängigkeit, der Poole-Frenkel-Mechanismus angewendet für dunne Dielektrikas kann die gemessene temperaturabhängigkeit nicht erklären und Feldionisation in Fehlstellen eingefangener Elektronen scheidet aus wegen der fehlenden Temperaturabhängigkeit). Felderhöhung an rauher Isolationsoberfläche und entlang von Kanten kann den Ladungsverlust ebenfalls nicht erklären.

1

Introduction

EPROMs store the logical information in form of electrons on the floating gate of the memory cells. During programming, hot electrons are injected from the channel to the floating gate. These electrons can be removed by U.V. light. The reliability of the device is primarily determined by the quality of the dielectrics surrounding the floating gate, besides conventional failure mechanisms of integrated circuits. Under normal operating conditions, data retention time of more than 10 years is usually specified by the manufacturer and expected by the user.

1.1 Purpose

As a consequence of scaling down of nonvolatile memories, the thicknesses of the dielectrics surrounding the floating gate must be decreased. The type of charge carrier leading to charge loss and its transport mechanism through the dielectrics, as well as the influence of defects in the dielectrics must be understood to predict data retention time. There is no quantitative model based only on physical parameters published up to now which describes the charge loss in function of the dielectric properties.

The purpose of this work is to develop an electric field and temperature dependent model for the charge transport through the interpoly dielectric, which is the dielectric between the floating gate and the control gate of an EPROM-cell.
The fact that the data retention time of nonvolatile memories is greater than 10 years under normal operating conditions, requires charge transport accelerating procedures which can be either based on high electric field stress and/or high temperature stress. In this work high temperature stress has been chosen. The electric field is in the same range as under normal operating conditions.

Chapter 1 gives a review of the literature on charge loss and charge transport models. Chapter 2 describes then the structure of the examined floating gate cell and derives the dependence of the floating gate charge and voltage from the drain-source current. In Chapter 3, test methods are described, followed by the experimental results. In Chapter 4, these data are applied to the traditional charge transport mechanisms. In Chapter 5, the multiphonon-assisted tunneling mechanism will be introduced and compared with test results. Conclusions are drawn in Chapter 6.

1.2 Fundamentals

The EPROM belongs together with the E²PROM and Flash E²PROM to the family of nonvolatile memories. They differ mainly in their program and erase process. EPROMs are programmed by hot electron injection from the channel to the floating gate. These electrons can be removed by U.V. light. The E²PROM cell is programmed and erased by Fowler-Nordheim injection of electrons through the tunnel oxide located at the drain side of the floating gate transistor. A Flash cell is programmed by hot electron injection like the EPROM cell while the erasing is done by Fowler-Nordheim mechanism comparable to the E²PROM cell, except that it occurs at the source side of the floating gate transistor.

Data retention is the ability of a memory cell to keep its logical information in the time. The floating gate charge determines the threshold voltage of the cell transistor and is used to indicate the stored logical information by comparison with a reference cell. Any change of the charge distribution between substrate and control gate leads to a threshold voltage shift. Data loss can occur due to charge loss or charge gain of the charged or uncharged floating gate, respectively. Charge loss leads to a threshold voltage decrease while charge
gain results in an increasing threshold voltage.

A description of charge transport through a dielectric is generally based on constant voltages on the left- and right-hand side of the dielectric, while a charge loss description also includes the change of the floating gate voltage in function of time.

Charge loss at high temperatures have at least two phases. One initial charge loss phase which saturates after about 100 hours at temperatures higher than 250 °C and the long term charge loss phase in which the threshold voltage decreases to a grade where the cell fails. This work considers long term charge loss measurements of up to 60 % charge loss from the programmed quantity on the floating gate.

The floating gate is surrounded by the following dielectrics: the gate oxide between substrate and floating gate, the interpoly dielectric between floating gate and control gate, and the field oxide or the CVD oxide between floating gates of adjacent cells. The interpoly dielectric is either an oxide film, or in newer technologies, an oxide/nitride/oxide (ONO) sandwich.

1.3 Literature Review

Charge Loss Models

Some long term charge loss models for nonvolatile memories have been discussed in the literature:

1. For SAMOS structures and SEEPROM cells the thermionic electron emission model has been proposed [50, 51]. The temperature behavior is modeled by the Arrhenius law where the activation energy is interpreted as the energy barrier between the conduction band edges in Si and SiO₂. This parameter is much lower than if measured by optical or Fowler-Nordheim experiments. In the optical experiment the irradiation energy at which the electrons surmount the energy barrier between the conduction
band edges in Si and SiO₂ is detected. The Fowler-Nordheim experiment uses this energy barrier as a fit parameter which is very sensitive to the slope of the I-V characteristic of MOS-capacitors. With both experiments an energy barrier of about 3.1 eV was estimated.

2. The thermionic electron emission model has been modified by introducing an electric field dependent barrier lowering due to the image force effect and a temperature dependent charge accumulation around the floating gate [31]. At low temperatures a larger charge accumulation occurs compared to high temperatures. This reduces the electric field on the place of electron injection to the oxide and thus prevents a charge loss from the floating gate. The model gives a good fit over a large temperature range but still uses fit parameters which do not agree with other measurement methods.

3. For EPROMs with ONO interpoly dielectric it has been found that trapped electrons at the nitride-oxide interface can directly tunnel through a thin (30 Å) top oxide [54].

4. In a later paper [55], the same authors as in [54] modeled the long term charge loss above 300 °C with the Poole-Frenkel mechanism. From the temperature slope a barrier height for trapped electrons on the nitride-top oxide interface has been calculated. The electric field dependence is due to barrier lowering.

5. An analytical charge loss model for SONOS devices was presented in Ref. [56] and [28]. The model considers the following mechanisms: (1) electron back-tunneling from the nitride traps to the Si conduction band, (2) electron back-tunneling from the nitride traps to the Si/SiO₂ interface traps, and (3) hole injection from the Si valence band to the nitride traps. An amphoteric trap charge distribution is used in this model. Step (1) determines the initial charge loss phase, while steps (2) and (3) determine the long term charge loss phase.

6. For E²PROMs with a thin tunnel oxide, high field experiments at room temperature indicate that Fowler-Nordheim injection is responsible for the
1.3 Literature Review

charge loss. At low field, i.e. normal operating conditions, the mechanism must be replaced by direct tunneling [30]. Because of its strong dependence on insulator thickness, this mechanism cannot be applied to the thicker interpoly dielectric or gate oxide in EPROMs.

**Charge Transport Mechanisms**

Many results from experiments made on test capacitors have been published to explain charge transport in oxide (SiO₂), nitride (Si₃N₄), NO (Si₃N₄/SiO₂) and ONO (SiO₂/Si₃N₄/SiO₂).

1. In oxide films, Fowler-Nordheim injection is dominant at high field strengths (higher than 5 MV/cm for a dielectric thickness of about 100 Å). This mechanism has a weak temperature dependence at ordinary temperatures [18]. For high temperatures and low fields, Richardson injection becomes dominant. This mechanism is strongly temperature but only weakly field-dependent [63]. Direct tunneling becomes responsible for charge transport in thin oxides at low fields along with a weak temperature dependence [26]. The charge transport is due to electron conduction and is limited by injection from the electrode (electrode-limited conduction) if the influence from traps can be neglected.

2. In nitride films, hole conduction is larger than electron conduction [77, 78, 6, 34]. The charge transport is limited by the bulk properties of the dielectric (bulk-limited conduction). According to Ref. [69], the current density is the sum of three contributions: at high fields and high temperatures the Poole-Frenkel effect dominates; at high fields and low temperatures the current is due to field ionization of trapped charge; and at low fields and moderate temperatures hopping from one trap to the other is dominant. The current density in silicon-nitride films is larger than in oxides at the same field.

3. In nitride-oxide stacked films, charge transport is due to the above described mechanism for each film, respectively. Since the current-field characteristics are different for the two materials, the fields will adjust
themselves by charge accumulation in the nitride close to the interface until current continuity is established [20, 35, 66 – 68, 82, 3]. The polarity of the trapped charge can be identified by measuring the flatband voltage shift [38, 49].

4. In oxide-nitride-oxide stacked films, an anode-side oxide (positive electrode voltage with respect to the cathode-side) thicker than 30 Å can block hole injection into the nitride. The oxide on the cathode-side (negative electrode voltage with respect to the anode-side) determines the electron injection. Holes injected into the nitride are accumulated on the oxide-nitride interface on the cathode-side, while electrons accumulate on the nitride-oxide interface on the anode-side. Some of the charge can recombine in the nitride. The nitride thickness influences the amount of trapped charge [75, 76, 43 – 46].

5. Some publications exist on trap-assisted tunneling where electrons tunnel to traps in the insulator and are then emitted. For thin insulators the probability is small to find two defects along one tunneling path. Svensson et al. [67] applied this mechanism to a MNOS structure. In the first step electrons tunnel by "modified Fowler-Nordheim injection" [66] from the conduction band of the electrode through a very thin oxide layer into nitride traps. The second step, where the electrons are emitted to the nitride conduction band, was neglected because of the smaller tunnel probability compared to that of the first step. The temperature dependence originates from the occupation probability in the conduction band of the electrode. Fleischer et al. [11, 17] presented a closed formula for the two-step tunneling mechanism through a single insulator layer. The model is valid for intermediate electric fields and yields no temperature dependence. Yasuda et al. [81] used an asymmetric spatial trap distribution for the two-step tunneling mechanism to explain the voltage polarity dependence of stress-induced leakage current through MOS capacitors.

6. Other authors involve Poole-Frenkel conduction in combination with direct tunneling in a non-equilibrium condition in MNOS structures [79] or field emission from the cathode in combination with space-charge build-up in the body of a single layer dielectric [52]. Ref. [22] presents a
model where electrons which have tunneled by Fowler-Nordheim mechanism through the potential barrier, gain energy from the electric field in the oxide and will lose energy by various scattering mechanisms. The hot electrons arriving at the anode will lose their energy by emitting surface plasmons. The emitted surface plasmons will decay via the excitation of electron/hole pairs and by the generation of both hot holes and electrons. The hot holes may be emitted over or tunnel through the potential barrier. For more mechanisms see also [37, 39, 41, 57].

**Synthesis of Data Loss Mechanisms**

The following data loss mechanisms have been previously identified:

1. Defects in the interpoly dielectric or gate oxide leading to electronic leakage resulting in charge loss or charge gain on the floating gate. The affected cells are generally randomly located in the memory array [40, 62].

2. Ionic contamination can compensate the stored charge. Positive charged ions move due to the electric field resulting from the negative floating gate charge. If the cells are erased, the ions can move due to their concentration gradient and cause charge gain. The failing cells form regions which generally increase in magnitude as function of the bake time [40, 14, 58].

3. During U.V. erasing, some of the electrons which were stored on the floating gate can be trapped in the interpoly dielectric or in the gate oxide. After the reprogramming of the cells and a second bake the release of electrons, previously trapped during U.V. erasing, results in a threshold voltage decrease just like charge loss due to electrons stored on the floating gate. The charge loss would stop when the traps were emptied. All memory cells are affected by this mechanism [40].

4. For ONO interpoly dielectrics three distinct phases exist in the charge loss characteristic during bake time. An initial fast threshold voltage shift of less than 10 minutes at 250 °C can be explained by carriers movement in
the nitride or a nitride polarization effect. The threshold voltage shift of the second phase is caused by the movement of trapped electrons which are mostly injected into the nitride during memory programming. This phase saturates after about 100 h at 250 °C. The third phase is the non-saturating long term threshold voltage shift. It is determined by electrons leaking through the bottom and top oxide. The first and second phases are a strong function of nitride thickness while the third phase is dependent on the oxide thicknesses of the ONO [80, 53].
2

Memory Cell Description

Two lots have been measured which differ only in the type of interpoly dielectric: one with a 205 Å thick oxide layer and the other with an ONO sandwich of 70 Å top oxide, 70 Å nitride and 100 Å bottom oxide. The single oxide dielectric has the equivalent oxide thickness of the ONO dielectric. The cell is described by using the one-dimensional long-channel transistor model with capacitive coupling from the control gate and drain to the floating gate. Calculated drain-source currents versus control gate-to-source voltage are compared with measured values of one cell.

2.1 Structure and Technology

The charge loss measurements have been made on commercial 4 Megabit EPROMs. The cell is a standard MOS transistor except for the addition of a floating gate positioned between the control gate and channel. All cells along one row have their control gates connected via a word-line. All cells in the same column have their drains connected and are fed to the sense amplifier via a bit-line. All cell sources are held at ground potential. Due to particular test modes it was possible to control the gate and drain voltage of each floating gate transistor through the word-line and bit-line decoder. The device was fabricated in 0.8 µm technology. The substrate is p-doped while floating gate and control gate are n-doped poly silicon.
Figure 2.1: SEM photo of an EPROM cell after metal, CVD oxide and field oxide etching. G, D and F denotes control gate, drain and floating gate, respectively.

Figure 2.2: Schematic description of the EPROM cell: view along the word-line (left), view along bit-line (right).

Figure 2.1 shows a SEM cross-section through the cell. The metal, CVD oxide and the field oxide have been removed. In the foreground the drain contact D can be seen while the source diffusion is hidden by the word-line. The word-line forms the control gate G of the floating gate transistor. The
floating gate \( F \) is below the control gate. It has a larger overlap with the control gate than with the substrate. Figure 2.2 shows schematically the cell structure. The right-hand side shows the same view of the cell as the SEM photo in Figure 2.1. The gate oxide is the dielectric between the floating gate and the substrate. The interpoly dielectric, which can be either an oxide dielectric or an ONO dielectric, is located between the floating gate and the control gate.

Two lots have been measured, one with oxide, and the other one with ONO as interpoly dielectric. Recent technologies use ONO dielectrics. The advantages of the ONO are the larger permittivity of nitride compared to that of oxide, the smaller defect density of the stacked dielectric compared to that of a single oxide layer, and a higher breakdown voltage. In both lots, the oxidation was performed at 1000 °C. The nitride in the ONO-devices was grown at 800 °C. The first poly was doped by implant. The nominal oxide thicknesses are 205 Å for the single oxide dielectric and 70 Å, 70 Å and 100 Å from top to bottom for the ONO sandwich (see Figure 2.3).

![Figure 2.3: Structure of the interpoly dielectric: oxide (left), ONO (right).](image)

The top oxide prevents hole injection from the control gate into the nitride. The single oxide dielectric has the equivalent oxide thickness of the ONO dielectric. It is calculated by

\[
d_{G,o} = d_{b,o} + \frac{\varepsilon_o}{\varepsilon_n} d_n + d_{i,o},
\]

(2.1)
where $d_{G,o}$ is the equivalent oxide thickness, $d_{b,o}$, $d_n$ and $d_{t,o}$ are the thicknesses of bottom oxide, nitride and top oxide, respectively, $\varepsilon_o$ and $\varepsilon_n$ are the permittivities of oxide and nitride. This implies that the oxide field is the same for both lots at a given voltage drop between control gate and floating gate. The ratio $\varepsilon_o / \varepsilon_n$ is about 1/2. Table 2.1 summarizes the cell parameters. The two lots differ only in the type of interpoly dielectric. The total capacitance is the sum of the capacitances between floating gate and control gate, floating gate and drain, and floating gate and substrate (see section 2.2).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate oxide length</td>
<td>$l_F$</td>
<td>0.8 µm</td>
</tr>
<tr>
<td>Gate oxide width</td>
<td>$w_F$</td>
<td>1 µm</td>
</tr>
<tr>
<td>Gate oxide thickness</td>
<td>$d_F$</td>
<td>200 Å</td>
</tr>
<tr>
<td>Interpoly dielectric length</td>
<td>$l_G$</td>
<td>0.8 µm</td>
</tr>
<tr>
<td>Interpoly dielectric width</td>
<td>$w_G$</td>
<td>2.4 µm</td>
</tr>
<tr>
<td>Interpoly equivalent oxide thickness</td>
<td>$d_{G,o}$</td>
<td>205 Å</td>
</tr>
<tr>
<td>Total capacitance</td>
<td>$C_T$</td>
<td>4.6 fF</td>
</tr>
</tbody>
</table>

**Table 2.1:** Cell parameters of oxide and ONO devices.

For further investigations the following coordinate system is introduced: the x-axis from control gate to substrate, the y-axis from source to drain and the z-axis perpendicular to the previous two.

### 2.2 Floating Gate Transistor Model

The floating gate charge can be only indirect determined by measuring the drain-source current at fixed control gate-to-source voltage and drain-to-source voltage. In the measurement condition the control gate-to-source voltage was set to 8 V and the drain-to-source voltage to 1 V. During the bake no voltage is applied to the control gate and the drain. Source voltage is always on ground potential.
Measurement Condition

The floating gate transistor can be regarded as a normal field effect transistor with the floating gate voltage on the gate [74, 33]. The drain-source current can be calculated with eqn. (2.2) and (2.3) valid for small drain-to-source voltages.

\[
I_D = \frac{\beta}{2b} (U_{FS} - U_t)^2 \quad \text{for} \quad U_t < U_{FS} \leq U_t + bU_{DS}, \quad (2.2)
\]

\[
I_D = \beta \left[ (U_{FS} - U_t) U_{DS} - \frac{b}{2} U_{DS}^2 \right] \quad \text{for} \quad U_t + bU_{DS} < U_{FS}. \quad (2.3)
\]

$I_D$ is the drain-source current, $U_{FS}$ is the floating gate voltage, $U_{DS}$ is the drain-to-source voltage and $U_t$ is the threshold voltage. $U_t$, $\beta$ and $b$ are functions of electron mobility and doping concentration in the substrate, channel width and channel length, bulk potentials in substrate and floating gate, permittivity of oxide, and oxide thickness [70].

![Diagram of Floating Gate Transistor](image)

**Figure 2.4:** Floating gate transistor in measurement condition.
Figure 2.4 illustrates the model used in calculating the floating gate charge $Q_F$. The control gate and floating gate are highly doped and can thus be treated like a metal. The channel is in strong inversion. In Figure 2.5 $\psi_{b,S}$, $\psi_{b,F}$, and $\psi_{b,G}$ denotes the bulk potentials in the substrate, floating gate and control gate, respectively. The Fermi level $E_{f,S}$ in the substrate far away from the gate oxide is set to zero. $E_c$, $E_v$, and $E_i$ denotes the bottom of the conduction band, the top of the valence band, and the intrinsic Fermi level, respectively. By using the Gauss law the floating gate charge is given by

$$Q_F = C_G(U_{FS} - U_{GS}) + C_D(U_{FS} - U_{DS}) + \frac{C_F}{l_F} \int_0^{l_F} [U_{FS} - U_{CS}(y)] dy,$$

where $U_{GS}$ is the control gate-to-source voltage, $U_{CS}$ is the voltage along the channel, $l_F$ is the channel length, and $C_G$, $C_D$, and $C_F$ are the capacities indicated in Figure 2.4. If the drain-to-source voltage is small and the transistor is not in saturation, the voltage along the channel is approximately linear, increasing from source to drain: $U_{CS} = (U_{DS}/l_F)y$. With this

Figure 2.5: Energy band diagram of the floating gate transistor in measurement condition on a position $y$ between source and drain.
approximation and eqn. (2.4) the floating gate charge becomes

\[ Q_F = C_G (U_{FS} - U_{GS}) + C_D (U_{FS} - U_{DS}) + C_F \left( U_{FS} - \frac{1}{2} U_{DS} \right). \]  

(2.5)

From eqn. (2.5) the floating gate voltage results

\[ U_{FS} = \frac{Q_F}{C_T} + \alpha_G U_{GS} + \alpha_D U_{DS} + \frac{\alpha_F}{2} U_{DS}, \]  

(2.6)

with

\[ \alpha_G = \frac{C_G}{C_T}, \quad \alpha_D = \frac{C_D}{C_T}, \quad \alpha_F = \frac{C_F}{C_T}, \quad C_T = C_G + C_D + C_F, \]  

(2.7)

while \( U_{DS} = U_{DS0} - R_D I_D \). \( R_D \) is the resistor from outside to the drain contact and \( U_{DS0} \) is the externally applied drain-to-source voltage.

**Figure 2.6:** Drain-source current versus control gate-to-source voltage at 20 °C with U.V. erase time as parameter. Measurements (dots) and model (solid lines).
Figure 2.6 shows the drain-source current versus control gate-to-source voltage of one cell with 1 V drain-to-source voltage in different erase states. The dots represent the measurements while the solid lines were calculated using eqn. (2.6) in (2.2) and (2.3). The device was erased with U.V. light. At different times the drain-source current versus control gate-to-source voltage was measured. The cell is completely erased after about 10 minutes. The floating gate transistor parameters in Table 2.2 are valid for both device lots.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_T$</td>
<td>4.6 fF</td>
</tr>
<tr>
<td>$\alpha_G / \alpha_D / \alpha_F$</td>
<td>0.65 / 0.07 / 0.28</td>
</tr>
<tr>
<td>$\beta$</td>
<td>$7 \cdot 10^{-5}$ A V$^{-2}$</td>
</tr>
<tr>
<td>$b$</td>
<td>1.1</td>
</tr>
<tr>
<td>$U_i$</td>
<td>1.2 V</td>
</tr>
<tr>
<td>$R_D$</td>
<td>600 $\Omega$</td>
</tr>
</tbody>
</table>

Table 2.2: Floating gate transistor parameters of oxide and ONO devices.

Bake Condition

During the bake no voltage is applied to the control gate and drain, but there is still an electric field across the isolation due to the floating gate charge. This situation is modeled with the equivalent capacitive circuit shown in Figure 2.7. Figure 2.8 shows the energy band diagram in bake condition.

![Figure 2.7: Floating gate transistor in bake condition.](image)
2.2 Floating Gate Transistor Model

Since the substrate and floating gate are differently doped, the voltage drop across the gate oxide is reduced compared to a MIM structure. The difference is $\psi_{b,s} - \psi_{b,F} = -1V$, while $\psi_{b,s} < 0$, and $\psi_{b,F} > 0$. The substrate is in accumulation, thus the floating gate charge is given by

$$Q_F = C_G (U_{FS} - U_{GS}) + C_D (U_{FS} - U_{DS}) + C_F (U_{FS} + \psi_{b,F} - \psi_{b,S}). \quad (2.8)$$

From eqn. (2.8) the floating gate voltage results in

$$U_{FS} = \frac{Q_F}{C_T} + \alpha_F (\psi_{b,s} - \psi_{b,F}). \quad (2.9)$$

For the device with oxide interpoly dielectric the electric field $F_F$ and $F_G$ in the gate oxide and interpoly oxide are given by

$$F_F = \frac{U_{FS} + \psi_{b,F} - \psi_{b,S}}{d_F}, \quad (2.10)$$
and

\[ F_G = \frac{U_{FS}}{d_G}. \]  \hspace{1cm} (2.11)

For the device with ONO interpoly dielectric the electric field in the top oxide is the same as in the bottom oxide: \( F_{G,o} = F_{G,i} = F_{G,b} \). It is calculated by replacing the interpoly thickness \( d_a \) in eqn. (2.11) with the equivalent oxide thickness \( d_{G,o} \) of the ONO specified in eqn. (2.1). The nitride electric field \( F_{G,n} \) is smaller than the oxide electric field \( F_{G,o} \) due to the larger permittivity: \( F_{G,n} = F_{G,o} \epsilon_o / \epsilon_n \). For further calculations only the absolute value of the electric field is used.
Experimental Investigations

The floating gate charge can either be determined by measuring the drain-source current at specified control gate and drain voltage or by a search algorithm for the margin voltage of the floating gate transistor. The margin voltage is related to the threshold voltage of the floating gate transistor. The relationship is defined by the sensing method. Long term data loss can be due to defects in the dielectrics surrounding the floating gate, mobile ions, or electronic leakage. The experiments described in this chapter lead to the following conclusions: 1. Charge loss due to mobile ions can be excluded for the examined devices. 2. Long term charge loss is limited by the oxide conductivity.

3.1 Experimental Methods

Measuring the Drain-Source Current

The drain-source current is a function of the floating gate charge. An increasing drain-source current indicates a decrease of the negative floating gate charge, if the other variables are constant. All drain-source current measurements presented in this chapter were performed at 8 V control gate-to-source voltage and 1 V drain-to-source voltage. The floating gate charge has been calculated using the transistor model described in Section 2.2.
The measurements have been performed with a Sentry S50 VLSI-tester. First, the device was powered up with 5 V and set into the test mode using the chip enable and output enable pins. After this, the control gate-to-source voltage was defined by the power supply voltage and the drain-to-source voltage was applied on one of the output pins. The floating gate transistor was selected by the applied cell address and by the connected bit of the output pins. The drain-sources current was measured on the appropriate output pin, using a PMU (Precise Measurement Unit). After each address change a wait time of 5 µs was necessary before the next measurement to avoid disturbance from switching phenomenas. The method is a quick way to measure many transistors, but the accuracy is limited by the complicated current pass through the peripheral circuitry.

Figure 3.1 shows three intermediate measurements on one device during the bake experiment as described in Section 3.3. 2048 cells have been measured along 4 word-lines. After each 512 addresses the next word-line was selected.

![Figure 3.1: Drain-source current of 2048 cells at three intermediate measurements on one device during the bake experiment (oxide device as in Fig. 2.3 left).](image-url)
Since the 2048 cells have different geometrical positions in the memory matrix, the pass resistor between drain and output pin varies from one cell to the other. In Figure 3.1 the influence on the pass resistor can clearly be seen at larger drain-source currents.

### Measuring the Margin Voltage

The margin voltage is defined as the maximum cell threshold voltage shift which could occur before causing a read error within the device's specified power supply tolerance. It can be used to detect poor programming or erasure. The margin voltage is related to the threshold voltage of the floating gate transistor. The relationship is defined by the sensing method. The idea is to vary the control gate-to-source voltage until the drain-source current of the matrix cell passes over the drain-source current of a reference cell (see Figure 3.2). The matrix cells store the logical information. All matrix cells along one word-line have together one reference cell. The programming and

![Figure 3.2: Sensing method using the load ratio approach (characteristic of a programmed, erased and reference cell).](image)
erasing have no influence on the reference cell. A matrix cell with a drain-
source current below the reference current will be sensed as a logical zero
while a matrix cell with higher drain-source current will be sensed as a logical
one. The control gate-to-source voltage $U_{gs}$ is defined by the power supply
voltage $V_{cc}$ since the decoder output of the selected word-line is nearly
equal to $V_{cc}$. The pass over the reference current is detected by a read
function test. The difference between the measured $V_{cc}$ maximum value and
the $V_{cc}$ maximum specified is the device program margin.

There are three sensing methods: 1. the reference current stays constant while
$V_{cc}$ is varied, 2. the reference current increases less than the drain-source
current of the matrix cell while $V_{cc}$ is varied (load ratio approach), 3. the
reference current has the same shape as an erased matrix cell characteristic with
a constant negative current offset (offset current approach). The above
technique can be used to characterize the exact margin value only if the control
gate-to-source voltage varies with $V_{cc}$ while all other device variables,
especially the reference current, stay constant. If this is not the case, as for the
load ratio approach presented in Figure 3.2, qualitative information can still be
drawn from this test. The margin voltage test fails completely in the case of the
offset current approach [21].

Several single bit charge loss were observed on the investigated devices using
the margin voltage method. The power supply voltage was increased from
4 V to 12 V using step size of 100 mV. After each step a read function test was
performed on the entire device. The number of failed cells where plotted in a
histogram. The input voltage levels where set on $V_{IL} = 0$ V and $V_{IH} = 3$ V.
The timing was twice as specified to ensure that the peripheral circuitry does
not cause erroneous outputs. If only the worst programmed cell has to be
detected, a binary search algorithm applied to $V_{cc}$ can drastically reduce the
test time.

### 3.2 Test for Mobile Ions

Mobile ions can compensate stored charges. This can be observed with a
program-bake-erase-bake cycle [40, 14, 58]. The ions are driven to the
3.2 Test for Mobile Ions

floating gate by the electric field from the stored negative charge during the first bake. Electric field and mobile ions concentration gradient act concurrently upon the ions. By erasing the cell after the first bake, an excess of electrons which balance the attracted ionic charge remains on the floating gate. Since the electric field is no longer present, the concentration gradient causes the ions to leave the cell by diffusion during the second bake. This appears as charge gain because part of the electrons have not been removed from the floating gate during the erasing operation. Increasing temperature accelerates the process due to emission of mobile ions from traps. It has been reported that Na$^+$ ions can act as mobile ions leading to charge loss [58].

Figure 3.3 shows this program-bake-erase-bake cycle for both lots described in Section 2.1. The increasing drain-source current during the first bake indicates a decreasing threshold voltage. Since no decrease of the drain-source current occurs during the second bake, charge loss due to mobile ions can be excluded for these devices. Each dot in Figure 3.3 represents the average value of 2000 cells of one device. Oxide and ONO devices have different initial

![Figure 3.3](image)

**Figure 3.3:** Drain-source current versus bake time at 350 °C for oxide and ONO devices, mean values over 2000 cells.
drain-source current in the second bake phase of the program-bake-erase-bake cycle. This can be due to different erase properties of the oxide and ONO interpoly dielectric. U.V. erase speed for EPROM cells with ONO interpoly dielectric usually becomes slower than that with oxide interpoly dielectric [43]. The erase time in the program-bake-erase-bake cycle was the same for both device types (about 20 min).

3.3 Electronic Leakage

Section 3.2 allows the conclusion that electronic leakage is responsible for the non defective charge loss in the examined devices. Hole transport can be neglected due to the lower tunnel probability compared to that of electrons.

Figure 3.4 shows the drain-source current for oxide and ONO devices at intermediate measurements during a bake experiment at three temperatures. There is no basic difference in the charge loss characteristics between the devices with oxide and ONO interpoly dielectric. The oxide field of both lots

![Graph showing drain-source current versus time for oxide and ONO devices at three temperatures]}

**Figure 3.4:** Drain-source current of oxide and ONO devices versus time with bake temperature as parameter, mean values over 10000 cells.
3.3 Electronic Leakage

is the same for a given floating gate voltage (see Section 2.1). Each dot in Figure 3.4 represents the average value of 10000 cells distributed on five devices. The different initial drain-source current between oxide and ONO devices are probably due to a calibration problem of the tester, since oxide devices being measured more than one year after the ONO devices. Compared to this, there is no difference between the measured drain-source currents of oxide and ONO devices during the first bake presented in Figure 3.3 which were performed simultaneously on both device types.

From this experiment it can be concluded that charge transport action should be limited by the oxide conductivity. This can be confirmed by the results given in Ref. [53, 80] in which charge loss measurements on EPROM split lots with different nitride thicknesses of the ONO interpoly dielectric are reported. The charge loss characteristics show two initial charge loss phases which saturate after about 100 h at 250 °C, and a long term charge loss phase. The initial charge loss phases are strong functions of nitride thickness while the nitride has no influence on the long term charge loss phase. Similar activation energies of long term charge loss at EPROMs with oxide and ONO interpoly dielectric also confirm this result [62, 50, 51, 55, 2]. The range from 1 eV to 1.9 eV has been measured for temperatures from 200 °C to 425 °C. The activation energy in pure nitride capacitors was reported to be less than in capacitors with oxide [64].

Reprogramming an already baked device and performing a second bake shows no difference of the drain-source currents compared to the first bake up to 10 h at 350 °C (see Figure 3.5). After 10 h the charge loss during the second bake is less than during the first bake. A possible explanation is that there is no charge accumulation in the interpoly dielectric during the first bake. Charge accumulation would cause a different initial condition compared to the first bake. However, charge accumulation during the first bake may be removed due to the high electric field across the interpoly dielectric during reprogramming. Charge loss through the interpoly dielectric during the first bake may create traps along the charge loss pass which are filled during the second bake. The trapped negative charge would reduce the electric field on the floating gate side which would lead to a smaller charge loss during the second bake. For a reliable explanation, charge accumulation in equivalent test capacitors should
be examined by measuring the flatband voltage shift during high temperature storage with small electric fields in the oxide or ONO interpoly dielectric.

It has been reported that the main path for non defective charge loss in EPROMs with ONO interpoly dielectric is through the ONO [53 – 55]. This can be verified by applying high voltage on the control gate of programmed and erased cells. The electric field of the programmed cell is small across the gate oxide and high across the interpoly dielectric. The condition of the erased cell is reversed. If there is no charge gain on the erased cells but a charge loss of the programmed cells during a bake it can be concluded that the charge transport occurs through the interpoly dielectric. This experiment was performed within the scope of this work with the control gate-to-source voltage between 4 V and 7 V at 250 °C. But since no difference was observed compared to the normal bake without bias, it has to be doubted that the voltage applied outside of the device actually reached the control gates. The devices were operating outside of the specified temperature range. The test was redone at 150 °C. But no change of the initial condition could be measured.

Figure 3.5: *Drain-source current of oxide devices versus time at 350 °C, mean values over 2000 cells.*

![Graph showing drain-source current of oxide devices versus time at 350 °C, mean values over 2000 cells.](image)
3.4 Defect Related Charge Loss

during 4000 h bake. In the impossibility to find a better proof, we rely here on the cited literature.

In Ref. [43, 45, 46, 53] extensive investigations about the influence of the individual layer thicknesses in the ONO interpoly dielectric on charge loss are published. The charge loss was measured during bakes at 250 °C and 300 °C. Reduction of the top-oxide thickness of an ONO with a thick bottom oxide (150 Å) shows no influence on the charge retention capability as long as the top oxide is thicker than 30 Å. For top oxides thinner than 30 Å the charge loss increases with decreasing top oxide thickness. To examine the influence of the nitride thickness two device groups were measured, one with top oxide thinner than 30 Å and one with thicker top oxide. When the top oxide is thin, a thicker nitride leads to enhanced charge loss if the equivalent oxide thickness is kept constant, i.e. the bottom oxide thickness has to be decreased with increasing nitride thickness. In the case where the top oxide is thicker than 30 Å the nitride thickness dependence on long term charge loss is small. The initial charge loss still increases with increasing nitride thickness as in the case of thin top oxide. Bottom oxide scaling, down to around 100 Å, does not lead to a degradation of the data retention capability. Missing bottom oxide (ON interpoly dielectric) leads to large charge loss. However, if the top oxide thickness on the ON interpoly dielectric is increased, charge loss decreases. These results can be explained as follows: A top oxide thicker than 30 Å can block hole injection from the control gate into the nitride while the bottom oxide thickness has influence on electron injection from the floating gate into the nitride. Nitride conductivity is larger than oxide conductivity. In the case of thin top oxide holes injected from the control gate can recombine with electrons leaking through the bottom oxide. Since the tunnel probability of electrons is larger compared to that of holes the bottom oxide must be thicker than the top oxide. If the bottom oxide is missing (ON interpoly dielectric), charge loss must be prevented by a thicker top oxide.

3.4 Defect Related Charge Loss

Defects in the dielectrics surrounding the floating gate leading to electronic leakage result in charge loss or charge gain on the floating gate. The affected
cells are generally randomly located in the memory array [62, 40]. The reliability of the device is ruled by the retention time of the worst cell. The accelerated life test on floating gate memories is widely used as a reliability characterization methodology. It is based on the fact that the data retention failure mechanisms are enhanced by the temperature and the involved electric fields. But ideally, no failure mechanisms besides those at nominal operating conditions will be activated. Failure rates are then estimated by these accelerated life test data and are transformed to nominal operating conditions once the failure mechanisms are understood and the relative accelerating factors are known [8, 13]. We observed that high temperature storage can cause single bit charge loss generally related to defects, which were not present after operating at nominal conditions for 10 years.

3.5 Data Processing

Figure 3.4 already presented the average value of the charge loss measurements of the two investigated lots. This Section describes the total quantity of the measurements. After programming the cells of 15 devices with oxide and 15 devices with ONO as interpoly dielectric, a bake at 250 °C, 300 °C and 350 °C was performed. On each device the drain-source current of 2000 cells was measured as described in Section 3.1.

Figure 3.6 presents the histogram of the drain-source current measurements of one device. There has been no single bit charge loss seen among the measured cells. This results are true for all 30000 measured cells over the bake of 2000 h although, several single bit charge losses were observed on the investigated devices, but not considered in the evaluation.

Figure 3.7 compares the charge loss characteristic of two devices at the same bake conditions. The average value of both devices is about the same at the initial state, while a significant difference appears with increasing bake time.

Figure 3.8 shows the drain-source current of 10 individual cells at 350 °C versus bake time. The cell addresses are randomly selected out of the 5 ONO devices. The drain-source currents do not keep the position in the heap.
3.5 Data Processing

Figure 3.6: Histogram of the drain-source current of an ONO device measured on $N = 2000$ cells at 350 °C.

Figure 3.7: Histogram of the drain-source current of two ONO device (one white, the other black) measured on $N = 2000$ cells at 350 °C.
Figure 3.8: Drain-source current versus bake time. The 10 individual cells, distributed on 5 ONO devices, do not keep their position in the heap.

Figure 3.9: Drain-source current of ONO devices versus time with bake temperature as parameter. Measured average (dots), minimum/maximum (error bars) and fit (solid lines), employed in further calculations.
3.6 Current-Voltage Characteristic

Figure 3.10: Arrhenius plot of data retention rate versus temperature for 25 µA and 75 µA drain-source current. The activation energy is 1.2 eV.

The dots in Figure 3.9 show the average of the drain-source current of all 10000 cells of the same temperature. The error bars mark the minimum and the maximum. The solid line fits are employed in further calculations. The initial state of all measurements was almost the same and no change occurred until the first intermediate measurement.

Assuming that the temperature behavior of the charge loss rate for a given drain source current is according to $1/t = \exp(-E_a/kT)$, an activation energy of 1.2 eV has been estimated (see Figure 3.10).

3.6 Current-Voltage Characteristic

By the model described in Section 2.2, the floating gate charge $Q_F$ can be calculated from the measured drain-source current by using eqns. (2.6) in (2.2) and (2.3) and solving this according to $Q_F$. Thus, the floating gate charge is
Experimental Investigations

\[ Q_F = C_T \left( U_t - \alpha_G U_{GS} - \alpha_D U_{DS} - \alpha_F \frac{U_{DS}}{2} + \sqrt{\frac{2b I_D}{\beta}} \right) \]  \hfill (3.1)

for \( I_D < \frac{b \beta}{2} U_{DS}^2 \) and

\[ Q_F = C_T \left( U_t - \alpha_G U_{GS} - \alpha_D U_{DS} - \alpha_F \frac{U_{DS}}{2} + b \frac{U_{DS}}{2} + \frac{I_D}{\beta U_{DS}} \right) \]  \hfill (3.2)

for \( I_D \geq \frac{b \beta}{2} U_{DS}^2 \),

while \( U_{DS} = U_{DS0} - R_D I_D \). The derivative of this charge is the current leaking through the interpoly dielectric: \( I = dQ_F / dt \). The voltage drop across the interpoly dielectric is given by eqn. (2.9) during the bake.

Figure 3.11 shows the floating gate charge versus bake time calculated with eqns. (3.1) and (3.2), fitted from the measured drain-source current during the
Figure 3.12: Leakage current versus bake time. The long term charge loss starts where the leakage current reaches its maximum.

bake experiment (see Fig. 3.9). Figure 3.12 presents the leakage current versus bake time. In Figure 3.13, this leakage current is plotted versus the floating gate voltage calculated with eqn. (2.9) at corresponding times.

The initial floating gate charge in Figure 3.11 corresponds to about 95000 electrons. The charge loss characteristics at 350 °C and 300 °C describe more than 60% charge loss from the floating gate. The long term charge loss starts where the leakage current presented in Figure 3.12 reaches its maximum. Up to this point about 4000 electrons have left the floating gate, independent of the temperature. This is less than 5% of the initial floating gate charge. During the initial charge loss phase some of these electrons will be trapped in the interpoly dielectric, while the long term charge loss sets in after steady state condition is established. In Figure 3.13, the long term leakage current is plotted versus the floating gate voltage at corresponding bake times. This current-voltage characteristic is used to examine the charge transport mechanism through the interpoly dielectric in Chapters 4 and 5.
3.7 Conclusions

From a program-bake-erase-bake cycle it was possible to find out that long term charge loss is not due to mobile ions. It was reported that a top oxide thicker than 30 Å can block hole injection from the control gate into the nitride [43, 44]. Thus, the long term charge loss of the examined devices is limited by the oxide conductivity of the ONO interpoly dielectric. In the nitride the conductivity is larger than in the oxide. Since hole injection from the control gate into the nitride is prevented by the 70 Å thick top oxide, charge loss is due to leakage of electrons.

Figure 3.13: Leakage current versus floating gate voltage calculated from the data retention experiment.
Traditional Charge Transport Mechanisms

This chapter compares the electric field and temperature dependence of the traditional charge transport mechanisms with the measured charge transport characteristic. The traditional transport mechanisms form basically three groups: 1. Electrode limited conduction (Richardson emission, Fowler-Nordheim tunneling, direct tunneling) 2. Bulk limited conduction (hopping conduction, Poole-Frenkel conduction, field ionization of trapped electrons, space charge limited current), and 3. Conduction depending on both electrode and bulk properties (trap-assisted tunneling, resonant tunneling). However, the experimentally observed leakage current cannot be explained by pure electrode limited charge transport as well as by bulk limited currents or by field gain on asperities and along edges.

4.1 Electrode Limited Conduction

When electrons travel through a dielectric in free flight (i.e. without scattering due to phonons or impurities), the current is limited only by the electrode injection phenomena. In classical mechanics, an electron cannot cross an energy barrier unless its energy at the dielectric interface is greater than the energy barrier. However, electrons with less energy still have a non-zero transition probability (tunnel probability). Depending on the energy level where the dominant transition occurs, the current density through the dielectric
can be described by different approximations [26]. In the case of high temperature, electrons can have sufficient energy to surmount the energy barrier. This can be described by Richardson emission. In the case of high electric field (greater than 5 MV/cm) or small dielectric thickness (less than 100 Å), the dominant transition occurs at Fermi level. This can be described either by Fowler-Nordheim tunneling for high electric fields or by direct tunneling for small dielectric thickness.

An electron inside of the dielectric induces an electric field on the interface of the dielectric. This electric field can be described by the charge itself and an image charge which is symmetrical positioned with respect to the interface. As a result of this electric field the energy barrier has a round edge. This effect is called the image force or image charge effect. The superposition of an external electric field leads due to the round edge to a field dependent barrier lowering.

The tunnel emission described by eqn. (4.1) includes both, direct tunneling for $\phi_o - q F d > 0$ and Fowler-Nordheim tunneling for $\phi_o - q F d < 0$ [18]

$$J_1 = \frac{q [\varphi(F) + q F d]^2}{8\pi d^2 h\phi_o} \exp\left[-\frac{4}{3} \left(\frac{\phi_o}{h\theta_o}\right)^{3/2} + \frac{4}{3} \left(\frac{\varphi(F)}{h\theta_o}\right)^{3/2}\right]$$

(4.1)

with

$$\varphi(F) = (\phi_o - q F d) \Theta(\phi_o - q F d),$$

(4.2)

and

$$h\theta_o = \left(\frac{\hbar^2 q^2 F^2}{2 m_{c,o}}\right)^{1/3}.$$  

(4.3)

$F$ is the electric field in the oxide, $\phi_o$ is the energy barrier of the conduction band edge between semiconductor and oxide on the electrode side, $m_{c,o}$ is the effective electron mass in the oxide and $d$ is the oxide thickness. $\Theta(F)$ denotes the step function and $h\theta_o$ is the electrooptical energy
4.1 Electrode Limited Conduction

for electron tunneling (i.e. 0.15 eV for $F = 2$ MV/cm). There is no image force effect included in this approximation because its influence is less than 1% which is insignificant compared to the large range of current density plotted in Figure 4.1 [32]. Direct tunneling is a strong function of the dielectric thickness; this is shown in Figure 4.2 using eqn. (4.1). The flat part at 4 MV/cm and 5 MV/cm is due the thickness independent Fowler-Nordheim approximation.

The Richardson emission is described by eqn. (4.4). A weak electric field dependence results from the barrier lowering $\Delta \phi$ introduced by the image force effect. $\varepsilon_o$ is the permittivity of oxide and $kT$ denotes the thermal energy (i.e. 26 meV at 300 K)

$$J_2 = \frac{4\pi q m_{c,o} (kT)^2}{h^3} \exp\left(-\frac{\phi_n - \Delta \phi}{kT}\right)$$  \hspace{1cm} (4.4)

with

$$\Delta \phi = q \sqrt{\frac{qF}{4\pi \varepsilon_o}}.$$ \hspace{1cm} (4.5)

The total electrode limited current is the sum of both, tunnel emission and Richardson emission $J = J_1 + J_2$.

In Figure 4.1 the electrode limited current is compared with the current density from the charge loss experiment and from I-V measurements. The I-V measurements have been performed on test capacitors. The oxide was grown on a high n-doped substrate, resulting in a nominal thickness of 100 Å. The gate electrode is formed of high n-doped poly silicon. A negative voltage ramp was applied to the gate electrode for the measurement. Thus, the voltage polarity is the same like across the interpoly dielectric in bake condition. At high electric fields, the Fowler-Nordheim tunneling (which is not temperature dependent) can explain the I-V measurements, while the Richardson emission which is dominant at low electric fields and high temperatures can not explain the charge loss measurements.
Figure 4.1: Current density versus electric field: electrode limited current (solid lines), charge loss and I-V measurements (dots).

Figure 4.2: Tunnel emission versus oxide thickness with electric field as parameter. A 40 Å thick oxide would give a current density of about $10^{-12} \text{A/cm}^2$ due to direct tunneling.
4.2 Bulk Limited Conduction

In the case of bulk limited conduction, the current density is described by the capture and emission process of charge carriers (electrons or holes) which move from one trap to the other. Traps are defects in the bulk or on the interface of a dielectric, which interact with charge carriers. The current density is not limited by the charge injection process into the dielectric. Based on the value of its ionization energy, a trap can be classified as shallow or deep. Based on its propensity for capturing a given type of carrier, a trap can be referred to as an electron or hole trap. Based on its state of charge when empty or filled, a trap can be considered as an acceptor or donor center. Based on its capture cross-section a trap can be considered as coulombic attractive, coulombic repulsive, or neutral [7].

Table 4.1 summarizes the basic bulk limited conduction mechanisms and shows their dependence on electric field and temperature [69, 70, 26, 19, 5, 7]. $\varepsilon_o$ denotes the permittivity in the dielectric, $m_{c,o}$ the effective electron mass in the dielectric, $\phi_i$ the trap depth, $\Delta\phi_a$ the activation energy of electrons and $\mu(T)$ their mobility. The Poole-Frenkel conduction is due to

<table>
<thead>
<tr>
<th>Process</th>
<th>Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poole-Frenkel conduction</td>
<td>$J \sim F \exp \left( -\frac{\phi_i - q \sqrt{q F / \pi \varepsilon_o}}{kT} \right)$</td>
</tr>
<tr>
<td>field ionization of trapped electrons</td>
<td>$J \sim F^2 \exp \left( -\frac{4 \sqrt{2 m_{c,o} \phi_i^3}}{3 \hbar q F} \right)$</td>
</tr>
<tr>
<td>hopping conduction</td>
<td>$J \sim \frac{F}{T} \exp \left( -\frac{\Delta\phi_a}{kT} \right)$</td>
</tr>
<tr>
<td>space charge limited current</td>
<td>$J \sim \mu(T) F^2$</td>
</tr>
</tbody>
</table>

Table 4.1: Bulk limited conduction mechanisms.
field-enhanced thermal excitation of trapped electrons into the conduction band. For trap states with coulomb potential, the quantity of barrier lowering $\sqrt{qF/\pi\varepsilon_o}$ is twice as large for a given electric field as the one due to image force effect in the case of Richardson emission. The second mechanism in Table 4.1 describes field ionization of trapped electrons into the dielectric conduction band. This is a tunneling process essentially independent on temperature and strong dependent on electric field. The third mechanism in Table 4.1 is ascribed to the hopping of electrons from one isolated state to an other, i.e. thermally excited electrons tunnel through the energy barrier between two electron traps. The last mechanism in Table 4.1, the space charge limited current results from a carrier injection into the dielectric, where no compensating charge is present and thus, the assumption of constant electric field is no longer valid.

In Ref. [69] it is concluded that in the case of nitride dielectric the total bulk limited current density is the sum of the first three mechanisms described in Table 4.1. For a given dielectric, each conduction mechanism may dominate in certain temperature and electric field ranges. At high temperatures and high fields (greater than 50 °C at 5.3 MV/cm) Poole-Frenkel conduction is dominant. At low temperatures and high fields (less than -80 °C at 5.3 MV/cm) the current density is due to field ionization of trapped electrons. At low electric fields and moderate temperatures (less than 2 MV/cm at 25 °C) hopping conduction is dominant [69].

Figure 4.3 to 4.5 show the experimentally observed leakage current versus floating gate voltage as it was derived in Section 3.6. The data are the same but the axes are transformed in a way that one of the plots would show straight lines if the electric field dependence acts according to Poole-Frenkel conduction, hopping conduction or space charge limited current.

Figure 4.3 shows that the charge loss mechanism has an electric field dependence which may correspond to the one of Poole-Frenkel conduction. Also the slope is correct if the oxide permittivity is used for the calculation. A similar result is already reported in Ref. [55]. However, according to Ref. [26] the Poole-Frenkel mechanism is different for thin and thick dielectrics. In the case of thick dielectrics the parameter $\phi$, denotes the trap depth while for
Figure 4.3: Leakage current versus square root of floating gate voltage according to the Poole-Frenkel conduction mechanism.

Figure 4.4: Leakage current versus floating gate voltage according to the hopping conduction mechanism.
**Figure 4.5: Leakage current versus square of floating gate voltage according to the space charge limited current mechanism.**

Thin dielectrics, which is the present case, it should denote the barrier height between Si and SiO₂. Thus $\phi_i$ must be about 3.1 eV which can not explain the activation energy of 1.2 eV, which was measured by the bake experiments. Field ionization of trapped electrons can also not explain the charge loss measurements because it is a pure tunneling process which is not dependent on temperature. Hopping conduction yields an ohmic characteristic exponentially dependent on temperature. Figure 4.4 shows that the measured leakage current has not an ohmic characteristic. Figure 4.5 shows that charge limited current also has not the required electric field dependence.

**4.3 Electric Field Gain on Asperities and Edges**

In this work, it has been verified that the effect of field gain on asperities and along edges can not increase the charge loss current to the range experimentally observed. The field gain $G$ is defined as the ratio of the field at any place in the dielectric and the homogeneous field [10]. The worst case
4.3 Electric Field Enhancement on Asperities and Edges

Edge around the floating gate can be described by two angular plates, displaced by a distance \( d \) (see Figure 4.6). P. Henrici presents in Ref. [25] a nearly complete compilation of plain potential problems with sharp or round corners solved by conform transformation technique.

Figure 4.6 shows the transformed regular grid of equipotential lines and field lines, and Figure 4.7 compares the potential distribution along two selected field lines, one starting on the round edge and ending in the opposite edge and the other being situated in the homogeneous region (see Appendix A5). The maximum field gain appears along the bent floating gate-dielectric interface. It is constant along the entire curve and can be calculated with

\[
G = \left( \frac{8}{3\pi} \frac{h^2 + d^2 h}{d^2 r} \right)^{1/3},
\]

(4.6)

or

\[
G = \left( \frac{16}{3\pi} \frac{d}{r} \right)^{1/3}
\]

(4.7)

for \( h = d \). Here, \( h \) and \( d \) denote the horizontal and vertical distance of the plates, respectively and \( r \) is the bending radius.

The question is, whether this field gain can increase the electrode limited current to the range of the charge loss measurements. With eqn. (4.7) a field gain \( G = 2.2 \) is calculated for \( d = 200 \, \text{Å} \) and \( r = 30 \, \text{Å} \). The Fowler-Nordheim and Richardson approximations are derived with the assumption that the electric field is constant in the entire dielectric. This means that using an enhanced electric field by a factor \( G \) in eqn. (4.1) and (4.4) will overestimate the current density. Figure 4.1 shows that an increase of the electric field from 2 MV/cm to about 4 MV/cm can not increase the electrode limited current to the required range. But it is also seen that a significant influence occurs at high electric fields due to field gain along edges (see also [15, 16, 4, 9, 42, 57, 71 – 73]). The exact current density results by calculating the tunnel probability through an energy barrier with the conduction band edge according to the potential distribution plotted in Figure 4.7 [65].
Figure 4.6: Electrostatic potential in the interpoly dielectric near a floating gate edge. Equipotential lines (solid lines) and electrostatic field lines (dashed lines).

Figure 4.7: Electrostatic potential along electrostatic field line: near the above described floating gate edge (solid line) and in the homogeneous region (dashed line). The maximum electrostatic field occurs at $x = 0$. 
New Approach

A trap-assisted tunneling mechanism is proposed in this chapter as a model, where electrons tunnel to oxide traps and are then re-emitted. The electron-phonon coupling results in virtual energy levels in the oxide which allow for more effective tunneling paths. Trap levels between 1.5 eV and 1.7 eV, measured from the conduction band edge, give the dominant contribution to the current density at high temperatures and low electric fields. The most effective traps are located close to the floating gate-bottom oxide interface. A trap density \( N_t = 6.5 \cdot 10^{15} \text{ cm}^{-3} \) and a lattice relaxation energy \( \varepsilon_R = 0.36 \text{ eV} \) result in good agreement with the measured field and temperature dependence of the steady-state leakage current.

5.1 Model based on Multiphonon-Assisted Tunneling

The main path for charge loss in EPROMs with ONO interpoly dielectric is through the ONO [53 – 55]. Electrons stored on the floating gate may be captured by traps in the bottom oxide and then emitted into the nitride by a multiphonon-assisted tunneling process. In the nitride, the conductivity is larger than in the oxide. It is assumed that electrons which have passed the bottom oxide can pass the top oxide, likewise. Hole transport from the control gate is prevented by the 70 Å thick top oxide. Figure 5.1 illustrates the charge transport mechanism through the bottom oxide.
Although in the present case silicon, oxide, and nitride are not crystalline, sharp conduction band edges are assumed as in the case of single crystal materials. It is also assumed that the bottom oxide contains monoenergetic electron traps with a constant spatial density $N_t$ and a thermal binding energy $E_t$. The interaction between electrons and oxide phonons, described by an effective phonon energy $\hbar \omega_0$, and two coupling constants – the lattice relaxation energy $\varepsilon_R$ and the Huang-Rhys factor $S$ – results in a thermal broadening of the trap level $E_t$. A series of virtual states of the coupled electron-phonon system in the energy gap of the oxide occurs which allows for more effective tunneling paths. The "ladder" of these states is indicated in Figure 5.1. Each sub-level can serve as initial state for the multiphonon-assisted tunneling transition into the nitride after the electron has been captured by the trap. The occupation probability of the traps is defined by

$$f_t = \frac{n_t}{N_t},$$  \hspace{1cm} (5.1)$$

where $n_t$ is the density of filled traps. The rate of charge carriers (per volume and time) that occupy or leave the traps can be expressed by

**Figure 5.1:** Energy band diagram illustrating one possible trap-assisted tunneling path.
5.1 Model based on Multiphonon-Assisted Tunneling

\[ R_i(x) = \tau_i^{-1}(x) N_i (1 - f_i), \quad (5.2) \]

\[ R_r(x) = \tau_r^{-1}(x) N_r f_r, \quad (5.3) \]

where \( \tau_i \) and \( \tau_r \) are the time constants for capture or emission of electrons, respectively. The difference of these two rates defines the variation of the trapped charge density with time

\[ \frac{dn_i(x)}{dt} = R_i(x) - R_r(x). \quad (5.4) \]

Under steady state conditions, \( \frac{dn_i}{dt} = 0 \) or equivalently \( R = R_i = R_r \). Using eqns. (5.1) to (5.3) and assuming steady state, the rate of charge carriers per volume and time passing the isolation via traps is given by

\[ R(x) = N_i \frac{1}{\tau_i(x) + \tau_r(x)}, \quad (5.5) \]

and the current density contribution from the traps in a small interval \( dx \) at a distance \( x \) is

\[ dJ(x) = q R(x) dx. \quad (5.6) \]

The time constants \( \tau_i \) and \( \tau_r \) contain characteristic quantities of the floating gate, oxide, and the nitride; namely the density of states in the conduction band of the floating gate \( N_i \) and nitride \( N_r \), the occupation probability in the conduction band of the floating gate \( f_i \) and nitride \( f_r \), and the tunnel probability \( T_i \) from the floating gate to a trap at distance \( x \) and the tunnel probability \( T_r \) from this trap to the nitride

\[ \tau_i^{-1}(x) = \int_{E_{i}(x)}^{E_{t}(x)} N_i(E) f_i(E) T_i(E,x) c_n(E,x) dE, \quad (5.7) \]

\[ \tau_r^{-1}(x) = \int_{E_{i}(x)}^{E_{t}(x)} N_r(E) [1 - f_r(E)] T_r(E,x) e_n(E,x) dE. \quad (5.8) \]
Here, $c_n(E,x)$ denotes the capture rate

$$c_n(E,x) = c_0 \sum_{l=0}^{\infty} L_l(z) \delta(E - E_l(x)), \quad (5.9)$$

with $L_l(z)$ as in eqn. (5.12) and $e_n(E,x)$ the emission rate according to [60, 61]

$$e_n(E,x) = c_0 \exp \left[ -\frac{E - E_l(x)}{kT} \right] \sum_{l=0}^{\infty} L_l(z) \delta(E - E_l(x)), \quad (5.10)$$

where $c_0$ is

$$c_0 = \frac{8\pi^2 r_i^3 q^2 F^2 \hbar}{m_{c,a} \phi_{g,a}}, \quad (5.11)$$

with $r_i$ the localization radius of the trap, $q$ the magnitude of electronic charge, $F$ the electric field in the oxide, $m_{c,a}$ and $\phi_{g,a}$ the effective electron mass and the band gap of the oxide, respectively, and $E$ the energy. The energy of the conduction band edge on the left-hand side was set to zero. Only energy levels $E_l(x) = E_l(x) + \ell \hbar \omega_0$, where $\ell$ is a natural number, are allowed for the capture and emission process due to the one-mode model. This selection is done by the delta function $\delta(E)$. The multiphonon transition probability $L_l(z)$ is according to [60, 61]

$$L_l(z) = \left( \frac{f_B + 1}{f_B} \right)^{\ell/2} \exp(-S(2f_B + 1)) L_\ell(z). \quad (5.12)$$

Here, $S$ denotes the Huang-Rhys factor [29], which is a measure of the coupling strength of the electron-phonon interaction, $I_\ell(z)$ the modified Bessel function of order $\ell$ with the argument $z = 2S\sqrt{f_B(f_B + 1)}$, and $f_B$ the Bose function which gives the phonon occupation number

$$f_B = \frac{1}{\exp(\hbar \omega_0 / kT) - 1}. \quad (5.13)$$
The lower integration limit \( E_i(x) = E_{c,o}(x) - \phi \) in eqns. (5.7) and (5.8) indicates that all transitions via virtual states below the trap level were skipped because hole capture from the nitride and hole emission to the floating gate are neglected. \( E_{c,o} \) is the conduction band edge energy in the oxide. The densities of states on the left- and right-hand side of the oxide are taken according to [70]

\[
N_i(E) = N_0 \left( \frac{m_{c,l}}{m} \right)^{3/2} \sqrt{\frac{E - E_{c,l}}{kT}} \Theta(E - E_{c,l})
\]

(5.14)

and

\[
N_r(E) = N_0 \left( \frac{m_{c,r}}{m} \right)^{3/2} \sqrt{\frac{E - E_{c,r}}{kT}} \Theta(E - E_{c,r}),
\]

(5.15)

respectively, with

\[
N_0 = \frac{\sqrt{kT}}{2\pi^2} \left( \frac{2m}{\hbar^2} \right)^{3/2}.
\]

(5.16)

These forms involve two approximations. First, parabolic bands are assumed, although the electron energy can be more than 1 eV above the bottom of the conduction bands. Second, the density of states in the band gap of the floating gate is assumed to be zero. This neglects localized states in the poly silicon band gap and interface states at the poly-SiO\(_2\) interface. In above equations, \( \Theta(E) \) denotes the step function, \( m \) is the electron rest mass, \( m_{c,l} \) and \( m_{c,r} \) are the effective electron masses, and \( E_{c,l} \) and \( E_{c,r} \) are the energies of the conduction band edges on the left- and right-hand side of the oxide, respectively. Using Boltzmann statistics the occupation probability in the floating gate is given according to [70] by

\[
f_i(E) \approx \exp \left( - \frac{E - E_{f,l}}{kT} \right).
\]

(5.17)

\( E_{f,l} \) is the quasi Fermi energy on the left-hand side of the oxide (see Figure 5.1). The floating gate is highly n-doped, thus \( E_{f,l} \approx E_{c,l} \). On the right-
hand side of the oxide the following approximation is used

\[ 1 - f_r(E) \approx 1. \]  
(5.18)

The implication of (5.18) is that every arriving electron finds an empty state. The tunnel probability from the left-hand side to a trap at distance \( x \) and from this trap to the right-hand side can be expressed using the WKB approximation, as in [65],

\[
T_l(E, x) = \exp\left(-2\int_0^x |\kappa(\xi)| \, d\xi \right),
\]  
(5.19)

\[
T_r(E, x) = \exp\left(-2\int_x^d |\kappa(\xi)| \, d\xi \right),
\]  
(5.20)

with

\[
\kappa^2(\xi) = \frac{2 m_{c.o}}{\hbar^2} \left[ E_{c.o}(\xi) - E \right].
\]  
(5.21)

Neglecting the image force effect, assuming a constant electric field in the oxide and an abrupt potential well introduced by the trap, the tunnel probabilities become

\[
T_l(E, x) = \exp\left[ -\frac{4}{3} \left( \frac{\varphi(E, 0)}{\hbar \theta_o} \right)^{3/2} + \frac{4}{3} \left( \frac{\varphi(E, x)}{\hbar \theta_o} \right)^{3/2} \right],
\]  
(5.22)

\[
T_r(E, x) = \exp\left[ -\frac{4}{3} \left( \frac{\varphi(E, x)}{\hbar \theta_o} \right)^{3/2} + \frac{4}{3} \left( \frac{\varphi(E, d)}{\hbar \theta_o} \right)^{3/2} \right],
\]  
(5.23)

with

\[
\varphi(E, x) = (\phi_t - q F x - E) \Theta(\phi_t - q F x - E)
\]  
(5.24)
and

\[ \hbar \theta_o = \left( \frac{\hbar^2 q^2 F^2}{2 m_{c,o}} \right)^{1/3}, \tag{5.25} \]

where \( \phi_i - q F x \) is the conduction band edge energy \( E_{c,o} \) in the oxide. Eqns. (5.9) to (5.18) and (5.22) to (5.25) define all the expressions in (5.7) and (5.8). Due to the delta function in (5.9) and (5.10), the integration over all energies in (5.7) and (5.8) results in a sum over discrete energies \( E_t(x) \)

\[ \tau^{-1}_i(x) = \sum_{\ell=0}^{\infty} \tau^{-1}_{i,\ell}(x) \quad \text{and} \quad \tau^{-1}_r(x) = \sum_{\ell=0}^{\infty} \tau^{-1}_{r,\ell}(x), \tag{5.26} \]

with

\[ \tau^{-1}_{i,\ell}(x) = \tau_0^{-1} \frac{N_i(E_t)}{N_0} f_i(E_t) T_i(E_t, x) L_t(z), \tag{5.27} \]

and

\[ \tau^{-1}_{r,\ell}(x) = \tau_0^{-1} \frac{N_r(E_t)}{N_0} T_r(E_t, x) \text{Exp}\left(-\frac{\ell \hbar \omega_0}{kT}\right) L_t(z), \tag{5.28} \]

where the time constant \( \tau_0 \) is

\[ \tau_0 = \frac{1}{N_0 c_0}. \tag{5.29} \]

Using eqn. (5.6), the total current density is

\[ J = q N_t \int_0^d \frac{1}{\tau_i(x) + \tau_r(x)} \, dx. \tag{5.30} \]

The integration in eqn. (5.30) can be performed numerically.
5.2 Analytical Model Discussion

For the numerical investigations in this work, the electron effective mass in the Si on the left-hand side of the oxide, in SiO₂, and in the Si₃N₄ on the right-hand side of the oxide have been assumed to: \( m_{c,l} = 0.33 \, m \), \( m_{c,o} = 0.42 \, m \) and \( m_{c,r} = 0.42 \, m \). The energy barrier in the conduction band edge from Si to SiO₂ is set to \( \phi_l = 3.1 \) eV and for the energy barrier from SiO₂ to Si₃N₄ \( \phi_r = 1.1 \) eV is used. The effective phonon energy \( \hbar \omega_o \) in the amorphous oxide is assumed to be 60 meV [60]. The time constant, defined in eqn. (5.29)

\[
\tau_0 = \frac{1}{N_0 c_0} = \frac{\hbar \left( \frac{\hbar^2/2m_r^2}{\sqrt{kT}} \right)^{3/2}}{8 \sqrt{kT} \left( \hbar \theta_o \right)^3},
\]

(5.31)

consists of the following quantities: the thermal energy \( kT \) (i.e. 26 meV at 300 K), the energy gap of SiO₂ \( \phi_{g,o} = 8.9 \) eV, the "kinetic energy" of the defect electron \( \hbar^2/2 \, m \, r_i^2 = 3.81/r_i^2 \) eV with \( r_i \) in Å (i.e. 0.61 eV for \( r_i = 2.5 \) Å) and the electrooptical energy for electron tunneling \( \hbar \theta_o = 7.25 \times 10^{-6} \left( F^2 m/m_{c,o} \right)^{1/3} \) eV with \( F \) in V/cm (i.e. 0.15 eV for \( F = 2 \) MV/cm). The time constant \( \tau_0 \) is \( 5.9 \times 10^{-13} \) s for \( F = 2 \) MV/cm. Since this value is in the range from \( 10^{-12} \) s to \( 10^{-14} \) s it is in good agreement with Ref. [36, 67]. The model has two more parameters, the trap density \( N_t \) and the Huang-Rhys factor \( S \), which will be discussed in Section 5.4. The Huang-Rhys factor \( S \) and the phonon energy \( \hbar \omega_o \) define the lattice relaxation energy \( \epsilon_k = S \hbar \omega_o \). This energy must be small compared to the energy gap of SiO₂ \( \phi_{g,o} \).

The electron-phonon coupling is switched off if the Huang-Rhys factor \( S \) in eqn. (5.12) is set to zero. Then, the capture and emission rate defined in eqns. (5.9) and (5.10) turn into

\[
c_n(E,x) = c_0 \, \delta(E - E_t(x)),
\]

(5.32)

\[
e_n(E,x) = c_0 \, \exp \left[ -\frac{E - E_t(x)}{kT} \right] \, \delta(E - E_t(x)).
\]

(5.33)
5.2 Analytical Model Discussion

Figure 5.2: Inverse time constants $\tau_{i,\ell}^{-1}$ and $\tau_{r,\ell}^{-1}$ versus energy. The emission occurs at energies close to the oxide conduction band edge.

Figure 5.3: Arrhenius plot of the current density versus temperature. Multiphonon process (solid line) and zero-phonon process (dashed line).
The capture and emission process is reduced to one tunnel path at the trap energy $E_r$ and the integration in eqn. (5.7) and (5.8) only consists of the contribution from this energy level. Compared to this, Figure 5.2 shows the contributions to the sums $\tau^{-1}_i$ and $\tau^{-1}_e$ at higher energies for $T = 600$ K, $\hbar \omega_0 = 60$ meV, and $S = 6$ (lattice relaxation energy $\varepsilon_R = S \hbar \omega_0 = 0.36$ eV). The maximum of the capture and emission spectra occurs at different energies. The calculations show that for high temperature ($T = 600$ K), the capture process occurs at about trap level, while the emission process occurs close to the oxide conduction band edge. With decreasing temperature the dominant contributions of the emission process shifts towards lower energies.

Figure 5.3 shows the influence of the electron-phonon coupling on the temperature dependence. The solid line is calculated from eqn. (5.30) with $S = 6$ ($\varepsilon_R = 0.36$ eV) and the dashed line with $S = 0$. The temperature dependence of the zero-phonon process, also called two-step tunneling, is too weak to explain the strong temperature dependence of the measured charge loss data. In the two-step tunneling mechanism the temperature dependence results only from the occupation probability of electrons in the conduction band of the floating gate. Figure 5.3 shows that the electron-phonon coupling is relevant only at high temperatures. With decreasing temperature its influence on the current density becomes less and the mechanism approaches to the two-step tunneling mechanism.

Analyzing the transition rate $R(x)$ defined in eqn. (5.5) as a function of trap position $x$ for different trap depths $\phi$, at room temperature and for an electric field of $F = 2$ MV/cm, it turns out that deep traps ($\phi$ greater than 2.2 eV) are most effective, if they are located in the center of the oxide layer. This is illustrated by Figure 5.4. The most effective traps are those for which the capture rate is equal to the emission rate, i.e. $\tau_c(x) = \tau_e(x)$, see eqn. (5.5). A similar result as in Figure 5.4 was obtained by analyzing the transition rates of two-step tunneling [81] and resonant tunneling.

With increasing temperature the electron-phonon coupling becomes more important. As a result, the most effective traps are located close to the floating gate-bottom oxide interface independent of their energy. This is because the first step restricts the whole process, i.e. the emission rate is larger than the
capture rate. The restriction is due to the small thermal occupation probability of the corresponding energy levels in the floating gate. Then the transition rate becomes largest with maximum tunnel probability for the first step, i.e. for $x = 0$. Consequently, the mechanism is only weak dependent on the oxide thickness. High electric fields make tunneling more important for the complex process. The emission occurs at lower energies which makes the mechanism less distinguishable from the pure two-step tunneling transition.

In Figure 5.5 the current density is plotted versus the trap depth $\phi$, for two values of the electric field. A maximum appears at 1.6 eV and 1.7 eV. The current density changes by many orders of magnitude as the trap depth varies. Various trap levels have been reported for SiO$_2$. Since a very low trap density is sufficient to explain the measured current density with the multiphonon-assisted tunneling mechanism it is assumed that all energy levels are available in the range between 1.5 eV and 1.7 eV. Figure 5.6 shows the dependence of the trap depth resulting in the largest current density on electric field and temperature.
Figure 5.5: Current density versus trap energy measured from the conduction band edge.

Figure 5.6: Trap energy resulting in the largest current density measured from the conduction band edge versus electric field with temperature as parameter.
Instead of integrating the current density contributions over all trap energies only the maximum has been calculated. The half-width of the current density distribution in Figure 5.5 is about 0.2 eV at 600 K. Thus, the trap density $N_t$ refers to an energy interval of about 0.2 eV. The deeper traps are also used by carriers but with a much lower probability. It is assumed that all traps at any $E_t$ have similar microscopic coupling constants thus, the transition rates differ due to $E_t$, only. More permanent occupation of deeper traps has to be expected. That contributes to a steady state charge density in the oxide. Such charges could behave like "fixed" charges, i.e. they are present before and after repeated write operations.

5.3 Electric Field and Temperature Dependence of the Model

The dependence of the current density on the electric field is plotted in Figure 5.7. The dashed line is computed with variable trap depth according to

![Figure 5.7: Current density versus electric field. Constant trap depth (solid lines) and trap depth resulting in the largest current density (dashed line).](image)
Figure 5.8: Arrhenius plot of the current density versus temperature. Constant trap depth (solid lines) and trap depth resulting in the largest current density (dashed line).

Figure 5.6 and is the envelope of the solid lines which are calculated with constant trap depth. In Figure 5.8 the current density versus temperature is plotted in an Arrhenius plot. The activation energy is increasing with temperature while the trap depth giving the largest contribution to the current density is slightly decreasing. A high activation energy indicates a strong temperature dependence. At high temperatures the electron-phonon coupling has a dominant influence on the current density which results into a strong temperature dependence. With decreasing temperature the influence of the electron-phonon coupling becomes less and thus the current density is less temperature dependent.

5.4 Comparison with Experimental Results

The bake experiment has been performed between 250 °C and 350 °C. The electric field in the oxides of the ONO, given by
\[ F_{G,o} = \frac{U_{FS}}{d_{b,o} + \varepsilon_o \varepsilon_n^{-1} d_n + d_{t,o}} \] (5.34)

is less than 2 MV/cm. \( d_{b,o}, d_n \) and \( d_{t,o} \) are the thicknesses of bottom oxide, nitride and top oxide, respectively. \( \varepsilon_o \) and \( \varepsilon_n \) are the permittivities of oxide and nitride.

Figure 5.9 compares the experimental results with those obtained numerically from the model based on the multiphonon-assisted tunneling, by assuming a trap density \( N_t = 6.5 \times 10^{15} \) cm\(^{-3} \) and a Huang-Rhys factor \( S = 6 \). Both values, for \( N_t \) and \( S \) agree with the indications given in the literature, as shown below.

1. In Ref. [7] it is reported, that the trap density of electron traps located on the interface of Si-SiO\(_2\) or poly-Si-SiO\(_2\) over a distance of about 20 Å

![Graph](image)

**Figure 5.9:** Current density versus electric field: measurement (dots) and calculation (solid lines).
New Approach

is in the range of $10^{11}$ cm$^{-2}$ to $10^{13}$ cm$^{-2}$. To compare these values with the trap density in our model, it is necessary to relate the latter one to a single trap energy (because it refers to an energy interval of 0.2 eV) and to a sheet charge with constant spatial density, i.e. $N_s/(dxdE) = 1.7 \cdot 10^{11}$ cm$^{-2}$ eV$^{-1}$. Multiplying the trap density with the volume of the bottom and the top oxide results in 210 traps per EPROM cell in an energy interval of 0.2 eV around the trap level which is giving the largest current density. Assuming this to be an average value over the entire energy gap of SiO$_2$ a total of 9500 traps per EPROM cell can be estimated. Only a fraction of these traps will be actually occupied. Thus, the total trapped charge is comparable to the 4000 electrons which have left the floating gate during the initial charge loss phase (see Section 3.6).

2. In our model, the charge loss is only linear dependent on the trap density $N_s$ (see eqn. 5.30) and has thus no influence on the electric field and temperature dependence of the mechanism. The electric field and temperature dependence is described by involving the electron-phonon coupling, where the Huang-Rhys factor $S$ gives the coupling strength. This factor is not directly measurable in SiO$_2$. For the calculation of the solid lines in Figure 5.9, $S = 6$ was used, which results in a lattice relaxation energy $\varepsilon_R = S \hbar \omega_0$ of 0.36 eV with $\hbar \omega_0 = 60$ meV. Ref. [47] gives for $S$ a range from 4 to 15, appropriate to Li$_x$Ni$_{1-x}$O, and in Ref. [59, 60] a lattice relaxation energy of 0.24 eV is reported for silicon, which is similar to that used here. The latter value is based on experimental data obtained by emission time spectroscopy. However, this energy depends on the defect type which acts as a trap center. Ref. [48] shows that in a given dielectric, many trap centers with different properties can exist. Thus, this parameter is not an intrinsic value of the interpoly dielectric.

From the above considerations we can conclude that the proposed model can be used to describe quantitatively the electric field and temperature dependence of the charge loss in EPROMs with ONO interpoly dielectric. However, this model dose not deliver a closed formula for the computation of the charge loss. For this reason an empirical equation, fitting the experimental data, will be proposed in Chapter 6.
Conclusions

A model for long term charge loss in EPROMs with ONO interpoly dielectric, based on a multiphonon-assisted tunneling mechanism, is proposed in this work. The interaction of localized carriers with oxide lattice vibrations, described by the electron-phonon coupling strength, can explain the temperature dependence of the charge transport, which has been observed experimentally to have an activation energy of 1.2 eV. Previous charge loss models postulate a reduced energy barrier for the polycrystalline Si-SiO₂ interface to describe the measured temperature dependence, although photocurrent measurements show that polycrystalline Si-SiO₂-Al and singlecrystalline Si-SiO₂-Al MOS structures have identical interface energy barrier heights. The present model, based on multiphonon-assisted tunneling delivers an activation energy of 1.2 eV, even using the correct energy barrier height of 3.1 eV.

The model shows that traps play an important role for the data retention time. Since traps can be influenced by the manufacturing process, attention should be paid to trap properties like trap density and electron-phonon coupling strength. However, there are many methods to measure the trap density but not the electron-phonon coupling strength. Emission time spectroscopy, which was used to characterize the electron-phonon coupling strength in silicon, is limited to shallow traps (trap depth less than 0.5 eV measured from the conduction band edge) in oxide. The method fails because the deeper the traps the longer is the emission time. If one has to wait to long to observe emission,
the capture may play a significant role and the method becomes inaccurate. Thus, another method must be found to characterize the electron-phonon coupling strength in oxide.

The multiphonon-assisted tunneling mechanism was applied to the bottom oxide of the ONO dielectric and it was assumed that the top oxide is not charge transport limiting. This assumption could be verified experimentally. However, if the top oxide thickness is decreased, hole injection from the control gate may occur which then accumulate on the bottom oxide-nitride interface. This charge accumulation must be included in the floating gate transistor model to calculate the electric fields in the ONO. If the bottom oxide is too thin, electrons can pass through it by direct tunneling and accumulate on the nitride-top oxide interface. Under these conditions, the assumption that the top oxide is not charge transport limiting is not valid. However, Oxide and ONO devices have about the same charge loss characteristic and in particular the same activation energy. Electrons stored on the floating gate have to pass the same energy barrier between floating gate and oxide in both device types. Thus, it can be expected that charge loss is governed by the same mechanism, i.e. mainly influenced by the oxide properties close to the floating gate.

It was assumed that no charge accumulation in the interpoly dielectric occurs during the bake. Basically, this assumption can be verified by measuring the flatband voltage shift in test capacitors with ONO interpoly dielectric during high temperature storage biased under voltage producing low electric fields in the oxides of the ONO. The flatband voltage shift can give information about polarity and amount of trapped charge. However, it can be expected that different traps (i.e. other energy and location) are responsible for charge accumulation (i.e. more permanent trap occupation) and charge transport. Thus, such an experiment can not be used to verify the trap density which is used in the multiphonon-assisted tunneling mechanism.

The investigations presented in this work lead to the following results:

1. It has been found that long term charge loss is not due to mobile ions in the examined devices. Since hole injection from the control gate into the nitride is prevented by the 70 Å thick top oxide, it can be concluded that
charge loss is due to leakage of electrons. In this case, intrinsic long term charge loss through the ONO interpoly dielectric is limited by the oxide conductivity.

2. The charge loss measurements can be modeled by a multiphonon-assisted tunneling mechanism applied to the bottom oxide of the ONO interpoly dielectric under the assumption that the top oxide is not charge transport limiting. A trap density \( N_t = 6.5 \cdot 10^{15} \text{ cm}^{-3} \) and a lattice relaxation energy \( \varepsilon_R = 0.36 \text{ eV} \), result in good agreement with the measured field and temperature dependence of the steady-state leakage current. The model shows that trap levels between 1.5 eV and 1.7 eV, measured from the conduction band edge, give the dominant contribution to the current density at high temperatures and low electric fields. Furthermore, only traps near the floating gate-bottom oxide interface are active in the steady-state trapping and detrapping process under these conditions. At room temperature deeper trap levels contribute most, which favors traps around the center of the oxide layer. The activation energy decreases with decreasing temperature.

3. Since the numerical evaluation of the multiphonon-assisted tunneling mechanism is very time-consuming, it may be useful to have a simple empirical expression, which describes the dependence on electric field and temperature. Such an expression can be found as \( J \sim \exp[-1.2/(kT)] \exp[8.5 \sqrt{F}] \) with \( k = 8.6 \cdot 10^{-5} \text{ eV/K} \). Here, \( T \) denotes the temperature in °K and \( F \) the electrical field in MV/cm. This empirical expression is valid in the temperature range from 250 °C to 350 °C and for electrical fields between 0.5 MV/cm to 2 MV/cm.

The multiphonon-assisted tunneling mechanism is dominant at high temperatures and low electric fields (greater than 100 °C at 2 MV/cm for a 100 Å thick oxide). With decreasing temperature the mechanism approaches the two-step tunneling mechanism. At high electric fields (greater than about 5 MV/cm for a 100 Å thick oxide) Fowler-Nordheim mechanism becomes dominant. At high electric fields the current density is only weakly temperature dependent. Furthermore for thin oxides and low electric fields, direct tunneling becomes more important. To verify the multiphonon-assisted tunneling
mechanism at room temperature, charge loss measurements should be extended to over more than 10 years. It was shown that with decreasing temperature the present model predicts a decreasing activation energy. This behavior is expected, because at low temperatures the electron-phonon coupling has less influence on the charge transport. Thus, tunneling becomes more important for the capture and emission process which is not temperature dependent.
A1

Notation

\( \alpha_D, \alpha_F, \alpha_G \) Capacitive coupling between drain and floating gate, floating gate and substrate, control gate and floating gate, respectively

\( C_D, C_F, C_G \) Capacitance between drain and floating gate, floating gate and substrate, control gate and floating gate, respectively (F)

\( C_T \) Total capacitance around the floating gate (F)

\( d \) Insulator thickness (m)

\( d_{b,o}, d_n, d_{i,o} \) Thicknesses of bottom oxide, nitride and top oxide, respectively (m)

\( d_F \) Gate oxide thickness (m)

\( d_{G,o} \) Interpoly equivalent oxide thickness (m)

\( \delta \) Delta function

\( c_n, e_n \) Electron capture and emission rate, respectively (m^3 s^{-1})

\( \varepsilon, \varepsilon_n, \varepsilon_o \) Permittivity of vacuum, Si_3N_4 and SiO_2, respectively (F m^{-1})

\( E \) Energy (J)

\( E_{c,l}, E_{c,r} \) Conduction band energy on the left- and right-hand side of the insulator, respectively (J)

\( E_{c,o} \) Conduction band energy in SiO_2 (J)

\( E_t \) Trap energy (J)

\( E_{f,l}, E_{f,r} \) Quasi-Fermi energy on the left- and right-hand side of the insulator, respectively (J)
Appendix

\( f_B \)  
Bose function

\( f_l, f_r \)  
Occupation probability for an energy state on the left- and right-hand side of the insulator, respectively

\( f_t \)  
Trap occupation probability

\( F \)  
Electric field (V m\(^{-1}\))

\( F_F \)  
Electric field between floating gate and channel (V m\(^{-1}\))

\( F_{G,o}, F_{G,n} \)  
Electric field between control gate and floating gate in the oxide and nitride, respectively (V m\(^{-1}\))

\( \phi_{g,o} \)  
Energy gap of SiO\(_2\) (J)

\( \phi_t, \phi_r \)  
Energy barrier on the left- side and on the right-hand side of the insulator, respectively (J)

\( \phi_t \)  
Trap depth measured from the conduction band of the insulator (J)

\( G \)  
Electric field gain

\( h, \hbar \)  
Planck constant and reduced Planck constant, respectively (J s)

\( \hbar \omega_0 \)  
Phonon energy (J)

\( \hbar \theta_0 \)  
Electrooptical energy for electron tunneling (J)

\( I \)  
Leakage current (A)

\( I_D \)  
Drain-source current (A)

\( I_\ell (z) \)  
Modified Bessel function of order \( \ell \)

\( J \)  
Current density (A m\(^{-2}\))

\( k \)  
Boltzmann constant (J K\(^{-1}\))

\( kT \)  
Thermal energy (J)

\( l_F, l_G \)  
Length of gate oxide and interpoly dielectric, respectively (m)

\( m \)  
Electron rest mass (kg)

\( m_{c,l}, m_{c,o}, m_{c,r} \)  
Electron effective mass on the left- side, in SiO\(_2\) and on the right-hand side, respectively (kg)

\( n_t \)  
Density of filled traps (m\(^{-3}\))

\( N_1, N_r \)  
Density of states in the conduction band on the left- and right-hand side of the insulator, respectively (J\(^{-1}\) m\(^{-3}\))

\( N_t \)  
Trap density (m\(^{-3}\))

\( q \)  
Magnitude of electronic charge (C)

\( Q_F \)  
Charge on the floating gate (C)

\( \Theta \)  
Step function
$r_t$  Localization radius of the trap (m)
$R$  Transition rate of charge carriers (m$^{-3}$ s$^{-1}$)
$R_t$, $R_r$  Rate of charge carriers that occupy or leave the traps (m$^{-3}$ s$^{-1}$)
$R_D$  Drain resistance (Ω)
$S$  Huang-Rhys factor
$\tau_o$, $\tau_l$, $\tau_r$  Time constants (s)
$T_l$, $T_r$  Tunnel probabilities for electrons on the left- and right-hand side of the trap
$U_{CS}$  Voltage along the channel (V)
$U_{DS}$, $U_{FS}$, $U_{GS}$  Voltage on the drain, floating gate and control gate, respectively (V)
$U_t$  Threshold voltage (V)
$w_F$, $w_G$  Width of gate oxide and interpoly dielectric, respectively (m)
$\psi_{b,F}$, $\psi_{b,S}$  Bulk potential in the floating gate and substrate, respectively (V)
$x$, $y$, $z$  Cartesian coordinate axes

EPROM  Erasable Programmable Read-Only Memory
E²PROM  Electrically Erasable Programmable Read-Only Memory
ONO  Oxide-Nitride-Oxide
WKB  Wentzel, Kramers, Brillouin (approximation)

All calculations are done by using the international system of units. Nevertheless, some results are presented in different units like eV instead of J or cm$^2$ instead of m$^2$. 
### A2

## Constants

<table>
<thead>
<tr>
<th>Constant</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Permittivity of vacuum</td>
<td>$\varepsilon = 8.854 \cdot 10^{-12} \text{ F m}^{-1}$</td>
</tr>
<tr>
<td>Planck constant</td>
<td>$h = 6.626 \cdot 10^{-34} \text{ J s}$</td>
</tr>
<tr>
<td>Boltzmann constant</td>
<td>$k = 1.380 \cdot 10^{-23} \text{ J K}^{-1}$</td>
</tr>
<tr>
<td>Electron rest mass</td>
<td>$m = 9.109 \cdot 10^{-31} \text{ kg}$</td>
</tr>
<tr>
<td>Magnitude of electronic charge</td>
<td>$q = 1.602 \cdot 10^{-19} \text{ C}$</td>
</tr>
<tr>
<td>Permittivity of SiO$_2$</td>
<td>$\varepsilon_o = 3.9 \varepsilon$</td>
</tr>
<tr>
<td>Permittivity of Si$_3$N$_4$</td>
<td>$\varepsilon_n = 7.5 \varepsilon$</td>
</tr>
<tr>
<td>Reduced Planck constant</td>
<td>$\hbar = h / 2\pi$</td>
</tr>
<tr>
<td>Energy gap of SiO$_2$</td>
<td>$\phi_{g,o} = 8.9 \text{ eV}$</td>
</tr>
<tr>
<td>Energy barrier from Si to SiO$_2$</td>
<td>$\phi_j = 3.1 \text{ eV}$</td>
</tr>
<tr>
<td>Energy barrier from SiO$_2$ to Si$_3$N$_4$</td>
<td>$\phi_r = 1.1 \text{ eV}$</td>
</tr>
<tr>
<td>Electron effective mass in Si</td>
<td>$m_{c,l} = 0.33 \text{ m}$</td>
</tr>
<tr>
<td>Electron effective mass in SiO$_2$</td>
<td>$m_{c,o} = 0.42 \text{ m}$</td>
</tr>
<tr>
<td>Electron effective mass in Si$_3$N$_4$</td>
<td>$m_{c,r} = 0.42 \text{ m}$</td>
</tr>
<tr>
<td>Localization radius of the trap in SiO$_2$</td>
<td>$r_t = 2.5 \text{ Å}$</td>
</tr>
</tbody>
</table>
Tunnel Probability

The tunnel probability at level $E$ through an energy barrier between $x_1$ and $x_2$ can be expressed by using the WKB (Wentzel, Kramers, Brillouin) approach.

$$T(E) = \exp \left( -2 \int_{x_1}^{x_2} \kappa(x) \, dx \right),$$  \hspace{1cm} (A3.1)

with

$$\kappa^2(x) = \frac{2 m_{c,o}}{\hbar^2} \left[ E_{c,o}(x) - E \right].$$  \hspace{1cm} (A3.2)

It must be distinguished whether the tunnel path ends at the conduction band of the isolator or not. Figure A3.1 illustrates the two cases.

Neglecting the image force effect and assuming a constant electric field $F$ in the isolator eqn. (A3.1) can be solved analytically. The conduction band energy is

$$E_{c,o}(x) = \phi_l - q F x.$$  \hspace{1cm} (A3.3)

Using eqns. (A3.2) and (A3.3) in (A3.1) gives
**Figure A3.1:** Energy band diagram illustrating two possible tunneling paths.

\[
\ln[T(E)] = -2 \frac{\sqrt{2 m_{c,0}}}{\hbar} \int_{x_1}^{x_2} \sqrt{\phi_i - q F x - E} \, dx , \quad (A3.4)
\]

\[
\ln[T(E)] = \frac{4}{3} \frac{\sqrt{2 m_{c,0}}}{\hbar q F} \left( \phi_i - q F x - E \right)^{3/2} \bigg|_{x_1}^{x_2} , \quad (A3.5)
\]

For \( \phi_i - q F x - E < 0 \) at \( x = x_2 \) ends in the conduction band of the isolator. This can be expressed by

\[
\varphi(E, x) = (\phi_i - q F x - E) \Theta(\phi_i - q F x - E) , \quad (A3.6)
\]

where \( \Theta(E) \) denotes the step function. Thus, the tunnel probability is

\[
T(E) = \exp \left[ - \frac{4}{3} \left( \frac{\varphi(E, x_1)}{\hbar \theta_o} \right)^{3/2} + \frac{4}{3} \left( \frac{\varphi(E, x_2)}{\hbar \theta_o} \right)^{3/2} \right] , \quad (A3.7)
\]

with

\[
\hbar \theta_o = \left( \frac{\hbar^2 q^2 F^2}{2 m_{c,0}} \right)^{1/3} . \quad (5.25)
\]
Inverse Time Constants

The time constants $\tau_i$ and $\tau_r$ are expressed by

$$\tau_i^{-1}(x) = \int_{E_i(x)}^{E_r(x)} N_i(E) f_i(E) T_i(E,x) c_n(E,x) \, dE,$$  \hspace{1cm} (A4.1)

$$\tau_r^{-1}(x) = \int_{E_r(x)}^{E_i(x)} N_r(E) [1 - f_r(E)] T_r(E,x) e_n(E,x) \, dE.$$ \hspace{1cm} (A4.2)

The density of states in the conduction bands $N_i, N_r$, the occupation probabilities $f_i, f_r$, the tunnel probabilities $T_i, T_r$ from the floating gate to a trap at distance $x$ and from this trap to the nitride, and the capture and emission rates $c_n(E,x), e_n(E,x)$ are described in eqns. (5.9) to (5.18) and (5.22) to (5.25).

Zero-phonon Coupling

The electron-phonon coupling is switched off if the Huang-Rhys factor $S$ in eqn. (5.12) is set to zero. With $I_q(0) = 1$ for $\ell = 0$ and $I_q(0) = 0$ for $\ell \neq 0$ follows: $L_q(0) = 1$ for $\ell = 0$ and $L_q(0) = 0$ for $\ell \neq 0$. The sums in eqns. (5.9) and (5.10) turn into a single expression with $E_r(x) = E_i(x)$. Thus, the time constants defined in eqns. (A4.1) and (A4.2) turn into
\[ \tau^{-1}_t(x) = \tau_0^{-1} \left( \frac{m_{c,t}}{m} \right)^{3/2} \left( \frac{E_t(x) - E_{c,t}}{kT} \right) \Theta(E_t(x) - E_{c,t}) \times \right. \\
\left. \times \exp \left( - \frac{E_t(x) - E_{f,t}}{kT} \right) \times \right. \\
\left. \times \exp \left\{ - \frac{4}{3} \frac{E_{c,o}(0) - E_t(x)}{\hbar \theta_o} \right\}^{3/2} + \frac{4}{3} \left[ \frac{\phi_t}{\hbar \theta_o} \right]^{3/2} \right\} \] (A4.3)

and

\[ \tau^{-1}_r(x) = \tau_0^{-1} \left( \frac{m_{c,r}}{m} \right)^{3/2} \left( \frac{E_t(x) - E_{c,r}}{kT} \right) \Theta(E_t(x) - E_{c,r}) \times \right. \\
\left. \times \exp \left( - \frac{\phi_t}{\hbar \theta_o} \right)^{3/2} + \right. \\
\left. + \frac{4}{3} \left[ \frac{E_{c,o}(d) - E_t(x)}{\hbar \theta_o} \right] \Theta(E_{c,o}(d) - E_t(x)) \right\}^{3/2} \] (A4.4)

with

\[ \tau_0 = \frac{1}{N_0 c_0} = \frac{\hbar}{8} \left( \frac{\hbar^2/2 m r_i^2}{\sqrt{kT}} \right)^{3/2} \frac{\phi_{g,o}}{(\hbar \theta_o)^3}, \] (A4.5)

\[ \hbar \theta_o = \left( \frac{\hbar^2 q^2 F^2}{2 m_{c,o}} \right)^{1/3}, \] (A4.6)

\[ E_{c,o}(x) = \phi_t - q F x, \] (A4.7)

\[ E_t(x) = \phi_t - q F x - \phi_r, \] (A4.8)

\[ E_{c,l} = 0, \quad E_{c,r} = \phi_t - q F d - \phi_r, \quad \text{and} \quad E_{f,l} = E_{c,l} \] (A4.9)
Multphonon Coupling

In the case of multphonon coupling the time constants defined in eqns. (A4.1) and (A4.2) become

\[
\tau^{-1}_r(x) = \tau_0^{-1}\left(\frac{m_{c,l}}{m}\right)^{3/2} \sum_{\ell=0}^{\infty} \sqrt{\frac{(E_{\ell}(x) - E_{c,l})}{kT}} \Theta(E_{\ell}(x) - E_{c,l}) \times \\
\times \exp\left(-\frac{E_{\ell}(x) - E_{f,l}}{kT}\right) L_{\ell}(z) \times \\
\times \exp\left[\frac{4}{3} \left(\frac{E_{c,o}(0) - E_{\ell}(x)}{\hbar \theta_o} \Theta(E_{c,o}(0) - E_{\ell}(x))\right)^{3/2} + \\
+ \frac{4}{3} \left(\frac{E_{c,o}(x) - E_{\ell}(x)}{\hbar \theta_o} \Theta(E_{c,o}(x) - E_{\ell}(x))\right)^{3/2}\right]
\]

(A4.10)

and

\[
\tau^{-1}_l(x) = \tau_0^{-1}\left(\frac{m_{c,l}}{m}\right)^{3/2} \sum_{\ell=0}^{\infty} \sqrt{\frac{(E_{\ell}(x) - E_{c,r})}{kT}} \Theta(E_{\ell}(x) - E_{c,r}) \times \\
\times \exp\left(-\frac{E_{\ell}(x) - E_{l}(x)}{kT}\right) L_{\ell}(z) \times \\
\times \exp\left[\frac{4}{3} \left(\frac{E_{c,o}(d) - E_{\ell}(x)}{\hbar \theta_o} \Theta(E_{c,o}(d) - E_{\ell}(x))\right)^{3/2} + \\
+ \frac{4}{3} \left(\frac{E_{c,o}(d) - E_{\ell}(x)}{\hbar \theta_o} \Theta(E_{c,o}(d) - E_{\ell}(x))\right)^{3/2}\right]
\]

(A4.11)

with

\[
L_{\ell}(z) = \left(\frac{f_B + 1}{f_B}\right)^{\ell/2} \exp[-S (2f_B + 1) I_{\ell}(z),
\]

(A4.12)
\[ z = 2S \sqrt{f_B(f_B + 1)} \quad (A4.13) \]

and

\[ f_B = \frac{1}{\exp(\frac{\hbar \omega_0}{kT}) - 1}. \quad (A4.14) \]

The expressions \( \tau_0, \ h\theta_0, \ E_{c,0}(x), \ E_t(x), \ E_{c,l}, \ E_{c,r}, \ \text{and} \ E_{f,l} \) are the same as defined in eqns. (A4.5) to (A4.9).
P. Henrici presents in Ref. [25] a nearly complete compilation of plain potential problems with sharp or round corners solved by conform transformation technique. The solution given here is slightly more complicated but it gives a more round corner for large curvature radius. The derivation is based on the principal clause for conform transformation [23, 25]. A geometry described in the physical domain (z-plane) is conformally transformed to a model domain (w-plane) by using an analytical function \( w = f(z) \) with its inverse transform \( z = f^{-1}(w) \). If \( \phi(z) \) and \( \psi(w) \) are the potential distributions in the z-plane and w-plane as solution of \( \Delta \phi(z) = 0 \) and \( \Delta \psi(w) = 0 \), then is \( \phi(z) = \psi(w) \). The transformed relations between the gradients of the functions \( \phi(z) \) and \( \psi(w) \) are given by: \( \text{grad} \phi(z) = \text{grad} \psi(w) \cdot f'(z) \). As a consequence, a complicate physical domain where the Poisson differential equation is unknown can be transformed to a model domain with a regular shape where the electric field is constant. The transformation of the physical domain to the model domain described in Figure A5.1 is performed in three steps. First, the polygon in the z-plane is transformed by \( f_1 \) to the upper half of the s-plane by using the Schwartz-Christoffel transformation method. Second, the s-plane is transformed by \( f_2 \) to the s'-plane by using the Möbius transformation method. Third, the upper half of the s'-plane is transformed by \( f_3 \) to the w-plane with the logarithm function. The Schwartz-Christoffel transformation method is described in Ref. [25] and [12].
Figure A5.1: Conform transformation of two angular plates displaced by a distance \( d \).
Table A5.1 defines which corner of the z-plane is transformed to which point on the s-plane and it shows the power \( v \) of the corresponding expression in the transformation rule. Since point 1 will be transformed from a finite value in the z-plane to the infinity in the s-plane no corresponding expression will appear in the transformation rule.

<table>
<thead>
<tr>
<th>Point</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>( z )</td>
<td>0</td>
<td>+( \infty )</td>
<td>( h + id )</td>
<td>+i( \infty )</td>
</tr>
<tr>
<td>( s )</td>
<td>( \infty )</td>
<td>( -a^2 )</td>
<td>( b^2 )</td>
<td>( c^2 )</td>
</tr>
<tr>
<td>( v )</td>
<td>(-1)</td>
<td>( 1/2 )</td>
<td>(-1)</td>
<td></td>
</tr>
</tbody>
</table>

**Table A5.1: Schwartz-Christoffel transformation of polygon corners.**

According to Table A5.1, the Schwartz-Christoffel transformation \( s \to z = f^{-1}_1(s) \) is expressed by

\[
\frac{dz}{ds} = C \frac{\sqrt{s - b^2}}{(s + a^2)(s - c^2)}.
\]  

(Eqn. (A5.1))

Eqn. (A5.1) can be solved by using the substitution \( \zeta(s) = \sqrt{s - b^2} \) and expanding the resulting expression into four partial fractions. The result is

\[
z(s) = C \left\{ \frac{n \ln \left( \frac{\zeta(s) - n}{\zeta(s) + n} \right)}{\zeta(s) + n} - \frac{im \ln \left( \frac{\zeta(s) - im}{\zeta(s) + im} \right)}{\zeta(s) + im} \right\} + C_2,
\]  

(A5.2)

with

\[
m = \sqrt{a^2 + b^2},
\]  

(A5.3)

\[
n = \sqrt{c^2 - b^2}.
\]  

(A5.4)
The parameters $b^2$ and $c^2$ can set to 0 and 1, respectively. With the transformation of the points

$$z(\lim_{\Delta t \to 0} (c^2 - \Delta t)) = h + i\infty,$$  \hspace{1cm} (A5.5)

and

$$z(\lim_{\Delta t \to 0} (c^2 + \Delta t)) = 0 + i\infty,$$  \hspace{1cm} (A5.6)

it results $C_1 = h/(i\pi n)$ and $C_2 = 0$. With $z(b^2) = h + id$ follows $a = d/h$.

The second transformation $s' \to s = f^{-1}_2(s')$ performs only a rearrangement of the points 1 to 4 on the real axes to prepare the last step. This is realized with the Möbius transformation method [23]. The transformation is defined by the three points of Table A5.2.

<table>
<thead>
<tr>
<th>Point</th>
<th>1</th>
<th>2</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>$s$</td>
<td>$\infty$</td>
<td>$-a^2$</td>
<td>$c^2$</td>
</tr>
<tr>
<td>$s'$</td>
<td>1</td>
<td>$\infty$</td>
<td>0</td>
</tr>
</tbody>
</table>

**Table A5.2: Möbius transformation of polygon corners.**

The instruction is

$$s'(s) = \frac{s - c^2}{s - a^2}.$$  \hspace{1cm} (A5.7)

The inverse function of eqn. (A5.7) is given by

$$s(s') = \frac{c^2 + a^2 s'}{1 - s'}.$$  \hspace{1cm} (A5.8)
The last transformation \( w \rightarrow s' = f_3^{-1}(w) \) were the real axis is transformed into two parallel lines can be done with the complex logarithm of the values in the \( s' \)-plane

\[
w = \ln(s').
\]  
(A5.9)

The inverse function is

\[
s' = \exp(w).
\]  
(A5.10)

The complete transformation \( w \rightarrow z \) is thus defined by eqns. (A5.2), (A5.8), and (A5.10). A round edge is achieved by splitting point 3: \( z = h + id \) into \( 3' \): \( z = h + i(d + r) \) and \( 3'' \): \( z = h + r + id \). where \( r \) denotes the curvature radius. The superposition of the transformation rule \( f_1 \) defined by eqn (A5.2) gives a round corner if \( b^2 \) is first replaced by \( b^2 - \Delta b^2 \) and second by \( b^2 + \Delta b^2 \). Thus, the transformation \( s \rightarrow z \) is described by \( z = z_1 + z_2 \). With \( b = 0 \) follows

\[
z_k(s) = C_1 \left\{ n_k \ln \left[ \frac{\zeta_k(s) - n_k}{\zeta_k(s) + n_k} \right] - im_k \ln \left[ \frac{\zeta_k(s) - im_k}{\zeta_k(s) + im_k} \right] \right\} + C_2
\]  
(A5.11)

were \( k = \{1, 2\} \) and

\[
\zeta_1(s) = \sqrt{s + \Delta b^2}, \quad \zeta_2(s) = \sqrt{s - \Delta b^2}, \quad
\]  
(A5.12)

\[
m_1 = \sqrt{a^2 - \Delta b^2}, \quad m_2 = \sqrt{a^2 + \Delta b^2}, \quad
\]  
(A5.13)

\[
n_1 = \sqrt{c^2 + \Delta b^2}, \quad n_2 = \sqrt{c^2 - \Delta b^2}.
\]  
(A5.14)

The displacement \( \Delta b^2 \) in the \( s \)-plane is defined by the curvature radius in the \( z \)-plane

\[
\Delta b \approx \frac{1}{\sqrt{2}} \left( 3\pi \frac{d^2}{h^2 + d^2} \frac{r}{h} \right)^{1/3}.
\]  
(A5.15)
The transformations $f_2$ and $f_3$ are not changing because they are independent of point 3.

The potential distributions and the electrostatic field in the $w$-plane are

\[ \psi(w) = \frac{U_2 - U_1}{\pi} \text{Im}(w), \tag{A5.16} \]

and

\[ F(w) = \frac{U_2 - U_1}{i\pi}, \tag{A5.17} \]

respectively. The corresponding transformed expressions to the $z$-plane are

\[ \phi(f^{-1}(w)) = \frac{U_2 - U_1}{\pi} \text{Im}(w), \tag{A5.18} \]

and

\[ F(f^{-1}(w)) = \frac{U_2 - U_1}{h} \frac{n_1 + n_2}{\zeta_1(w) + \zeta_2(w)} = \frac{U_2 - U_1}{d} \frac{m_1 + m_2}{\zeta_1(w) + \zeta_2(w)}. \tag{A5.19} \]

The maximum field gain appears along the bent floating gate-insulator interface. It is constant along the entire curve and can be calculated with eqn. (A5.19) for $s = 0$. It follows

\[ G = \left( \frac{8}{3\pi} \frac{h^2 + d^2}{r} \right)^{1/3}, \tag{A5.20} \]

and

\[ G = \left( \frac{16}{3\pi} \frac{d}{r} \right)^{1/3} \tag{A5.21} \]

for $h = d$. 

\[ \text{Appendix} \]
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Curriculum Vitae

I was born in Hetzeldorf, Transylvania/Rumania, on August 13, 1962. In Hetzeldorf I attended the German division of elementary school. I attended the first two years of high school (Gymnasium) in Mediasch. After emigrating with my family to Cologne, Germany, in 1979, I finished high school, graduating with the abitur. From 1983 to 1988 I studied at the Swiss Federal Institute of Technology in Zürich where I received the diploma in electrical engineering (Dipl. El.-Ing. ETH). Since 1989 I worked as a research assistant at the reliability laboratory of Prof. Dr. A. Birolini in the field of fault modeling and testing of integrated circuits. During the last two years I concentrated on EPROM reliability.
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