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Strained-Si single-gate versus unstrained-Si double-gate MOSFETs

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Abstract

Self-consistent full-band Monte Carlo simulations are employed to compare the performance of nanoscale strained-Si single-gate (SG) and unstrained-Si double-gate (DG) MOSFETs for a gate length of 25 nm. Almost the same on-current as in the DG-MOSFET can be achieved by strain in a SG-MOSFET for the same gate overdrive. This is due to the compensation of the higher electron sheet density in the two inversion channels of the DG-MOSFET by the higher strain-enhanced velocity in the channel of the SG-MOSFET. The on-current of the strained-Si SG-MOSFET is almost 10% larger for a channel orientation along the crystallographic ⟨100⟩ direction than for the ⟨110⟩ direction. This confirms that the on-current is determined by quasi-ballistic transport, because the maximum enhancement of the in-plane velocity in bulk (001)-strained Si in the ⟨100⟩ direction is 5% at medium electric fields (the low-field mobilities and saturation velocities are the same and the difference in the thermal injection velocities is negligibly small), whereas the transient bulk velocity overshoot peak is 30% larger in the ⟨100⟩ direction.

1. Introduction

As the performance enhancement of silicon microelectronics by scaling of conventional bulk MOSFETs is thought to approach its physical and technological limits, alternative concepts are currently being explored. Double-gate (DG) and strained-Si MOSFETs are considered as the two most promising candidates which may take us to the limit of silicon complementary metal-oxide-semiconductor (CMOS) technology [1, 2] and high performance of such structures has been confirmed experimentally [3, 4]. At the same time, these nanoscale devices are interesting from a physical point of view because their on-state is governed by quasi-ballistic transport which is beyond the classical drift-diffusion (DD) equations. It is the aim of this paper to compare via self-consistent full-band Monte Carlo (FBMC) simulation [5] DG and strained-Si MOSFETs in an extremely scaled prospective structure and to explore the physical mechanisms which influence the on-current in the quasi-ballistic transport regime.

2. Monte Carlo model and device structures

The investigations in this paper are performed using the self-consistent full-band Monte Carlo simulator SPARTA [5]. The band structures are obtained from nonlocal empirical pseudopotential calculations [6] where in addition the spin–orbit interaction has also been taken into account. The scattering mechanisms comprise three f-type and three g-type intervalley phonon processes with exactly the same coupling constants as used by Jacoboni and Reggiani [7], intravalley phonon scattering, impact ionization, a calibrated Ridley model for impurity scattering and surface roughness scattering consisting of a combination of specular and diffusive scattering [8] with a percentage of 15% diffusive scattering. The biaxial tensile strain caused by the lattice mismatch between a silicon layer and a SiGe substrate shifts four of the six valleys upwards in energy leading to a smaller in-plane conductivity mass and reduced intervalley scattering. Experiments [9] and theoretical works [10–13] report a strongly improved bulk low-field mobility in strained Si and also measurements [4] as well as Monte Carlo simulations [14] of nanoscale bulk n-MOSFETs find a pronounced enhancement of the on-current under strain.

The unstrained-Si DG MOSFET has a gate length of $L_G = 25$ nm, a film thickness of $t_{Si} = 6.25$ nm, an oxide thickness of t_{ox}=1 nm and a tungsten metal gate. The doping level in the source/drain regions is 10^{20} cm^{-3} and falls off into the undoped channel by 2.5 nm dec^{-1}. In the single-gate

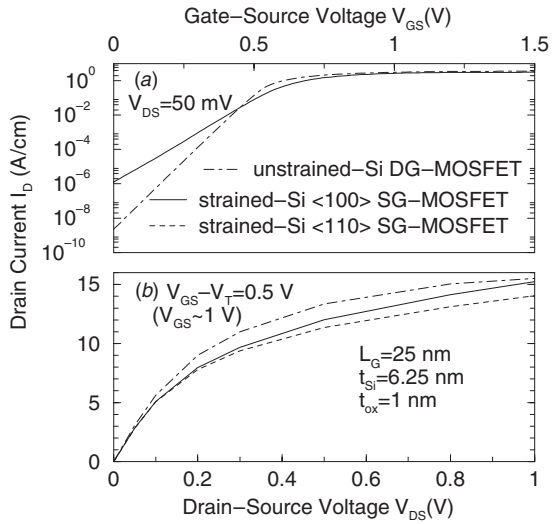

Figure 1. Transfer characteristics according to the DD model (*a*) and output characteristics computed by FBMC simulation (*b*) of an unstrained-Si DG-MOSFET and a strained-Si SG-MOSFET with a channel oriented along the crystallographic in-plane ⟨110⟩ or ⟨100⟩ direction. Note that there is no difference between the ⟨110⟩ and the ⟨100⟩ directions in the strained-Si transfer characteristics at $V_{DS} = 50$ mV (*a*), because the anisotropy only appears at higher drain voltages (see (*b*)).

(SG) strained-Si SiGe-on-insulator (strained-SOI) structure, the silicon channel is grown on a 100 nm p-doped relaxed SiGe buffer layer which is on top of a 50 nm buried oxide. Such a structure can be obtained by the combination of separation-by-implanted-oxygen (SIMOX) technology with a Si regrowth technique found suitable for device fabrication [15]. The germanium content of the relaxed SiGe buffer is 40% in this simulation study.

3. Simulation results

Figure 1(*a*) shows the transfer characteristics where the Ge content and the doping level in the SiGe buffer were adjusted to yield, similar to the DG MOSFET, a threshold voltage of about $V_T \sim 0.5$ V. The off-current in the strained-Si MOSFET is about three orders of magnitude larger than in the DG MOSFET, but the value of 0.1 nA μm^{-1} is still very small and appropriate for high-speed applications. The output characteristics in figure 1(*b*), computed for the same gate overdrive of $V_{GS} - V_T = 0.5$ V, demonstrate that almost the same on-current I_{on} as in the DG MOSFET can be achieved by strain in a SG MOSFET. The reason can be deduced from figure 2 where the profiles of sheet density and drift velocity are displayed: the higher charge density of the two inversion channels in the DG MOSFET is compensated by a higher drift velocity in strained Si.

The physically striking effect is that I_{on} of the strained-Si MOSFET is almost 10% larger for a ⟨100⟩ than for a ⟨110⟩ orientation of the channel in view of equal low-field mobilities μ_{low} and saturation velocities for both directions with a maximum enhancement in the ⟨100⟩ direction of 5% at 25 kV cm^{-1} (and negligible differences in the thermal injection velocities v_{inj}). This direction dependence of I_{on} in strained Si is similar to that found in nanoscale bulk n-MOSFETs in

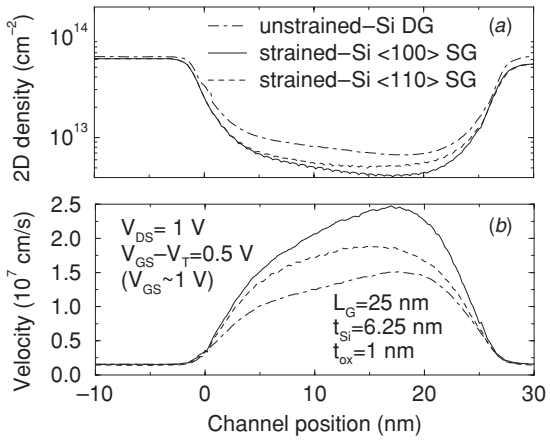

Figure 2. Profiles along the channel of (*a*) the sheet density obtained by integration of the electron density perpendicular to the Si/SiO_2 interface over the silicon film thickness t_{Si} and (*b*) the drift velocity, averaged perpendicularly to the interface with the electron density, in the on-state of the three device configurations of figure 1.

[14] where also the bulk simulation results for strained and unstrained Si are shown. This confirms that (i) quasi-ballistic transport determines I_{on}, since the transient bulk overshoot peak is 30% larger for the ⟨100⟩ direction in strained Si because of a stronger band curvature above 100 meV [16], and (ii) widely used models ascribing I_{on} to v_{inj} and μ_{low}-dependent backscattering [17] fail to describe the anisotropy of I_{on} in strained Si. The increasing contribution of quasi-ballistic transport to I_{on} in strained Si is also the explanation why strain still improves I_{on} for decreasing gate lengths. The apparent discrepancy as pointed out in [18] was that smaller gate lengths involve higher longitudinal electric fields, but that the on-current is still improved by strain in nanoscale MOSFETs [4] despite a vanishing strain-induced velocity enhancement in the high-field limit. However, the electrons are subject to quasi-ballistic overshoot effects when experiencing a strong field upon entering the source side of the channel and these overshoot effects are stronger in strained Si. This can also be seen in figure 2(*b*) which shows that the electrons travel in strained Si almost immediately after entering the channel with a velocity above the saturation velocity (see also [14] for a more comprehensive discussion).

In conclusion, our simulation study shows a similar high potential of both DG and strained-Si MOSFETs for the nanoscale regime. To decide which of the two approaches is to be preferred will require more detailed investigations considering also, e.g., restrictions on I_{off} or fabrication-related issues.

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