Self-heating analysis of monolithically integrated hybrid III-V/Si PIN diode

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ABSTRACT

Self-heating is a crucial effect in integrated nanophotonic devices regarding their power consumption. In this work, we employ coupled 3D thermo-electrical simulations to gain insight into the thermal behavior related to traps in a monolithic InP-InGaAs-InP pin-diode fabricated at IBM-Research Zurich. From transport study, two types of defects are found to be very likely present in the studied device: (i) positive oxide charges close to the interface between III-V materials and top oxide layer and (ii) electron-type traps at the p-InP/i-InGaAs interface. Thermal simulations show that the presence of electron-type traps at the p/i interface enhances the self-heating in the device.

Keywords: monolithically integrated pin-diode, self-heating, defects

1. INTRODUCTION

Energy-efficient photonic integrated circuits (PICs) are highly desirable for many future applications, such as optical interconnects[1;2] and quantum information processing[3;4;5]. However, their fabrication with sufficiently good material quality and device performance still remains challenging, especially for hybrid integration across different platforms. The template-assisted selective epitaxy (TASE) method[6] invented by IBM-Research Zurich could be one promising solution to overcome this problem. It allows the growth of high-quality III-V materials directly on silicon by making use of silicon dioxide as template, which enables the nanoscale integration of devices for photon emission, manipulation, and detection on a single platform. To enable applications with low-power consumption, understanding of the self-heating effects in the fabricated devices becomes essential, especially for forward-biased pin-diodes operating as photon sources. For this purpose, we utilize coupled 3D thermo-electrical simulations with *Sentaurus-Device* to analyze the measured thermal performance of one of the fabricated T-shape InP-InGaAs-InP pin-diodes[7]. In the following, the device structure and simulation methodology are briefly described at first. Then in the next sections, we will discuss the simulation results for electrical transport and thermal study in detail, showing the necessity to include material non-idealities and to analyze their impact on current flow and self-heating in the studied device.

Details of the device structure are shown in Fig. 1, where the top oxide layer and the Si seed region next to n^+-InP exist due to the TASE growth process. The p^+-InGaAs region is designed for a better p-type Ohmic contact, since in general a high Schottky barrier forms at the Au/p-InP interface[8;9]. The i-InGaAs region is assumed to be slightly n-doped with a concentration of 1e16 cm^{-3}. The doping concentrations of the other regions with the same unit are shown in the left bottom corner of Fig. 1. In order to understand the self-heating effect in the device, we run two-fold simulations. First, electrical simulations based on the drift-diffusion formalisms are performed to identify the physically relevant mechanisms of carrier transport. They are validated by reproducing the measured current under both reverse and forward bias. Given all transport-related mechanisms, we employ coupled thermo-electrical simulations based on the *thermodynamic* model to investigate the thermal impact of electron-type traps at the p/i interface, as the presence of such traps is of relevance in many III-V photonic devices.

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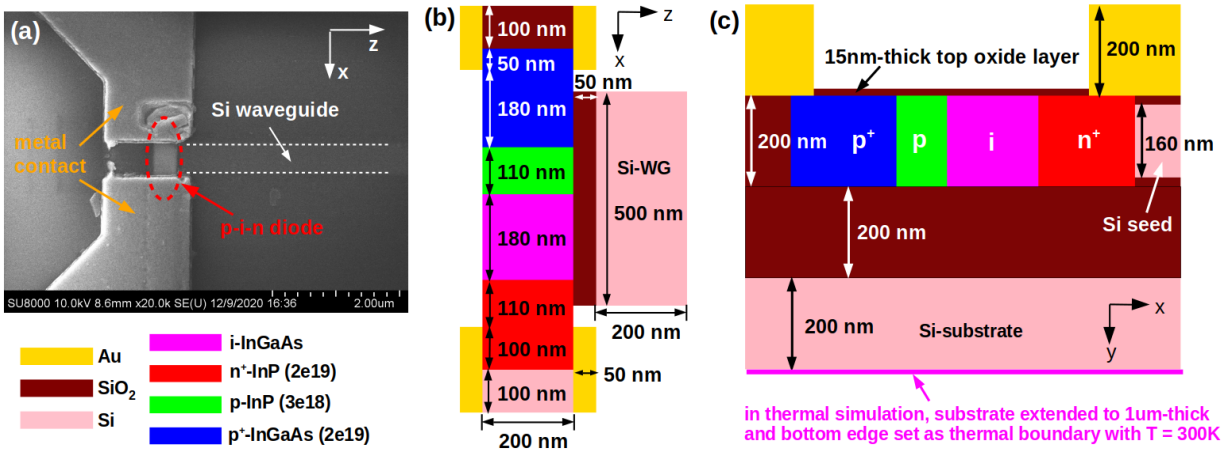

Figure 1. (a) Top view SEM picture of the fabricated T-shape p-i-n diode. Sketch of (b) top and (c) side view of the simulated device. The thickness of the Si substrate is set to 200 nm (1 μm) in the electrical transport (thermal) study.

To clarify the required material parameters for the thermal study and its simulation outputs used in later discussions, here we briefly describe the *thermodynamic* model provided in *Sentaurus-Device*. Further details are given in Ref. [10]. In this model the stationary heat transfer equation

$$-\nabla\cdot(\kappa\nabla T) = -\nabla\cdot\left[(P_nT+\Phi_n)\vec{J}_n + (P_pT+\Phi_p)\vec{J}_p\right] \tag{1}$$

is solved with user-defined thermal boundary conditions. The subindex n (p) is used to label the physical quantities related to electrons (holes). It is assumed that the charge carriers are in thermal equilibrium with the lattice, and thus their temperature can be represented by a single quantity T. Regarding material parameters, κ is the thermal conductivity and P is the thermo-electric power (also known as Seebeck coefficient). The right-hand side in Eq. (1) represents the total heat generation rate, where the current densities are given by

$$\vec{J}_n = -nq\mu_n(P_n\nabla T + \nabla\Phi_n)\,,\ \vec{J}_p = -pq\mu_p(P_p\nabla T + \nabla\Phi_p)\,, \tag{2}$$

containing both the gradients of electrostatic potential (Φ) and temperature, which together drive the electrical current. The elementary charge is represented by q, while n *(p)* is the electron (hole) density. By combining the above equations with the continuity equations

$$\nabla\vec{J}_n = q(R_{net,n} - G_{net,n})\,,\ -\nabla\vec{J}_p = q(R_{net,p} - G_{net,p})\,, \tag{3}$$

the total heat generation can be separated into heating source terms related to different mechanisms, namely Joule heat, recombination heat, and Thomson heat. The quantity R *(G)* above represents the carrier recombination (generation) rate. These terms together with the temperature profile can be obtained from the thermo-electrical simulation outputs, which enables us to compare the contributions from individual heat sources and to find the dominant mechanism (see discussion in Sec. 3). For material-related thermal parameters, except for III-Vs, the default values in *Sentaurus-Device* are used. For III-Vs the values are taken from Refs. [11-13], with thermo-electric power computed from the analytic model in Ref. [10] and tuned by fitting parameters. The choice of the thermal boundary condition is described in Fig. 1 (c).

2. STUDY OF ELECTRICAL TRANSPORT

Information about physical mechanisms related to carrier transport in an electronic device is encoded in its IV-characteristics, which can be extracted by reproducing the measurement by means of transport simulations. To do so, we start from an ideal case, where only Schockly-Read-Hall (SRH) recombination is considered in the p-i-n diode, with electron and hole lifetimes set to 1 ns for all III-V materials. Then we perform trial

simulations including additional mechanisms that probably exist in the studied device until a good match with the measurement is obtained. Choices of these additional mechanisms are made based on the following. First, we consider the well recognized basic physical processes in a p-i-n diode, like direct band-to-band tunneling (BTBT) relevant under high reverse bias [14;15]. Then, some commonly known material non-idealities that could exist given the studied device structure are also taken into account. Based on this procedure, we find that the experimental data can be fairly reproduced if four types of mechanisms/non-idealities are included additionally on top of the ideal case simulation (see Fig. 2 (a)). These are direct BTBT, positive oxide charges at the interface between top oxide layer and III-Vs with a concentration of 1.2e13 cm^{-2}, electron-type traps at the p-InP/i-InGaAs interface with trap concentration (energy level) of 5e11 cm^{-2} (at 0.28 eV below conduction band edge) [16] and p-contact resistance with a value of 4e-4 Ωcm^2 [17]. The measurement results are labeled by blue dots in Fig. 2 (a), and the plotted curves are the trial simulation results obtained from including different combinations of additional mechanisms, showing how to reproduce the experimental data step by step. The dashed black curve is the simulated ideal IV-curve, where the current under reverse bias is more than six orders of magnitude below the experimental data. It indicates that there must be additional mechanisms related to transport. The red solid curve represents the best-matching result compared with the experiment, with all four mechanisms above considered in the simulation.

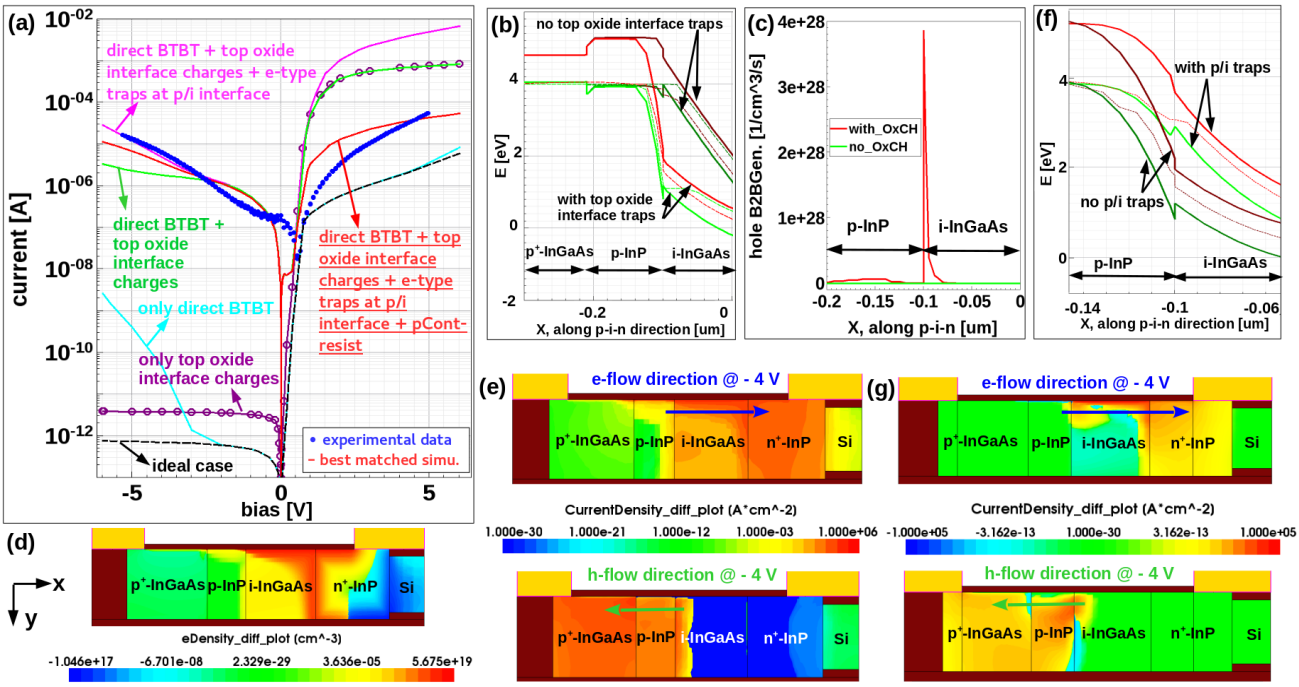

Figure 2. (a) Simulated and measured IV-curves of the studied device. (b)/(c) Comparison of band diagrams/hole band-to-band generation rate profiles at -4 V between simulated ideal case and the case with only top oxide interface charges included near the p/i interface, obtained from a line cut along the p-i-n direction at 100 nm below top oxide layer. (d) Difference in electron density at -4 V between the case with only top oxide interface charges included and the ideal case, extracted by subtracting the latter from the former. The plot is obtained from a central cut plane along the p-i-n direction. (e) Difference in electron and hole (upper and lower plot) current density at -4 V between the case with both top oxide interface charges and direct BTBT included and the ideal case, using the same extraction and plot procedure as in (d). Arrows label the carrier flow directions. (f) Comparison of band diagrams at -4 V between simulated cases with and without e-type p/i interface traps, obtained at the same location as in (b). (g) Difference in electron and hole (upper and lower plot) current density at -4 V between cases with and without e-type p/i interface traps, obtained using the same procedure as before.

By comparing these trial simulations with the ideal case and the measurement, the impact of an individual mechanism on transport can be figured out. First, direct BTBT increases the current at high reverse bias, as

seen from the comparison between black dashed curve (ideal case) and cyan solid curve (only direct BTBT included) in Fig. 2 (a). This is because strong band-to-band generation requires a high electric field (E-field), which in an ideal diode (i.e. without any additional alteration of the electrostatics) is only possible by increasing the reverse bias. Secondly, a reasonable amount of positive top oxide charges near its interface with the III-Vs *alone* can only slightly raise the overall current level, as seen by comparison of black dashed curve (ideal case) and labeled purple solid curve (only top oxide interface charges included) in Fig. 2 (a). However, when combining both effects, the reverse current becomes orders of magnitude higher than in the ideal case (compare black dashed and green solid curve in Fig. 2 (a)), reaching the measured reverse current level. This can be understood qualitatively by inspecting the current density of both types of carriers. In the presence of positive top oxide interface charges, more electrons are induced in the i-InGaAs and n^+-InP region as shown in Fig. 2 (d). The result is a higher electron current density (see the upper plot in Fig. 2 (e)), but also a down-shift of the band edges in the i-region accompanied by a stronger band bending at the p/i junction, as shown in Fig. 2 (b). The steepening of the band edges (much larger E-field) results in a higher BTBT current (see comparison in Fig. 2 (c)). Consequently, the hole current density under reverse bias also becomes larger compared with the ideal case, as seen from the lower plot in Fig. 2 (e). Thus, the main effect of the positive top oxide interface charges is an electrostatic amplification of the BTBT rate. Thirdly, electron-type traps at the p-InP/i-InGaAs interface cause a slight increase of the current at high reverse bias (see comparison between green and magenta solid curve in Fig. 2 (a)). Hence, the shape of the simulated IV-curve is tuned, becoming more similar to the measured one. The small current boost is related to the up-lifted band edges near the p/i interface in the presence of e-type traps. As shown in Fig. 2 (f), a stronger band bending and thus a larger E-field in the i-InGaAs region are the consequences, as well as a lowering of the valance band offset barrier for holes. Both, the electron and hole current at reverse bias increase (see Fig. 2 (g)). Lastly, the p-contact resistance simply suppresses the current at forward bias, which is absolutely relevant in reality and needed here to reproduce the measurement.

3. ANALYSIS OF SELF-HEATING EFFECT

In this section, we study the thermal impact of the considered e-type traps at the p-InP/i-InGaAs interface in this device. It is found by comparing the simulation results of two cases: (i) with all transport-related mechanisms included; (ii) only these traps are excluded. The result is shown in Fig. 3 (a), which indicates that the presence of e-type traps at the p/i interface heats up the device. The corresponding line plots of the temperature along the p-i-n direction are given in Fig. 3 (b). As seen from the comparison of solid red and green curves, if these traps do not exist, the original hot spot disappears and the device is generally cooler due to a much reduced total heat generation. The physics behind these observations is explained in the following. The e-type traps at the p-InP/i-InGaAs interface can be occupied by electrons supplied from the n-side under the high forward bias and thus carry a negative charge. This shifts the band edges near the p/i interface down (see Fig. 3 (c)). Therefore, when removing these traps, the band edges in the p-regions are lifted up, leading to a high conduction band barrier for electron injection from the i-InGaAs region (see dark red and green curves in Fig. 3 (c)). The electron current flow into the p-regions under froward bias is blocked (see comparison in Fig. 3 (d)), and the electron density becomes very low there (see Fig. 3 (e)). A low electron density, however, means that instead of the original strong recombination that dominates the heat generation, now carrier generation occurs in these regions (see Fig. 3 (f)) and leads to a thermal cooling in most parts as seen in Fig. 3 (g). This explains the observed overall lower device temperature when excluding e-type p/i interface traps.

4. CONCLUSION

We investigated the transport and self-heating behavior of a monolithic InP-InGaAs-InP pin-diode integrated on a silicon platform. From the transport study we found that a reasonable amount of positive charges at the III-V/top oxide interfaces and electron traps at the p-InP/i-InGaAs interface must be assumed to reproduce the measured IV-characteristics. The top oxide interface charges have a strong electrostatic impact and lead to an overall orders-of-magnitude increase of the current under reverse bias facilitated by direct BTBT, while the presence of p/i interface traps changes the shape of the IV-curve by slightly raising the current at high reverse bias. From the thermal analysis it turned out that e-type traps at the p/i interface rather enhance the device self-heating, which is related to the fact that they ease the electron current injection into the p-doped

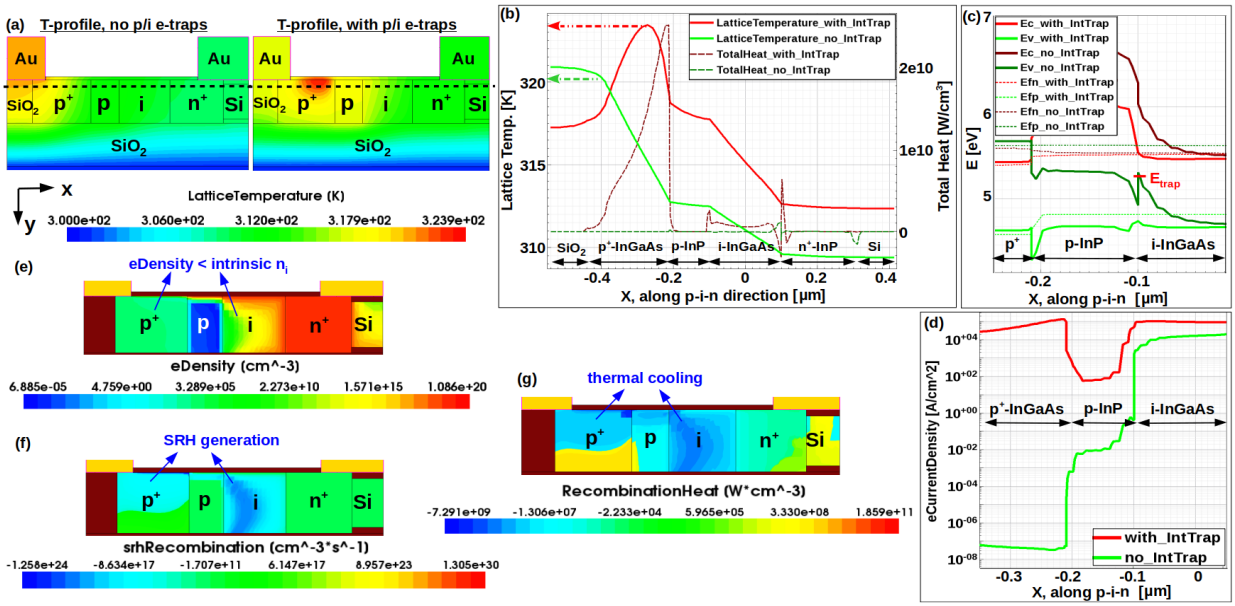

Figure 3. (a) Side view of simulated T-profile at +5.5 V, comparing without and with e-type p/i interface traps. Corresponding comparison of simulated (b) temperature and total heat generation rate profile, (c) band diagram and (d) electron current density along p-i-n, obtained from cutting along black dashed line in (a). Plot of (e) electron density, (f) SRH generation rate and (g) heat recombination rate profile in case of excluding e-type p/i interface traps, obtained from the same cut position as for (a). A negative value in (g) represents thermal cooling.

regions under high forward bias. This gives a clue to the possible physical origins of self-heating in other types of nanoscale III-V p-i-n photonic devices in view of the common relevance of such traps. Our work is helpful to improve fabrication technology and future device design.

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