# Three-dimensional Quantum Simulation of Silicon Nanowires

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## INTRODUCTION

Silicon nanowires are perspective core components of future integrated circuits. The feasibility of Si nanowire FETs has been demonstrated by several groups, e.g. by Cui et al. [1]. TCAD-oriented simulation tools can accompany the sophisticated fabrication process, providing aid for performance improvement, supporting the basic understanding, and facilitating the development of new structures. Nanowire FETs with small cross sections and ultra-short gates call for a three-dimensional (3D) quantum mechanical treatment of carrier transport beyond the effective mass approximation (EMA). As long as inelastic scattering is neglected, a Wave Function approach is the method of choice due to its numerical advantage over the Non-Equilibrium Green's Function (NEGF) technique [2]. However, the computational burden does not allow to treat important effects like phonon scattering and gate tunneling on a full-band (FB) level. These phenomena still require the EMA. In this paper, we describe a FB quantum transport simulator and show FB and EMA simulation results for quantum-ballistic currents in Si nanowire FETs. We focus on the effects of channel orientation, surface roughness, and direct gate tunneling leakage.

## SIMULATION METHODS

The FB 3D Schrödinger-Poisson solver is based on the nearest-neighbor $sp^3d^5s^*$ semi-empirical tight-binding (TB) method[3]. Current and carrier densities are obtained by calculating the device wave function with open boundary conditions (OBC) at different injection energies[2]. The OBCs are calculated with an improved scattering-boundary approach which significantly reduces the computational burden associated with established methods that take the form of a generalized eigenvalue problem or require iterative solvers. The Poisson equation is solved self-consistently on a finite element grid with atoms occupying node positions only. For the simulation of gate leakage the EMA is used everywhere in the device[4]. FB calculations would require a proper atomistic description of the oxide layers and of the gate materials. Compared to the recursive NEGF approach [5] all the injection contributions coming from the different gate contacts are included in the solution of the Schrödinger equation. The 3D gate tunneling approach allows to cover the important effect of electron wave diffraction at the gate edges.

## RESULTS

A typical nanowire structure is shown in Fig. 1 and explained in the caption. In the lower part, the cross sections corresponding to transport along the (a) [100], (b) [110], (c) [111], and (d) [112] crystal axis are given. Black dots represent Si atoms, while lines model atomic bonds. The transmission through the conduction and the valence bands of infinite Si nanowires with the same size as in Fig. 1 are plotted in Fig. 2 for the [100] and [110] orientations. In the energy range significant for charge and current density calculations ($\approx$150 meV from the band edge) the curves with and without spin-orbit coupling are almost identical, except for the valence band of the [100] nanowire. Hence, the FB transfer characteristics in Fig. 3 were calculated without spin-orbit coupling. The gate metal work functions were set to $\phi_m$ = 4.15 eV for n-FETs and $\phi_m$ = 5.0 eV for p-FETS (not adjusted for the same off-current). The [110] orientation offers the highest on-current both for the n-FET and the p-FET. Interface roughness was generated by randomly distributing the atoms at the Si-$SiO_2$ interface according to an exponential autocovariance function. The threshold voltage variations for the [100] and [110] orientations are shown in Fig. 4. Finally, Fig. 5 presents gate tunneling currents of a $3\times3\,nm^2$ Si nanowire with high-K stack layers.

## ACKNOWLEDGMENT

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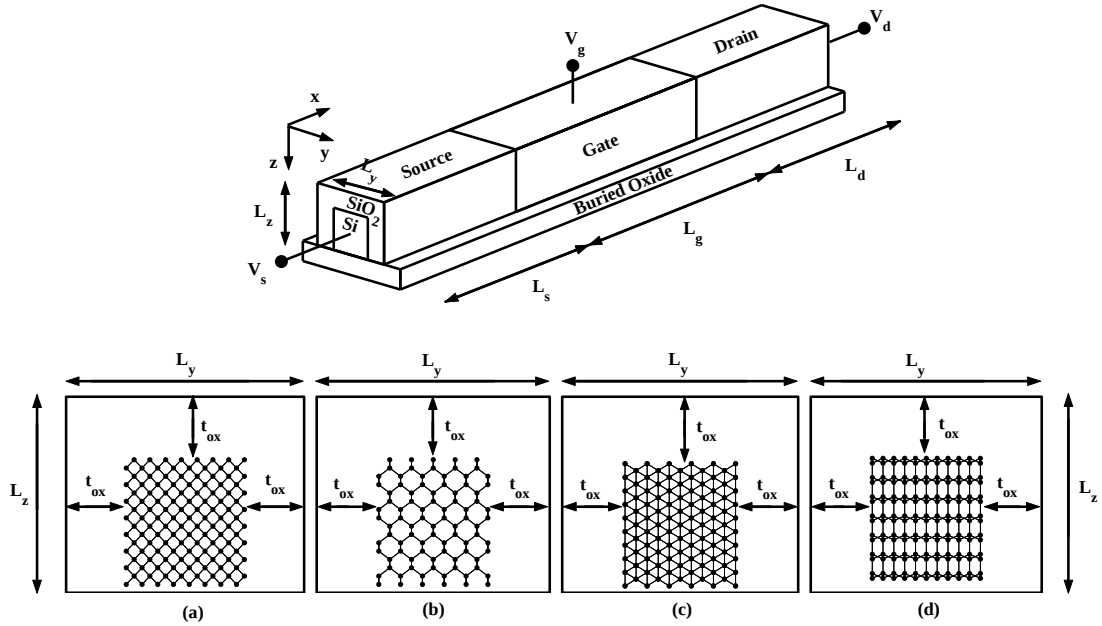


Fig. 1. Triple-gate nanowire transistor with a $2.1\times2.1\,\mathrm{nm}^2$ Si channel deposed on a buried oxide and surrounded by three oxide layers of thickness $t_{\mathrm{ox}}$ = 1 nm. The source and drain regions have a length of $L_{\mathrm{s}}$ = $L_{\mathrm{d}}$ = 9.7 nm, the gate of $L_{\mathrm{g}}$ = 13 nm. Along the transport direction $x$ the wire is composed of 60 slabs for $x$=[100] (a), 88 slabs for $x$ = [110] (b), 34 slabs for $x$ = [111] (c), and 49 slabs for $x$ = [112] (d). Each type of slab contains a different number of atomic layers. The projection of the slab atoms onto the cross section plane is shown in the lower part.

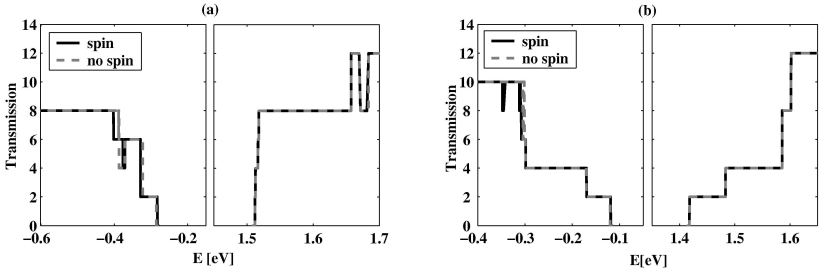


Fig. 2. Transmission through $2.1\times2.1\,\mathrm{nm}^2$ infinite nanowires with $x$ aligned with (a) [100] and (b) [110]. Calculations are shown for the conduction and the valence subbands with spin-orbit coupling (black solid lines) and without (gray dashed lines, curves multiplied by a factor 2).

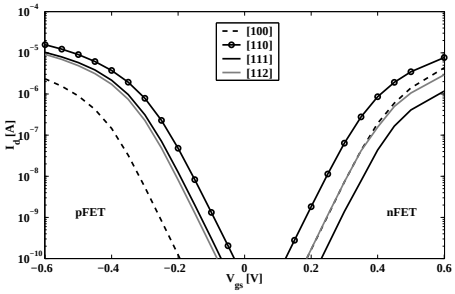


Fig. 3. FB transfer characteristics for $L_{\mathrm{g}}$ = 13 nm. Left: $I_{\mathrm{d}} - V_{\mathrm{gs}}$ ($V_{\mathrm{ds}}$=-0.4 V) of p-FETs with transport directions along [100] (dashed line), [110] (solid line with circles), [111] (black line), and [112] (gray line). Right: n-FET curves for $V_{\mathrm{ds}}$ = 0.4 V.

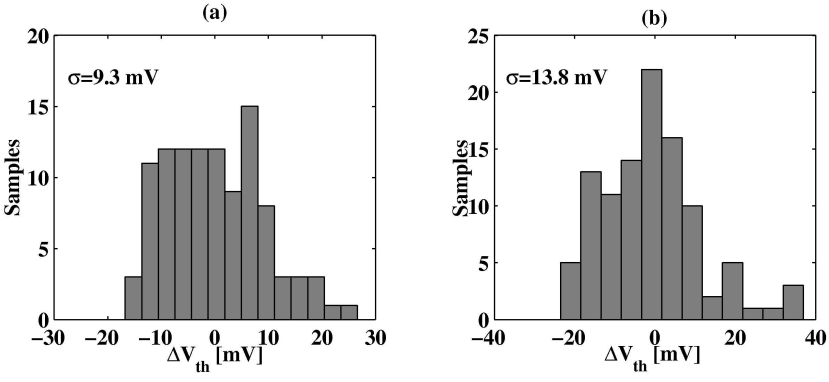


Fig. 4. Histogram distribution of 105 samples representing the threshold voltage variation caused by interface roughness. The results for (a) the [110] and (b) the [100] Si nanowire transistors are plotted. $\sigma$ is the standard deviation of $\Delta V_{\mathrm{th}}$.

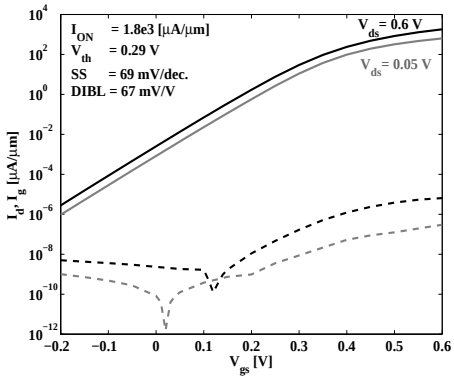


Fig. 5. $I_{\mathrm{d}} - V_{\mathrm{gs}}$ and $I_{\mathrm{g}} - V_{\mathrm{gs}}$ characteristics of a $3\times3\,\mathrm{nm}^2$ nanowire with TiN gates and stack layers of 0.5 nm $SiO_2$ and 3.25 nm $HfO_2$.