A Generalizable TCAD Framework for Silicon FinFET Spin Qubit Devices with Electrical Control

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***Abstract*—We present a TCAD-based simulation framework established for quantum dot spin qubits with full-electrical control implemented on a silicon FinFET platform. It works down to 1 K and consists of a two-step simulation chain, from qubit initialization with DC bias to state manipulation using microwave signals. After calculating the microwave electric field response at the qubit locations, an average field polarization vector at each quantum dot is provided for further estimation of the Rabi coupling strength. We demonstrate the functionality via simulation of a recently reported two-qubit device in form of a 5-gate silicon FinFET. The framework is easily generalizable to future multi-qubit systems.**

I. Introduction

Scalability is vital for quantum computing, but a tough task from the aspect of physical implementations. One promising platform to overcome this challenge is given by quantum dot (QD) spin qubits embedded in multi-gate silicon FinFETs, which can be fabricated using standard CMOS technology. Recently, hole spin qubits hosted by double QDs in a 5-gate silicon FinFET that can operate above 4 K have been reported in [1] [2]. To scale up the system in the near future, a simulation-aided analysis for the design of full-electrical control is highly desirable, especially for the qubit state manipulation with microwave (MW) signals. For this purpose, we developed a TCAD-based framework operable down to 1 K which enables simulations of qubit state initialization with DC bias and manipulation by MW control signals. The MW response electric field (E-field) polarization vector averaged over each QD is extracted in post-processing steps, allowing for the further analysis such as Rabi frequency estimation. The cross-talk between multiple gates is also taken into account in the MW simulations via a 1st. order capacitive coupling model.

We illustrate the simulation framework by taking the example of the two-hole-qubit device reported in Ref. [1], but the generalization to multi-qubit devices (either electron or hole spin based) and the extension to include more functionalities like cross-talk between qubits and readout bus-line in a larger system are straightforward. The simulated device structure adapted from the fabricated one [1] is shown in Fig. 1. In the following, we first introduce the MW simulation method including the cross-talk estimation model. Then, MW simulation results for two qubits each hosted in a one-hole QD are presented to clarify how the average response field polarization vector at a given QD is extracted. Finally , as an application example, we demonstrate the impact of the numbers of holes in a QD on the response field polarization vector.

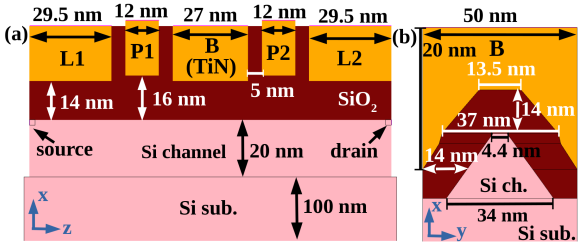


Fig. 1. Sketch of simulated 5-gate Si FinFET. (a) side view along fin direction, (b) cross section view perpendicular to fin direction under gate B.

II. Simulation Methodology

Modeling the MW field response in spin qubit devices has two special aspects. First, the charge distribution in the QDs is coupled self-consistently with the field response. Secondly, the device size (usually a few hundreds of nm) is much smaller than the wavelength of the applied MW signal (cm range). Therefore, commonly used techniques for MW simulation (like FDTD) are not proper options because of their high computational cost and the lack of self-consistency with the charge distribution. On the other hand, electrical small signal AC analysis fits well for this application, as long as the amplitude of the MW signal is much smaller than the applied DC bias. In S-Device, this technique proceeds by adding a small harmonic term to the original DC variable, i.e.

$$\xi_{total} = \xi_{DC} + \Delta\xi e^{iwt} \tag{1}$$

where ξ denotes potential (ϕ) or carrier density (n, p). The AC system containing the new variables is then solved in 1st-order of $\Delta\xi$ [3]. To calculate the response field, a two-step simulation is required. First, we run a quasi-stationary DC simulation (at T = 1 K) to generate QDs with a specific number of holes. The important effect of confinement in the fin tip is taken into account by the density gradient model [3]. Then, the electrical small-signal analysis is performed by ramping the AC voltage at gate P1. Since the MW field response that we are interested in is not a default output in S-Device, it needs to be extracted based on the following relations:

$$E = -\nabla\varphi \tag{2}$$

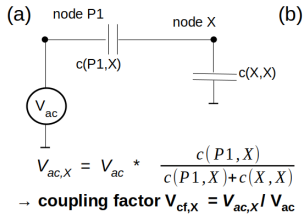
$$J_D = -i\omega\epsilon\nabla\varphi \tag{3}$$

$$\Re(E) = \Im(J_D)/\omega\epsilon \tag{4}$$

According to Eq. (4), the imaginary part of the displacement current response $\Im(J_D)$ (default output in S-Device)

is representative for the real E-field response $\Re(E)$. Their magnitudes differ only by a (computable) scaling factor, whereas the vector directions are exactly the same. This one-to-one correspondence facilitates the calculation of a response field polarization vector at each qubit location. Details will be discussed in Sec. III.

To take the cross talk between gates into account, we introduce a simplified capacitive coupling model based on the 1st-order estimation. This is achieved by running two-fold AC simulations. A first round is performed with the AC signal applied on gate P1 only, in order to extract the equivalent Y-matrix of the device. The obtained capacitance elements are then used to construct the simple voltage divider circuit model (see Fig. 2 (a)). The capacitive coupling factor $V_{cf,X}$ between P1 and any other gate (labeled as node X) can be calculated. Then, a second-round simulation is performed with AC signals also applied to all other gates, where their AC voltage amplitudes depend on the coupling factor $V_{cf,X}$. For example, Fig. 2 (b) shows the results of the coupling factors in case of one hole in each QD. The final field response is obtained after the second AC run including the gate cross talk.



(b) Gate coupling calculation for 1/1 hole @ QD1/2

Gate node X	cross cap. c(P1,X) [aF]	self cap. c(X,X) [aF]	$V_{cf,X}$ [1]
L1	11.050	15.707	**0.413**
B	10.882	26.920	**0.288**
P2	8.125e-4	24.237	3.352e-5
L2	5.341e-5	15.751	3.391e-6

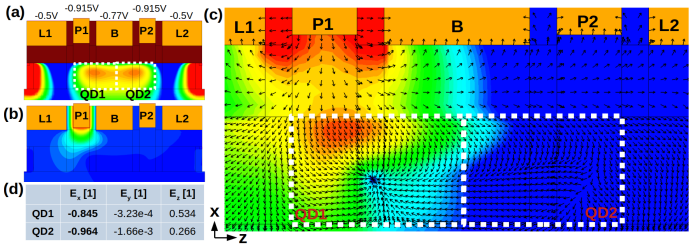
Fig. 2. (a) Simplified 1st-order capacitive coupling circuit model for gate cross talk calculation. (b) Calculated voltage coupling factor for case of two one-hole QDs. The coupling is strong only for gates L1 and B that are close to the AC control gate P1 as expected.

III. Simulation Results

We first present the MW simulation results for a basic two-qubit case, with each qubit hosted at a one-hole QD. Then, we discuss the impact of the number of holes in QD1 on the field response.

A. Two-Qubit Case with One-Hole QDs

First, we run DC simulation for qubit state initialization, with gate biases set to values adapted from the experiment. The obtained hole density profile (see Fig. 3 (a)) shows the formation of two one-hole QDs. The resultant real part of the potential response is plotted in Fig. 3 (b), where its gradient relates to the response field we are interested in. Since this response is the lowest in the region with the highest hole density, a response singularity appears at the center of each QD (see regions labeled by white dashed lines in Fig. 3 (c)). The presence of such singularities makes it hard to directly assign a single field vector to a particular QD. Thus, we introduce a normalized field vector averaged over the QD volume. It is calculated by integrating each component of the field vector over the dot volume and dividing by the root sum square (i.e. normalizing by the volume integral of the field magnitude). The results are shown in Fig. 3 (d).



	E_x [1]	E_y [1]	E_z [1]
QD1	**-0.845**	-3.23e-4	0.534
QD2	**-0.964**	-1.66e-3	0.266

Fig. 3. (a) DC hole density profile in fin direction with 1/1 hole at QD1/2. Applied DC biases are labeled on top of the corresponding gates. White dashed lines indicate the QD volume used for integration to obtain the number of holes. Corresponding (b) normalized real part of the potential and (c) imaginary part of the displacement current response, taken at V_{ac} = -12 mV. (d) Calculated components of the averaged response field vector at QDs. Color bar ranges from 1e14 to 1e18 cm^{-3} in (a), 0 (blue) to 1 (red) in (b), and from 1e2 (blue) to 1e4 (red) $Acm^{-2}V^{-1}$ in (c).

B. Impact of Number of Holes at QDs

Using the method above, we study the impact of the number of holes at QD1 on the response field, as this number can be hard to determine experimentally. Results for two cases, 3/3 and 5/3 holes at QD1/2, are shown in Fig. 4. Although the dominant field polarization in both QDs remains unchanged with more holes in QD1, the field vector at QD1/2 tends to have a stronger x/z-component and a weaker z/x-component. For QD1, this is because the increased charge there distributes the field response more homogeneously along z (see colormap comparison under P1). Consequently, the z-component of the field contributes less over the integrated dot volume. For QD2, the slightly larger z-component comes from the increased electrostatic impact along z due to more holes at QD1.

(a) 3/3 holes @ QD1/2

	E_x [1]	E_y [1]	E_z [1]
QD1	**-0.956**	-3.97e-4	0.292
QD2	**-0.836**	-1.67e-3	0.549

(b) 5/3 holes @ QD1/2

	E_x [1]	E_y [1]	E_z [1]
QD1	**-0.984**	-3.12e-4	0.180
QD2	**-0.827**	-1.69e-3	0.563

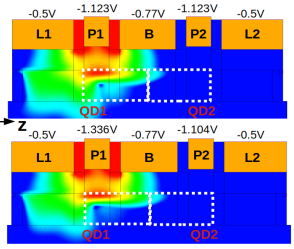


Fig. 4. Simulated field response for case (a) 3/3 and (b) 5/3 holes in QD1/2. Tables contain the components of the average response field vector. Field response magnitudes are plotted on the right. White dashed lines indicate the dot volume used for integration. Color bar range is kept the same as in Fig. 3 (c). Numbers on top of the gates indicate the corresponding DC biases to obtain 3/3 and 5/3 holes under QD1/2.

IV. Conclusion

A TCAD simulation framework developed for future large-scale silicon FinFET spin qubit devices allows to calculate the average MW E-field response vector at each QD. A reported two-qubit device is analyzed, showing that the MW response field polarization is very sensitive to the number of holes in the QD under the AC gate used for qubit control.

References

[1] S. Geyer, L. C. Camenzind, L. Czornomaz, V. Deshpande, A. Fuhrer, R. J. Warburton, D. M. Zumbühl, and A. V. Kuhlmann, "Self-aligned gates for scalable silicon quantum computing," *Applied Physics Letters*, vol. 118, no. 10, p. 104004, 2021.

[2] L. C. Camenzind, S. Geyer, A. Fuhrer, R. J. Warburton, D. M. Zumbühl, and A. V. Kuhlmann, "A hole spin qubit in a fin field-effect transistor above 4 kelvin," *Nature Electronics*, Mar. 2022.

[3] Synopsys, *Sentaurus Device User Guide*, Version R-2020.09.