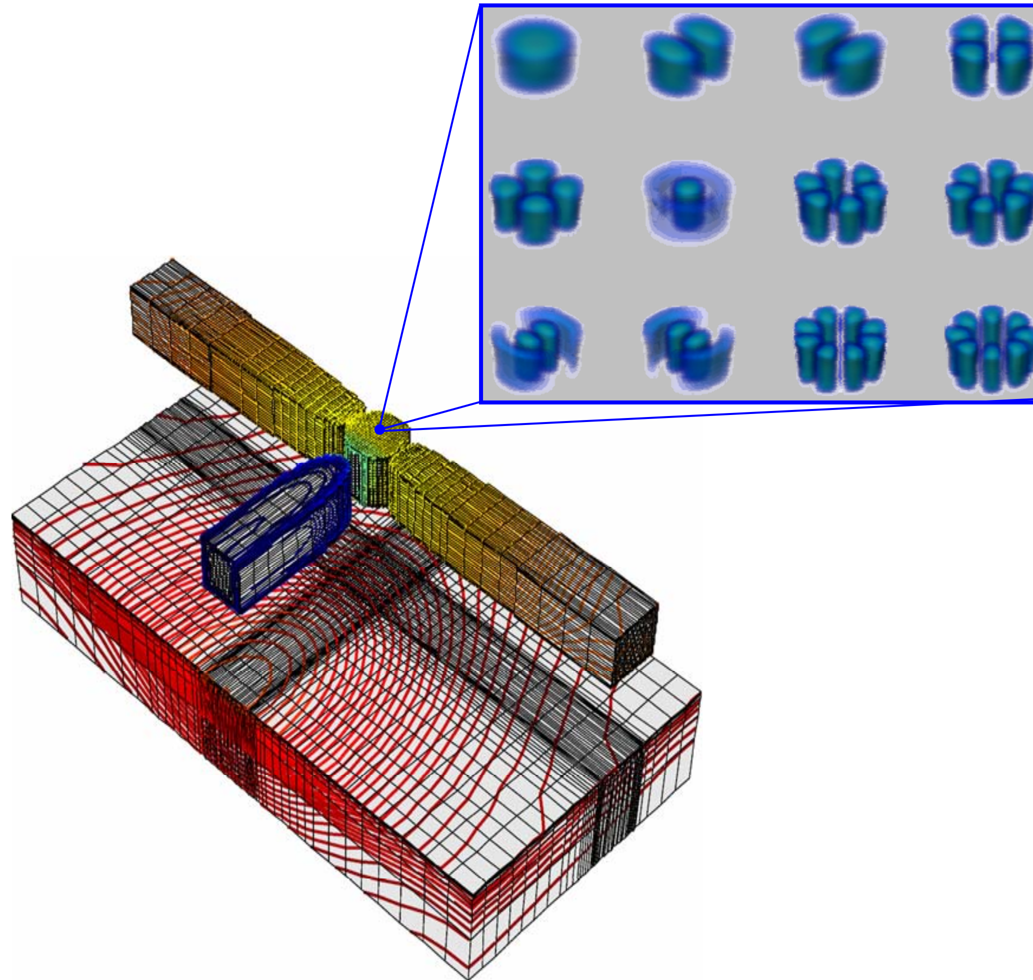
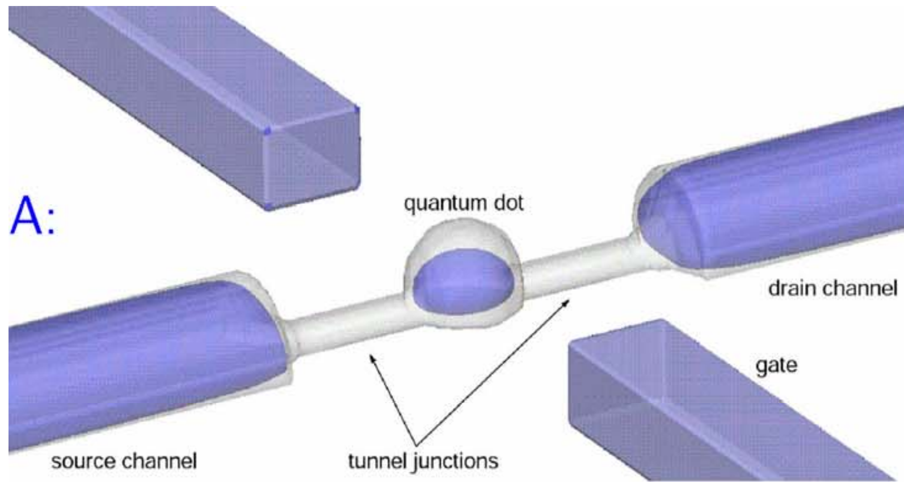
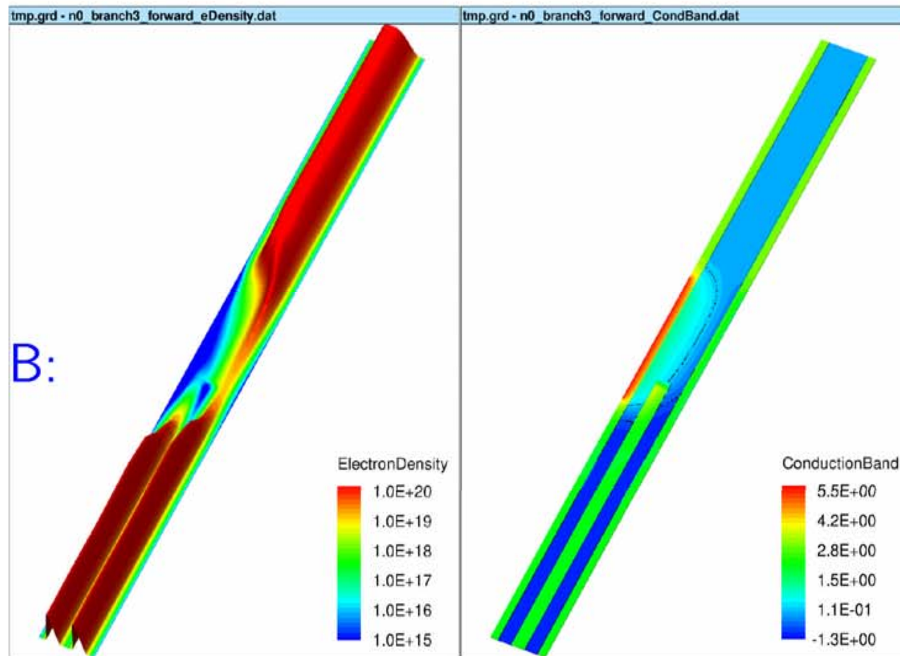
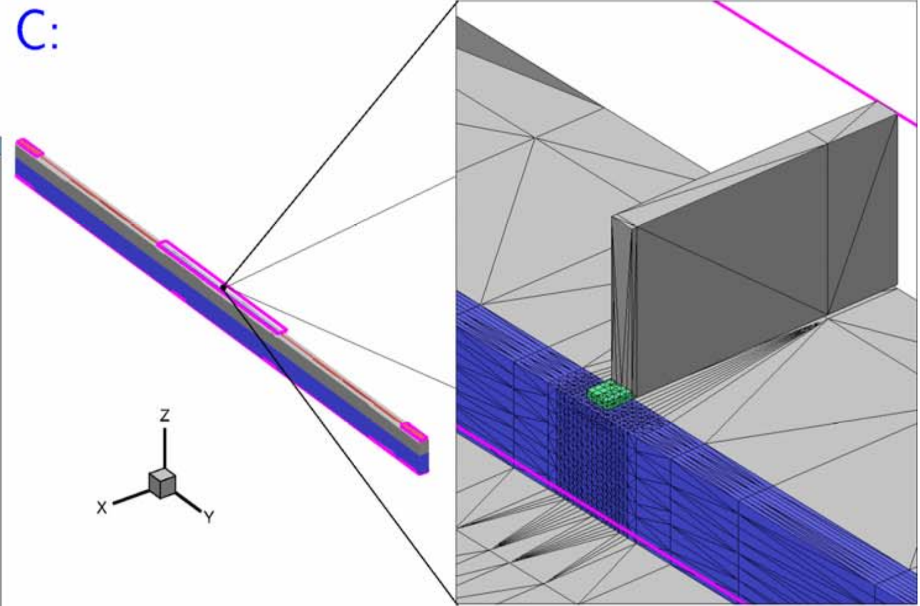
SIMNAD – SIMulator for NAnoDevices



Nanodevices have "critical dimensions" comparable with the electron wavelength.

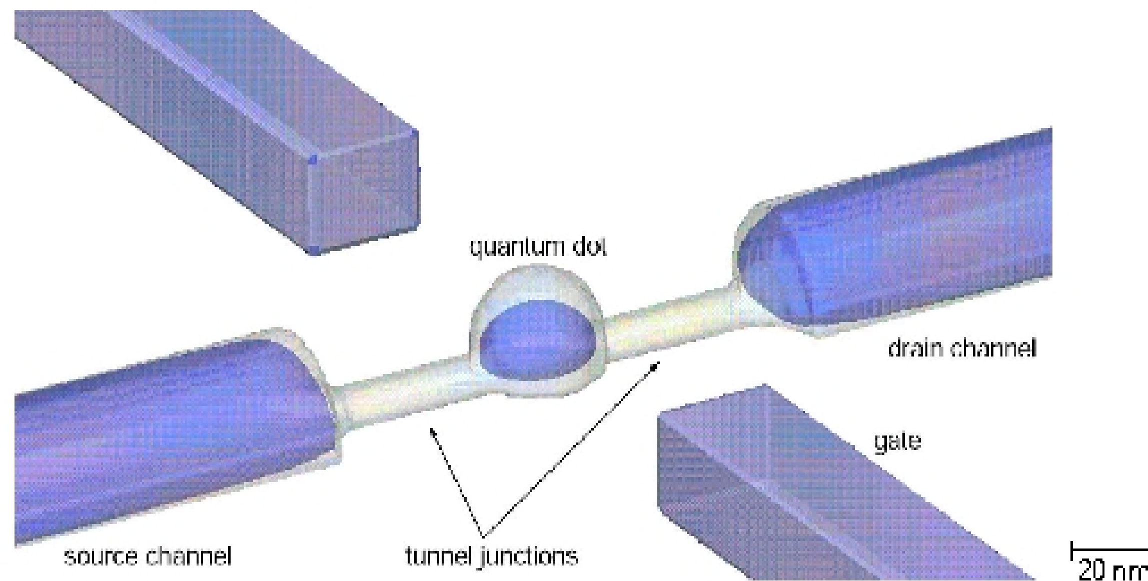






A: Single electron transistors
B: Quantum–ballistic devices
C: QD flash memory

The single-electron transistor



⋆ For SETs with extensions comparable to the electron wavelength this equivalent circuit treatment ceases to be applicable:

- Quantum depletion modifies the capacitances.
- Discrete energy levels influence the charging energy.
- The shape of individual wave–functions modulates the tunnelling resistances.

⇒ None of the parameters of the equivalent circuit are known!

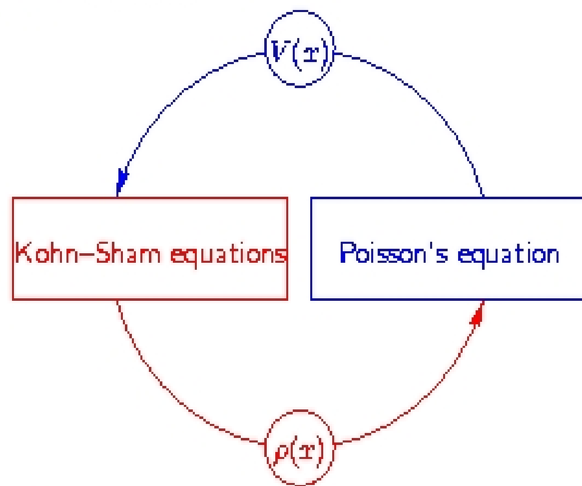
Physical model for nano-scale SETs

⋆ **Goal:** Compute the linear response conductance $G = \frac{\mathrm{d}I}{\mathrm{d}V_{\mathrm{drn}}}$ of nano–SETs !

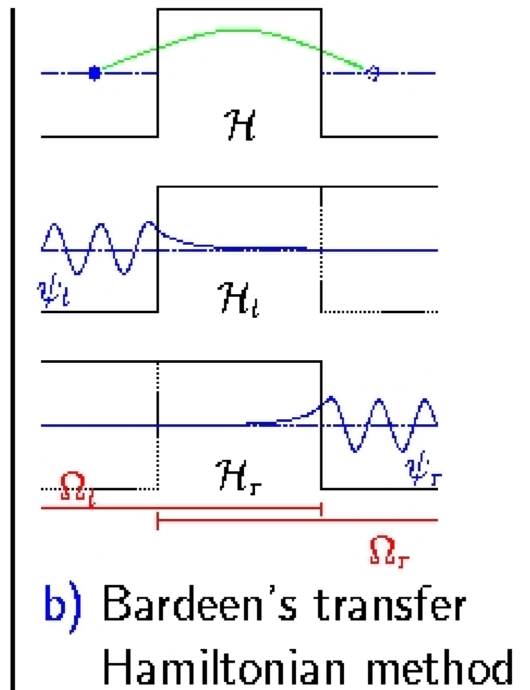
⋆ **Necessary ingredients:**

a) Self–consistent QM charge density and potential,
b) tunnelling rates between the quantum dot and the channels,
c) occupation probabilities of the individual energy levels of the quantum dot.

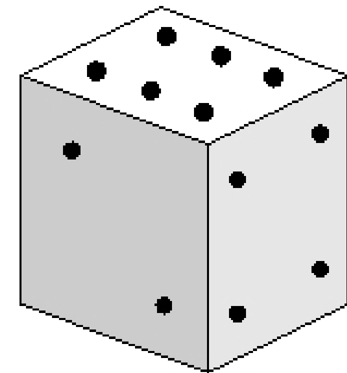
⋆ **Tools:**



a) finite temperature density functional theory

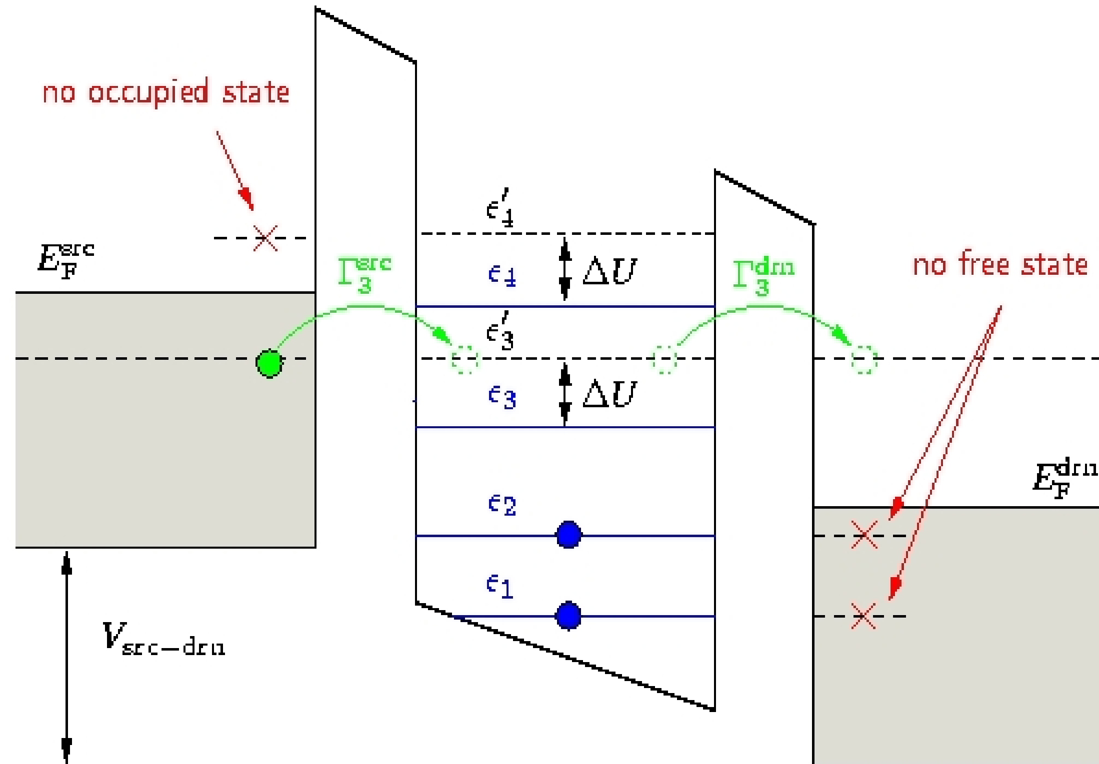


b) Bardeen's transfer Hamiltonian method



c) Monte–Carlo based statistical mechanics

Computation of the conductance

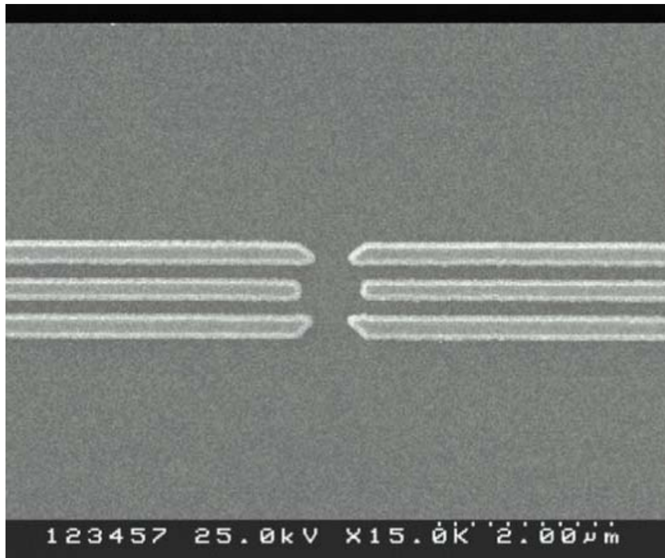


Linear response:

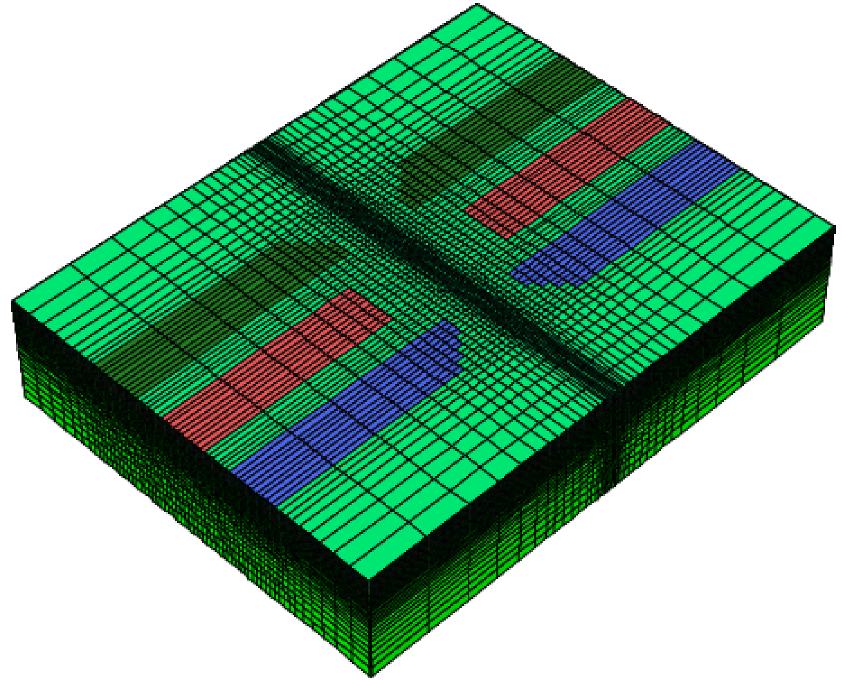
$$G = \left.\frac{dI}{dV}\right|_{V=0} = \frac{e^2}{k_B T} \boxed{\sum_{\{n_\alpha\}}} \sum_\alpha \frac{\Gamma_\alpha^{src}\Gamma_\alpha^{drn}}{\Gamma_\alpha^{src} + \Gamma_\alpha^{drn}} P_{eq}(\{n_i\})\delta_{n_\alpha,0} f\left(\beta(\epsilon'_{\alpha,\{n_i\}})\right).$$

The potentially **huge** phase–space sum $\sum_{\{n_\alpha\}}$ is evaluated by a Monte–Carlo method.

GaAs/AlGaAs QPC and SET



University Würzburg (2002)

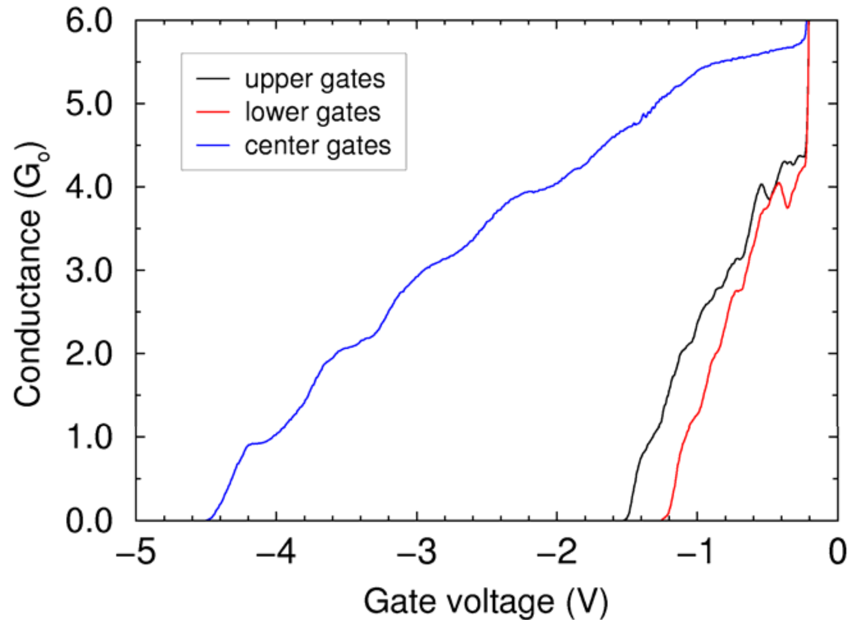


• vertical direction: 10 nm GaAs cap layer, 50 nm $Al_{0.2}Ga_{0.8}As$ layer doped with Si, 20 nm AlGaAs spacer (undoped), and GaAs (undoped) below

• 3 QPCs formed by biased pairs of opposite electrodes

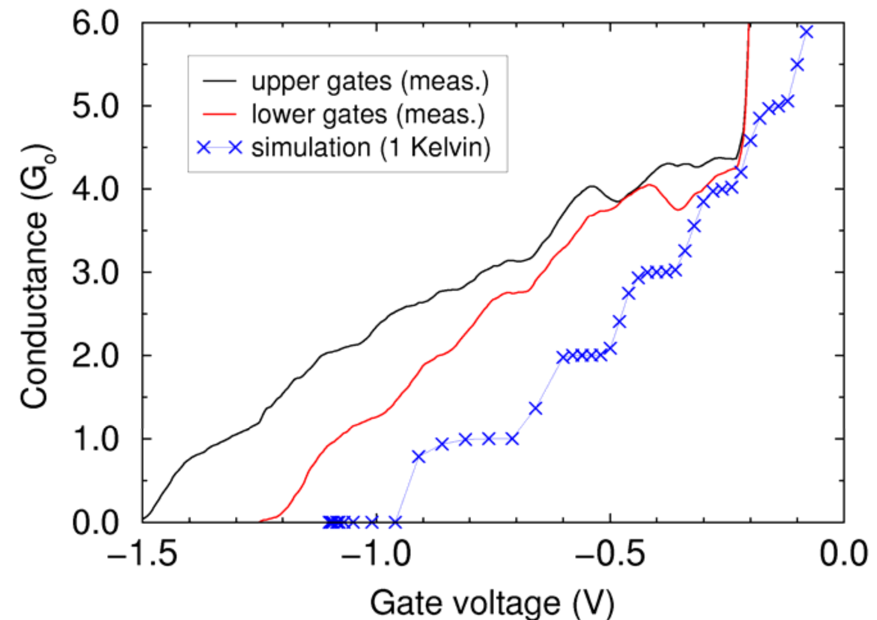
• SET operation when using outer pairs to form tunnel barriers and inner pair as “gate”

Conductance characteristics of QPCs

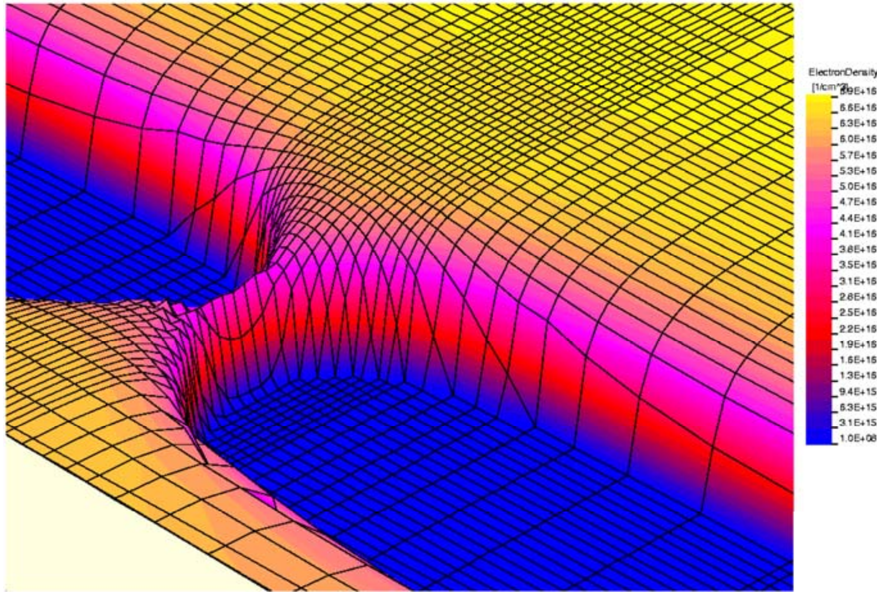


- measured QPC conductance of the 3 independent gate pairs at 0.3 K
- G_0 = 2 times quantum conductance $e^2/\hbar$ (incl. spin degeneracy)

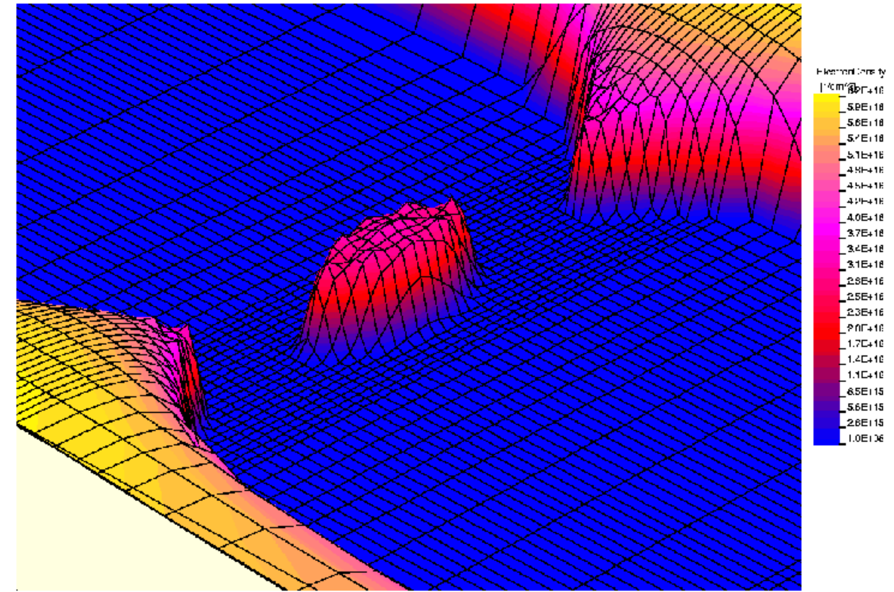
- comparison between simulation at 1 K and measured (nominally equal) outer gate pairs
- 1 K was found to be the sample temperature from simulated broadening of the conductance oscillation peaks



Charge density



- electron density in an outer QPC at a depth of 90 nm and a bias of -1 V (all other gates floating)



- electron density for SET operation at a depth of 90 nm with -1 V at outer gates and -0.5 V at inner gate

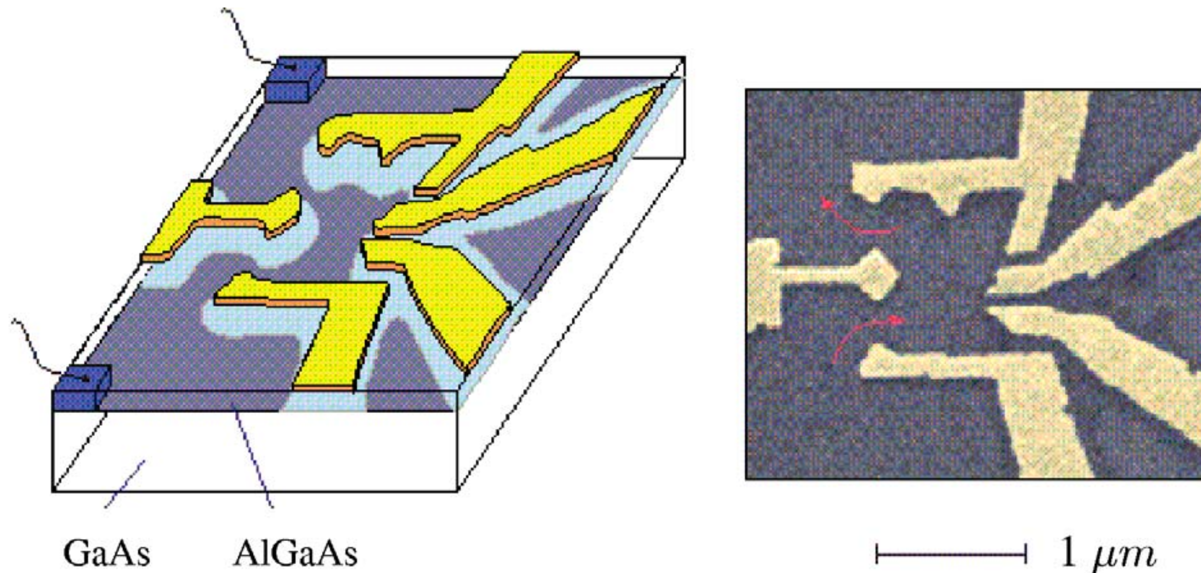
GaAs/AlGaAs split-gate SETs (general)

$GaAs/Al_xGa_{1-x}As$ heterostructures

- $Al_xGa_{1-x}As$: barrier material
- thin epitaxial layers (defect-free interfaces)
- formation of a 2DEG at interface

Split-gate technique

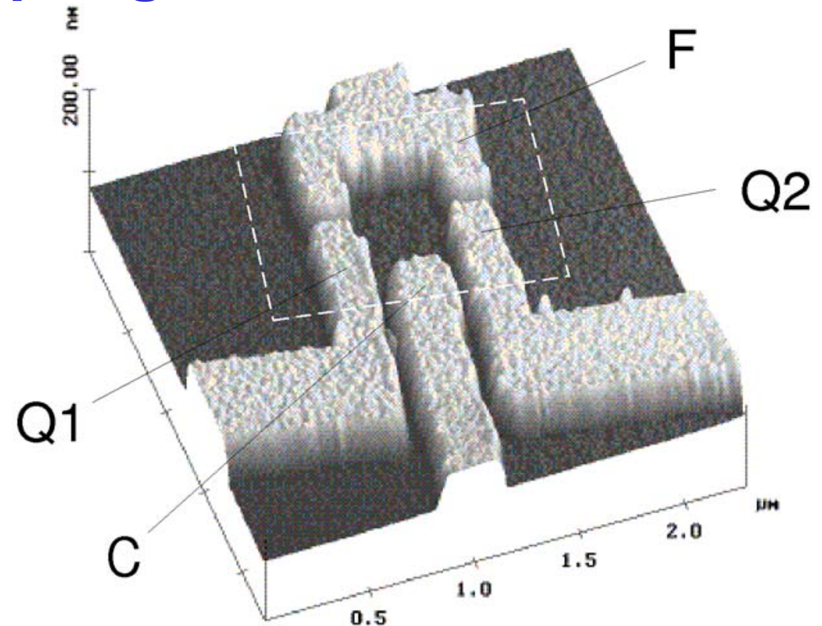
- 2DEG can be depleted electrostatically
- small channels or dots with variable size
- quantum dot diameter ~ 100 nm



S. R. Patel et al., PRL 80, 4522 (1998)

GaAs/AlGaAs split-gate SET

- $GaAs/Al_{0.32}Ga_{0.68}As$ heterointerface 37 nm below the top gate
- Fermi-level pinning: 600 meV below the conduction band
- gate: Ti(Au)/GaAs Schottky contact, barrier height 800 meV
- deplete 2DEG below -200...-300 meV



T. Heinzel, TU Munich (1994)

Conduction band E_C (eV)

0.0 0.4 0.8

z (nm)

0 20 40 60

y x z

5 nm GaAs cap-layer

8 nm $Al_{0.32}Ga_{0.68}As$

2 nm AlAs

2 nm GaAs

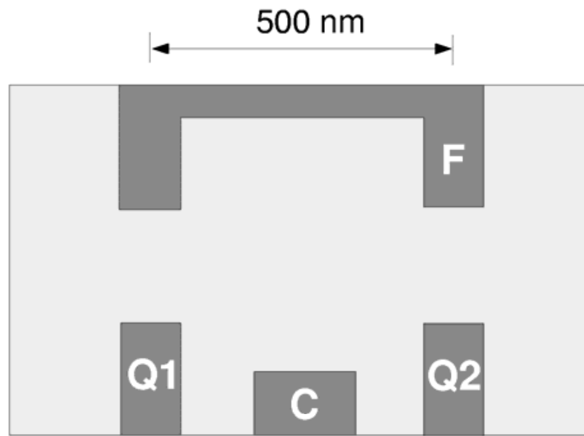
4 nm $Al_{0.32}Ga_{0.68}As$

$(N_d = 5 \times 10^{12}\ \mathrm{cm}^{-2})$

16 nm $Al_{0.32}Ga_{0.68}As$

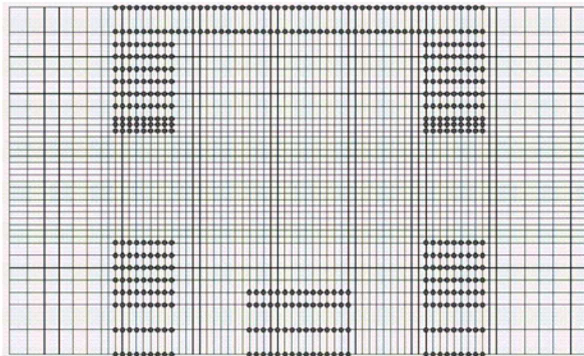
GaAs substrate

Device modeling



Scheme of the narrow split-gate

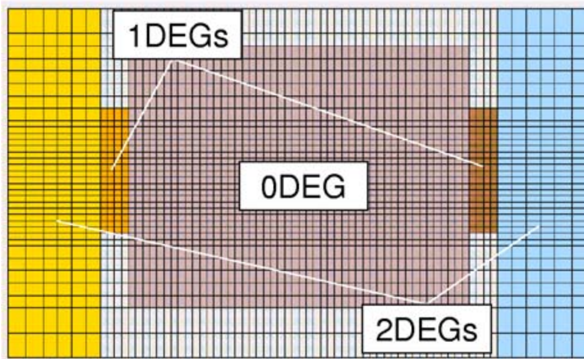
- black: Schottky gates
  - F: finger gate
  - Q1: QPC 1
  - Q2: QPC 2
  - C: control gate
- grey: exposed surface



3D non-uniform tensor-product grid

(cut in *xy*-plane at top gate layer)

- total area: 1000 nm x 600 nm x 290 nm
- 69 x 36 x 70 grid points, 173 880 nodes
- dots: Dirichlet bc at Schottky gates



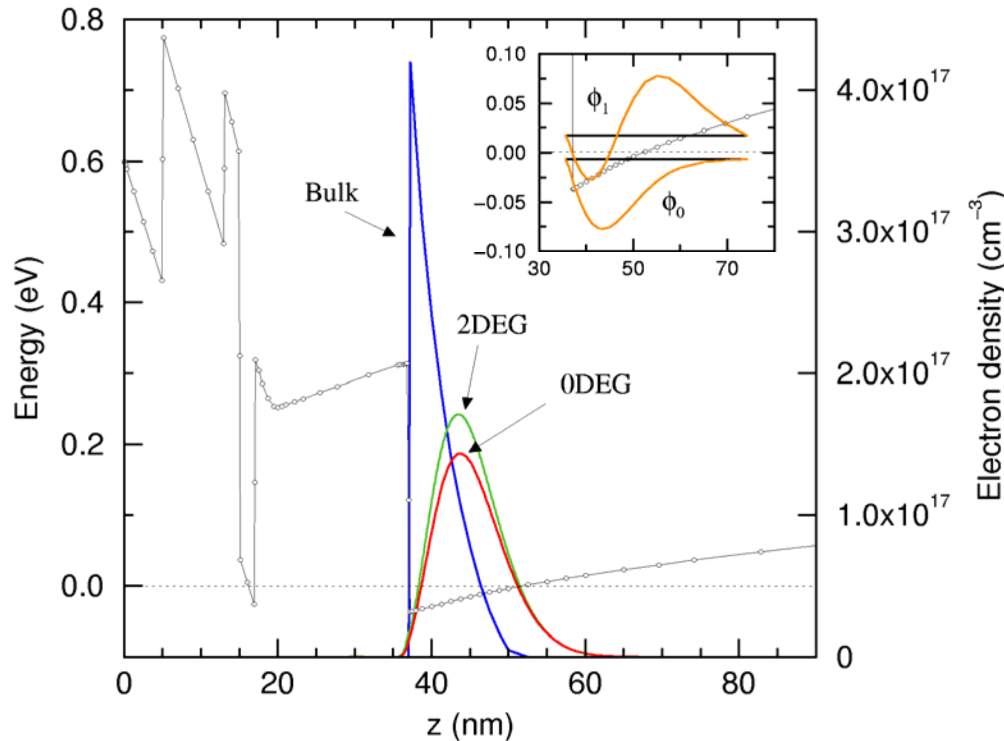
Domain decomposition

- quantum dot: 0DEG

585 nm x 450 nm x 39 nm, 42 336 nodes

- tunneling barriers (lead channels): 1DEGs
- lead regions (source, drain): 2DEGs

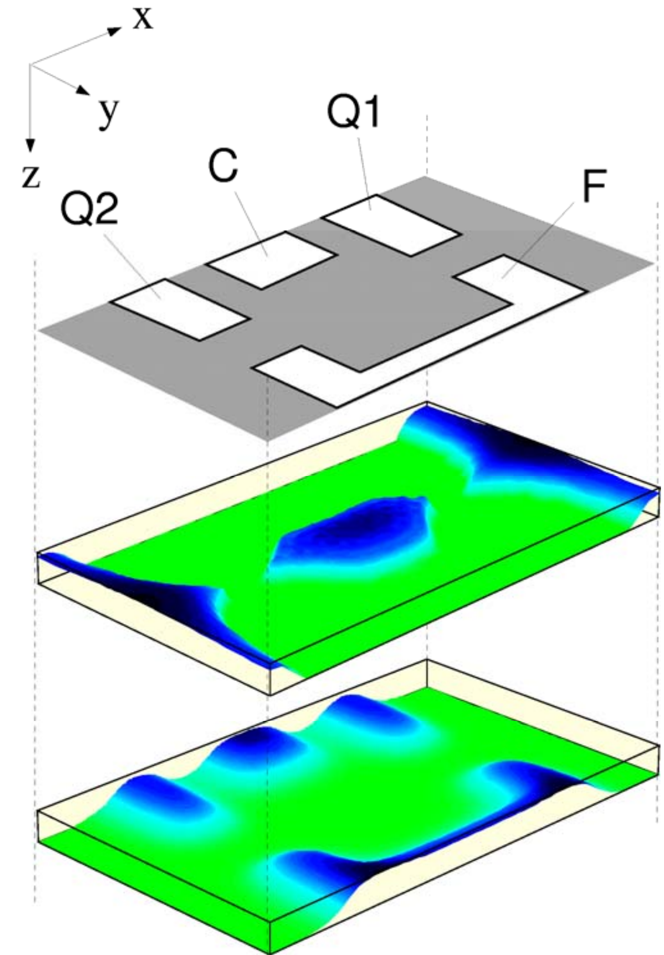
Self-consistent potential and charge density



Conduction-band edge and electron densities

(cut along the z-axis at the centre of the xy-plane)

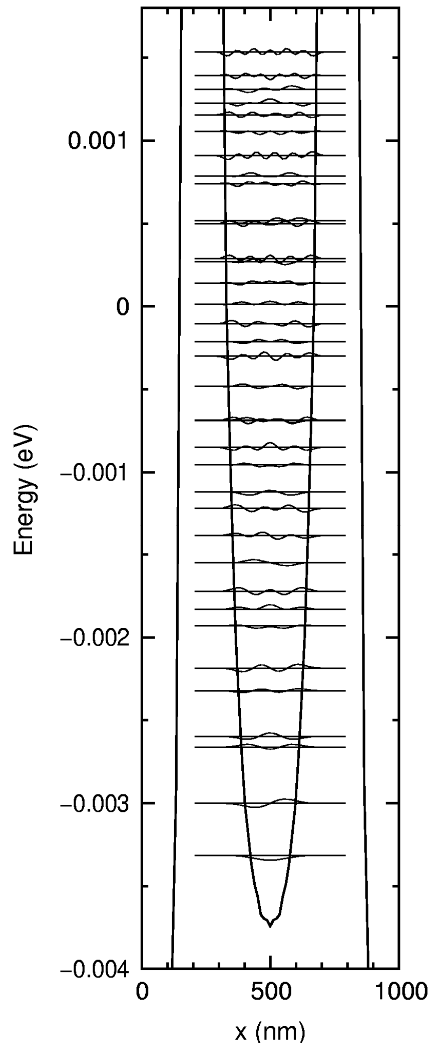
- GaAs/AlGaAs conduction-band offset: 360 meV
- Inset: 1D-subband energies (2DEG)

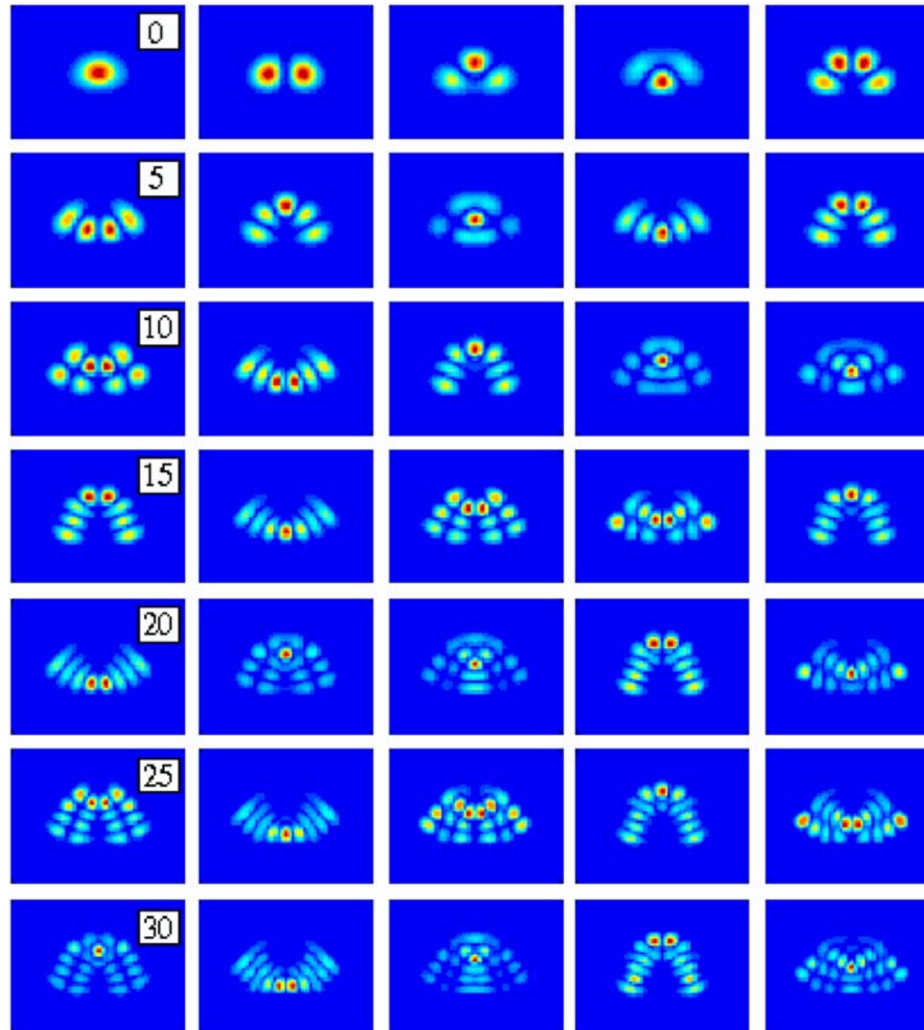


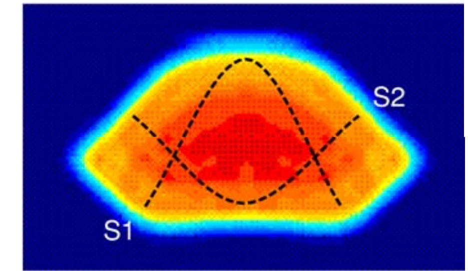
Split-gate structure (top), electron density (middle) and conduction-band edge (bottom)

(cut taken 8 nm below the interface in the xy-plane)

Single-particle wave functions







Approximate classical paths of wave function scars

S1
(4,6,9,12,15,19,23,28,33)

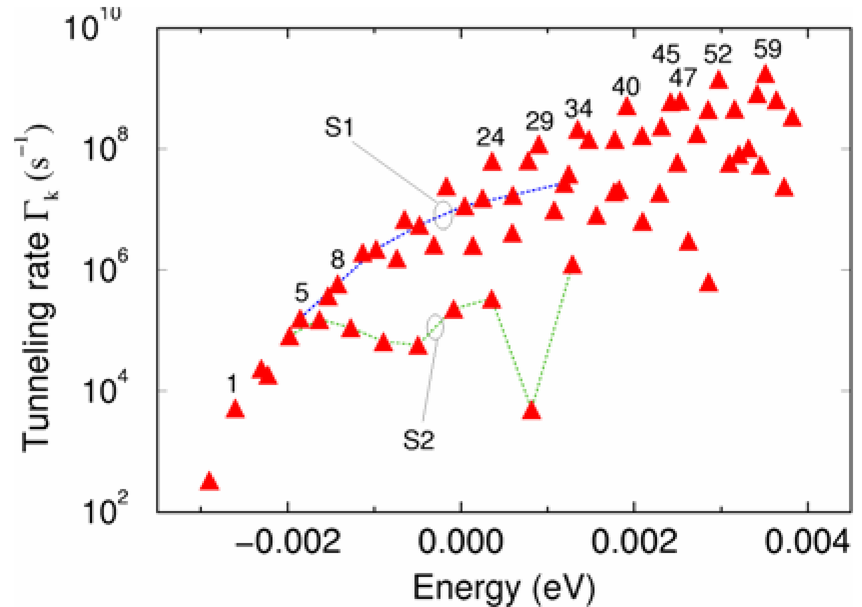
S2
(5,8,11,16,20,26,31)

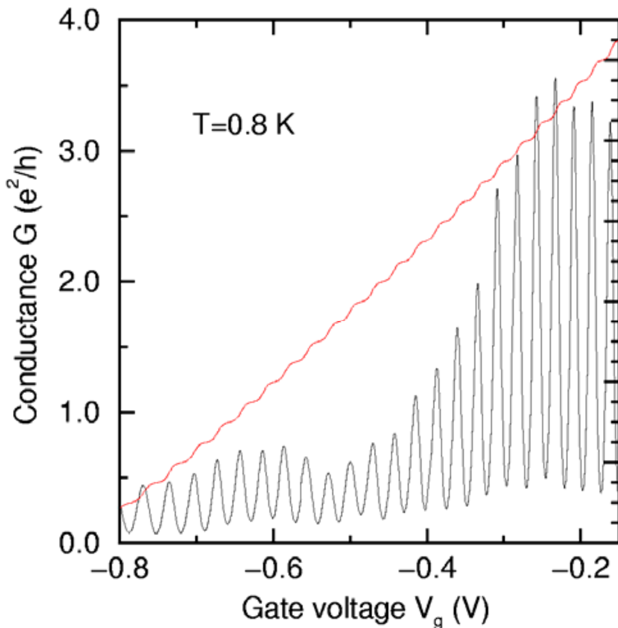
Single-particle level spectrum in the *x*-direction along the QPCs (left) and the squares of the lowest wave functions in the *xy*-pane (right) *(cut in the xy-plane)*

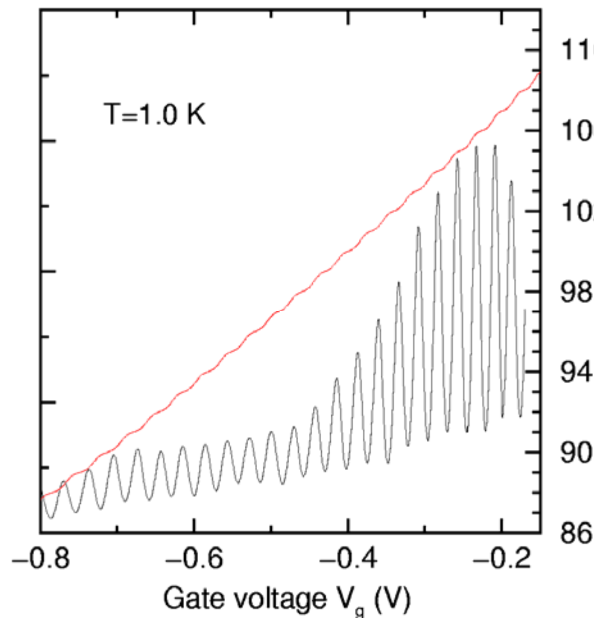
Conductance oscillations

Tunneling rates (elastic couplings) of the dot wave functions to the leads versus the single-particle eigenenergies.

- dotted lines link rates associated with a particular scar family
- states with strong coupling are labelled







Electron charging (red) and conductance (black) versus the control-gate voltage Vg at different temperatures.

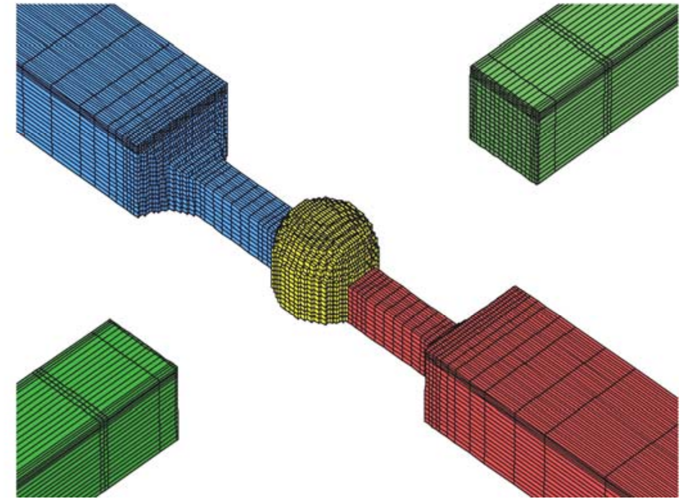
- oscillations with 300 meV period
- larger amplitude at lower temperature

SOI Single-electron transistor (SET)

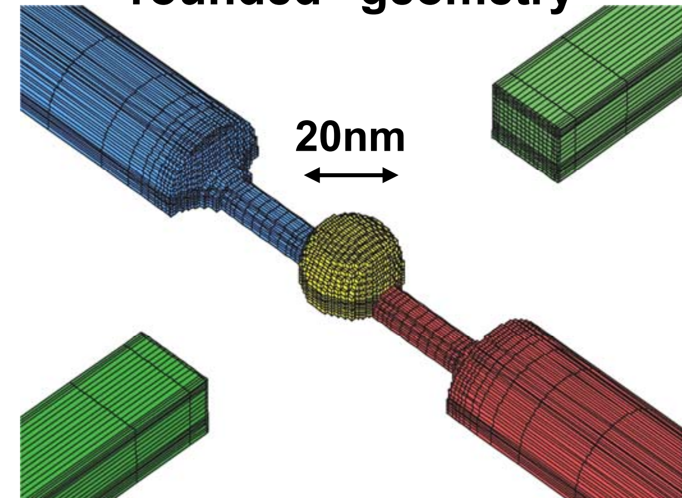
Template device:

Augke et al. APL 76, 2065 (2000)

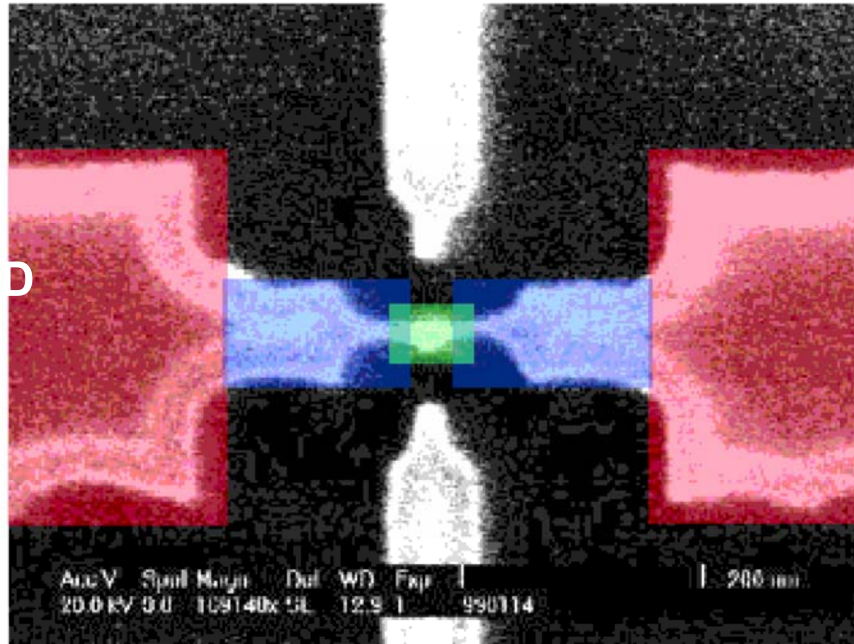
"prismatic" geometry



"rounded" geometry

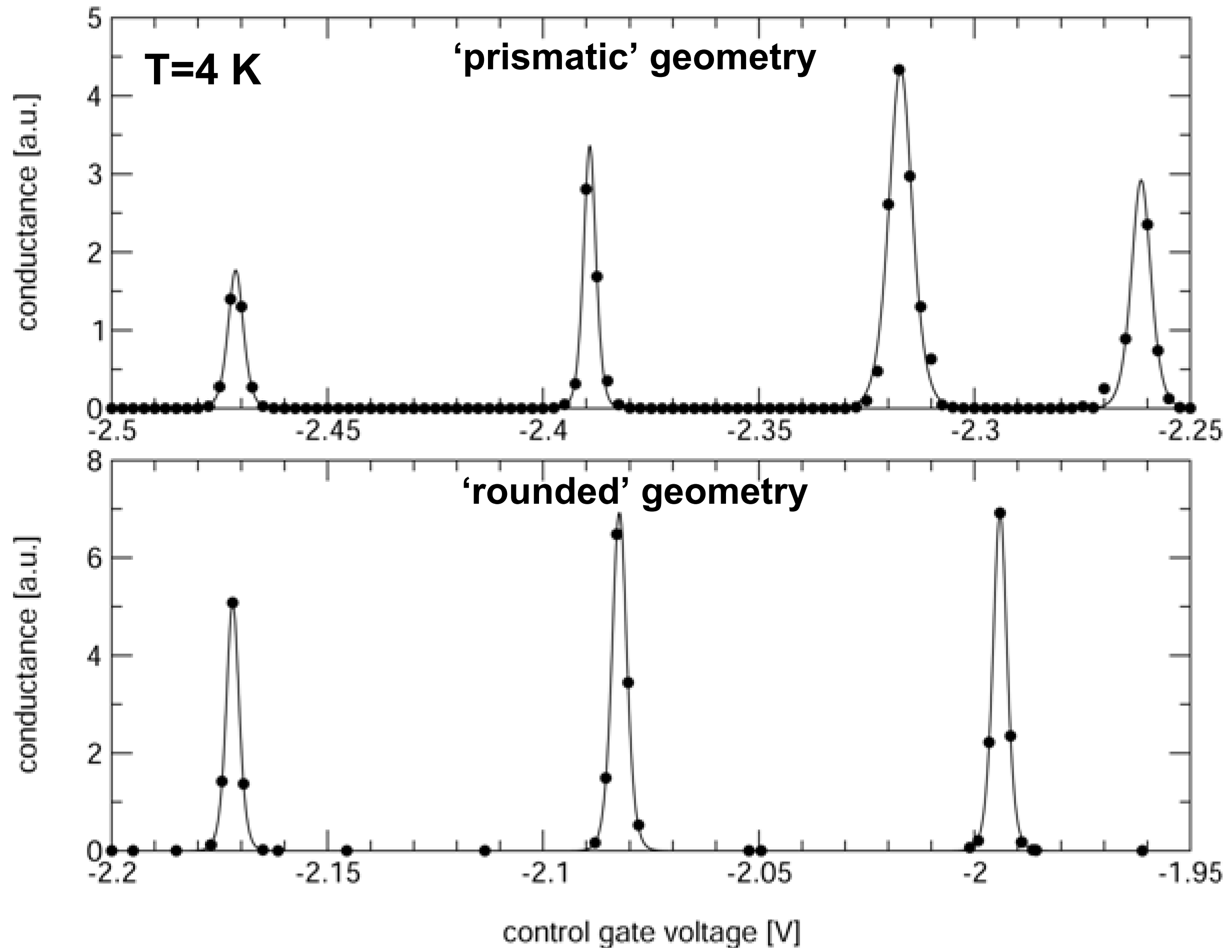


Simulation details



- Coupled Poisson/Kohn-Sham based on EMA and DFT (LDA for XC)
- 3D confinement in the dot, 2D in the narrow leads, 1D in the wide leads
- Adiabatic decoupling for computation of constriction conductance (Beenakker formula + Bardeen approach)
- Full phase-space sampling (MC) for dot occupation possible
- Complete ionization of donors (Mott)

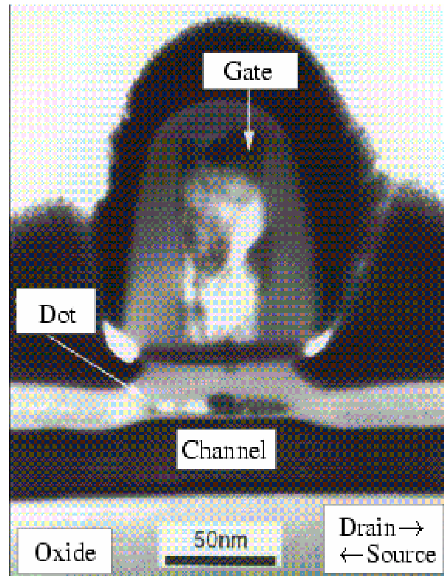
Conductance oscillations

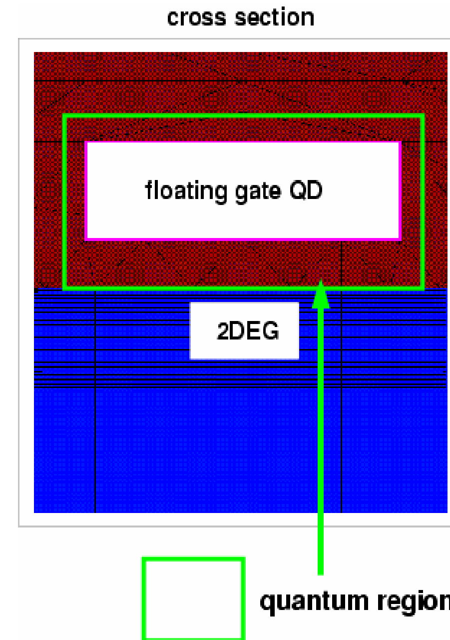


- C_g = 1.8 aF ('rounded'), C_g = 2.7 aF ('prismatic')
- Rounded geometry provides better electron confinement
- Conductance peaks several orders of magnitude off with respect to exp.

Simulation of memory devices

Device and interface definition

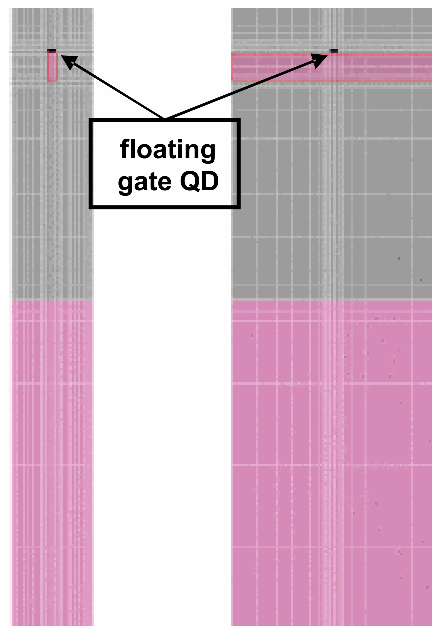


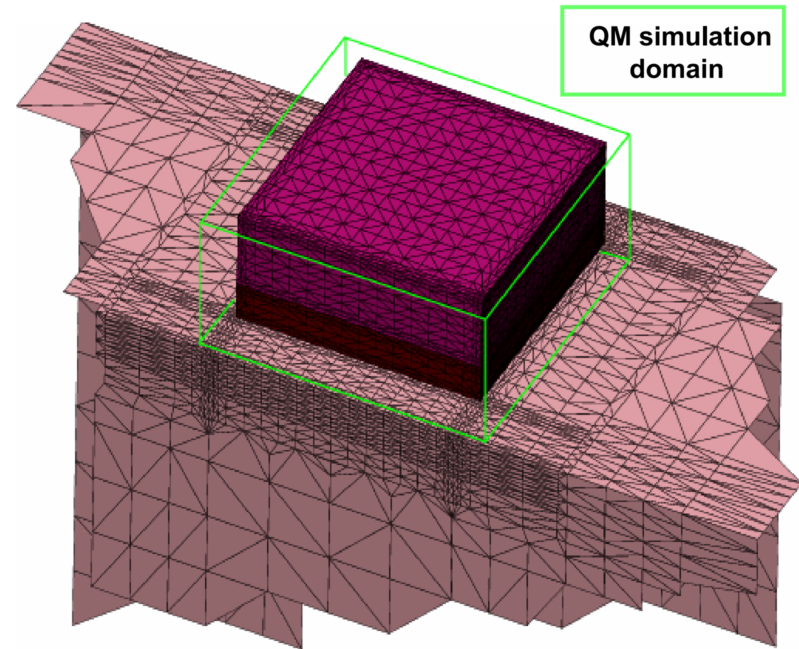


- SOI MOSFET with 7x7x2 nm^3 poly-Si floating gate (QD FLASH)
- channel doping = free parameter
- from Guo et al., Science *275*, 649 (1997)

- spatial interface: QM domain with QD, gate oxide, (optional: part of channel)
- Dirichlet boundary conditions for Kohn-Sham equation

Simulation of memory devices



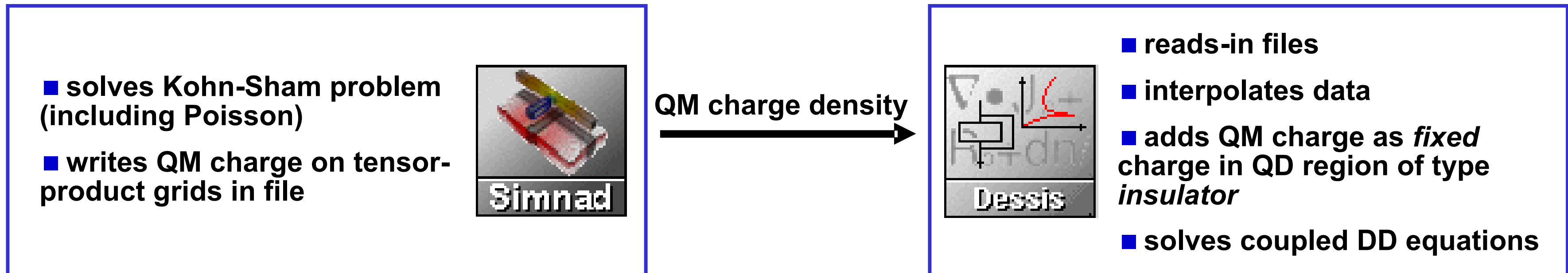


- equal SEM geometry for SIMNAD and DESSIS
- channel length = 200 nm, channel cross section = 10x26 nm^2
- ohmic source/drain contacts

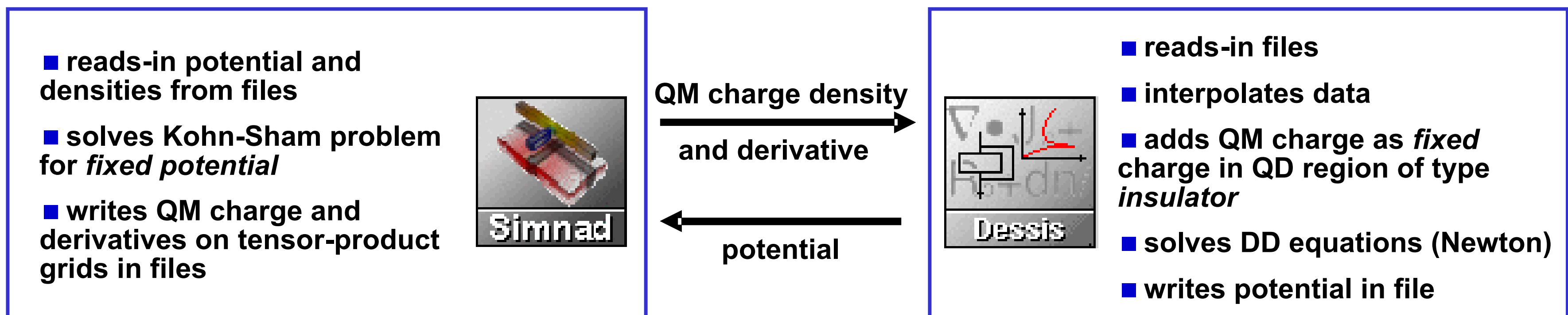
- tensor-product grid in QM simulation domain required
- refinement variation over 4 decades -> extreme challenge
- extremely inhomogeneous grids possible, but degradation of convergence

Coupling methodology *SIMNAD* – DESSIS

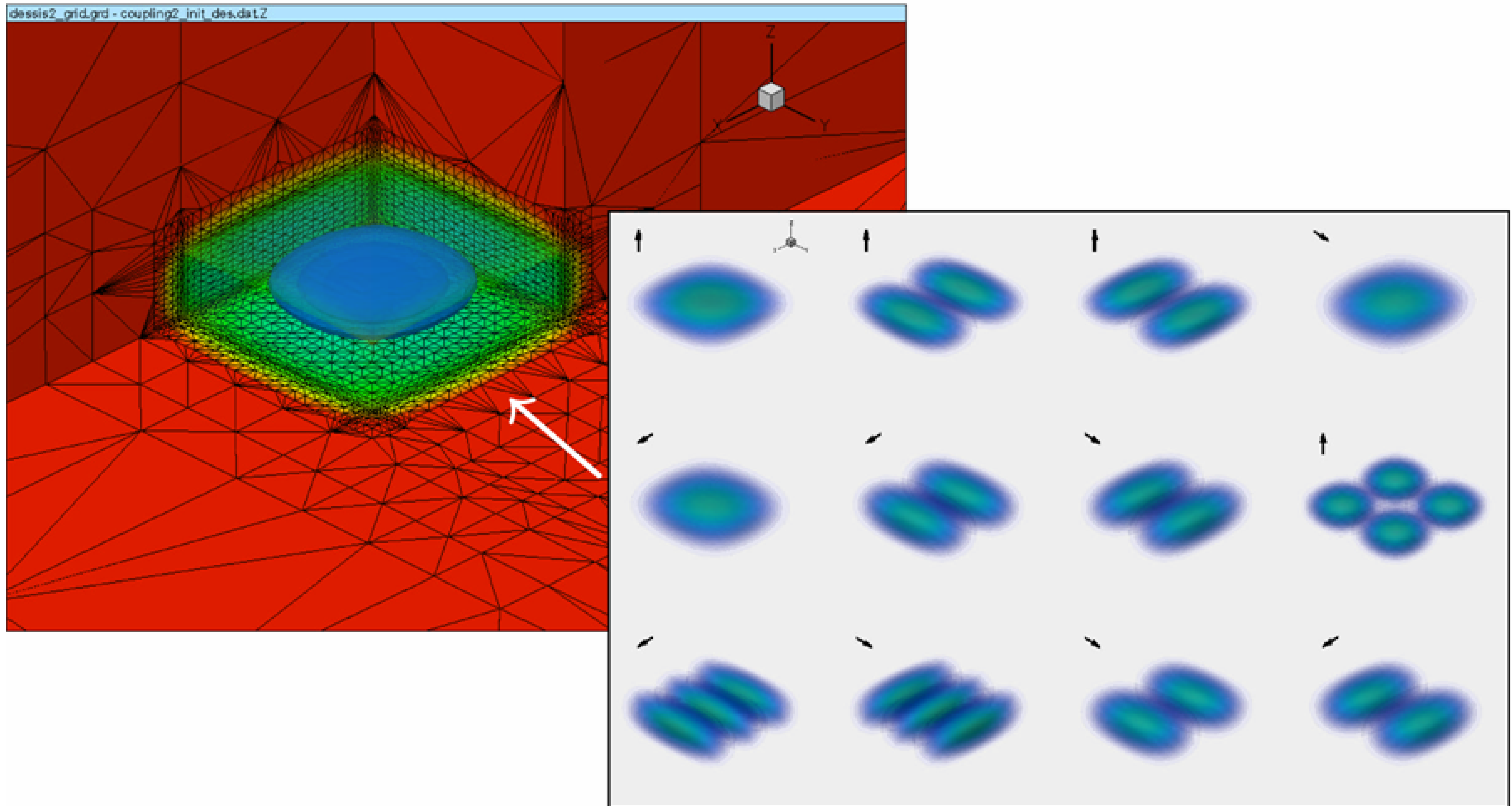
Non-self-consistent coupling:



Self-consistent coupling:

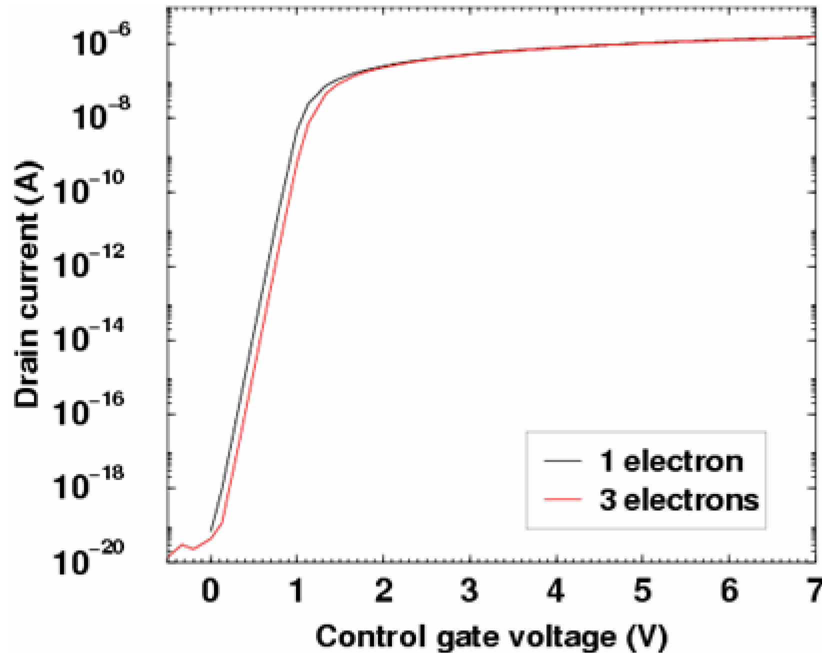


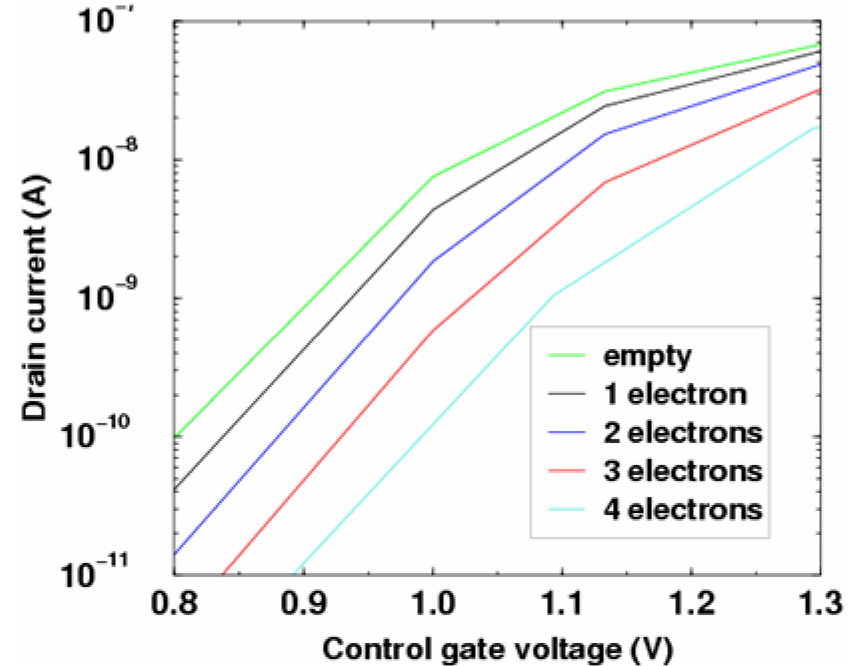
Simulator coupling: **SIMNAD** charge density on **DESSIS** mesh:



QM charge density in the dot from *SIMNAD* embedded in the DESSIS$_{\text{-ISE}}$ mesh

Threshold voltage shifts

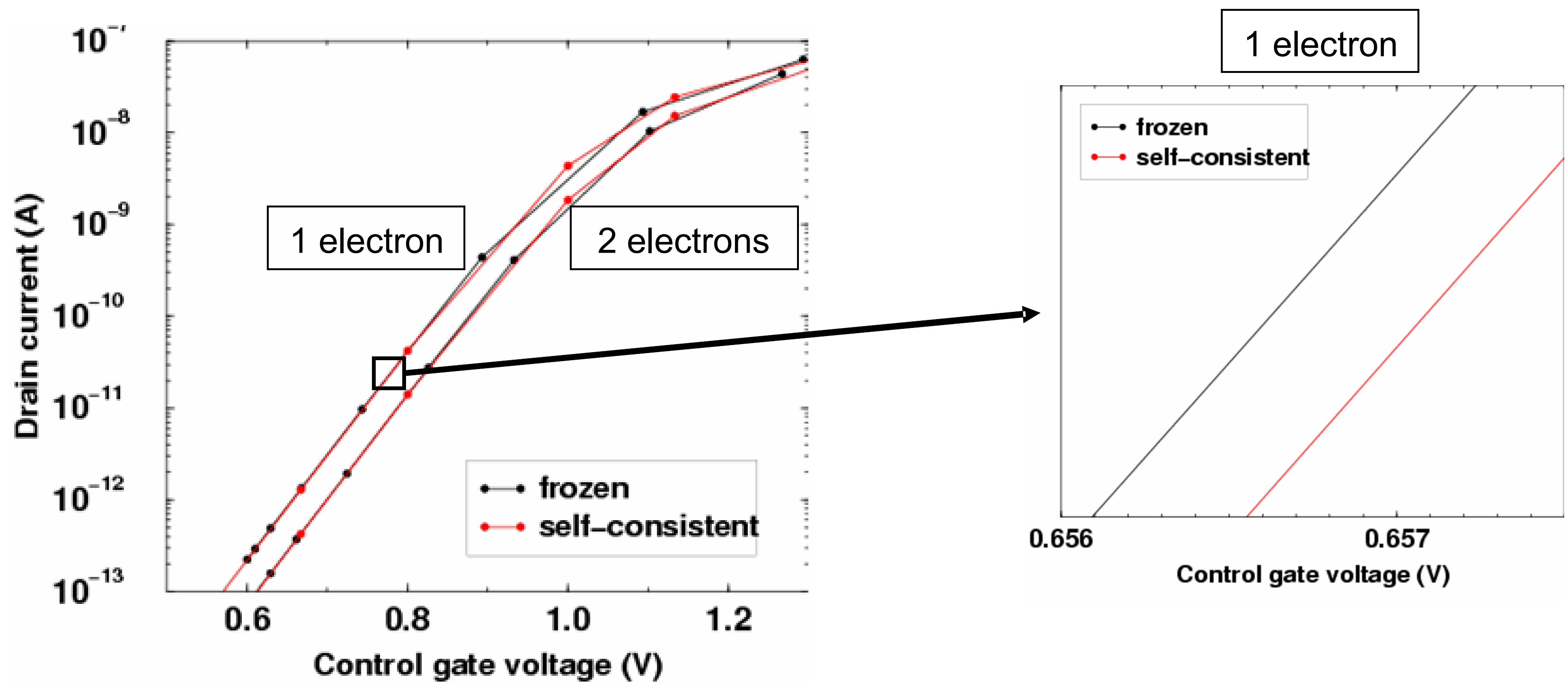




- I_D-V_G for frozen-in QM charge in QD
- main problem: mesh-refinement effects should not obscure single-electron effects => hugh meshes
- 53’917 vertices, 3.5 Gbyte memory, 100 min per bias point on DEC Alpha 4x1.25GHz

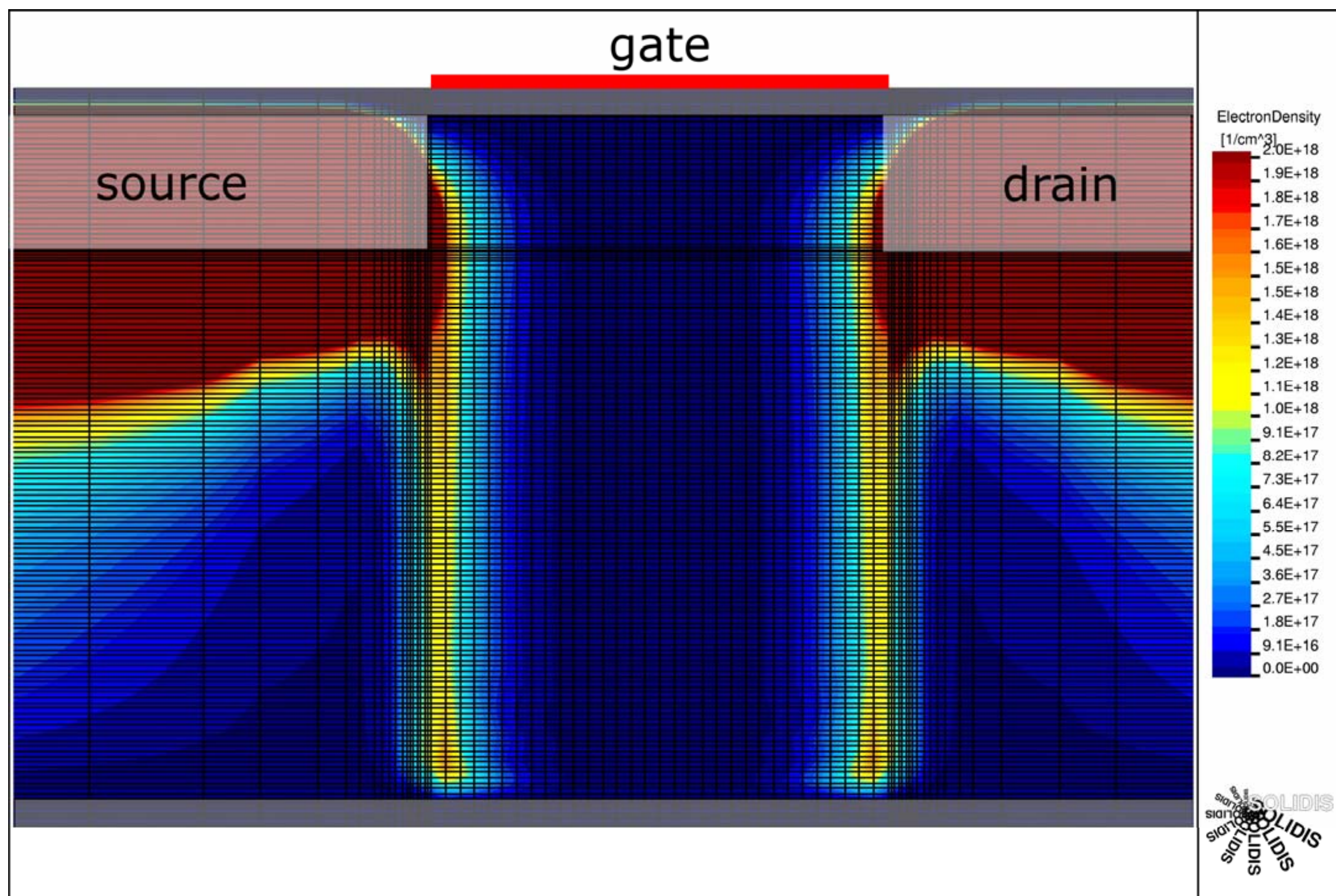
- increase of V_T per electron on QD between 35 – 55 mV
- monotonous increase (mesh?)
- good agreement with exp. (Guo)
- tiny difference to case of constant charge on floating gate!

Self-consistent coupling



- results for self-consistent coupling *SIMNAD* - DESSIS$_{\text{-ISE}}$
- almost no CPU time overhead
- very small self-consistency effect

Quantum-ballistic simulations of MOSFETs



Current density of a quantum system

★ $\mathbf{j} = \frac{\hbar}{m} |\mathbf{x}\rangle\langle\mathbf{x}| \Im\nabla$: (single–particle) current density operator

★ $\mathbf{P}$: statistical operator

★ expectation value of $\mathbf{j}$ in state $\mathbf{P}$:

$$\langle\mathbf{j}\rangle = \mathrm{tr}\left(\sum_{ij} c_i^+ c_j \langle i|\mathbf{j}|j\rangle \mathbf{P}\right)$$

★ in terms of the density matrix $M_{ij} = \mathrm{tr}\left(c_i^+ c_j \mathbf{P}\right)$

$$\langle\mathbf{j}\rangle = \sum_{ij} \langle i|\mathbf{j}|j\rangle M_{ij} = \mathrm{tr}\left(\mathbf{j}\ \blacksquare\right)$$

needs to be computed!

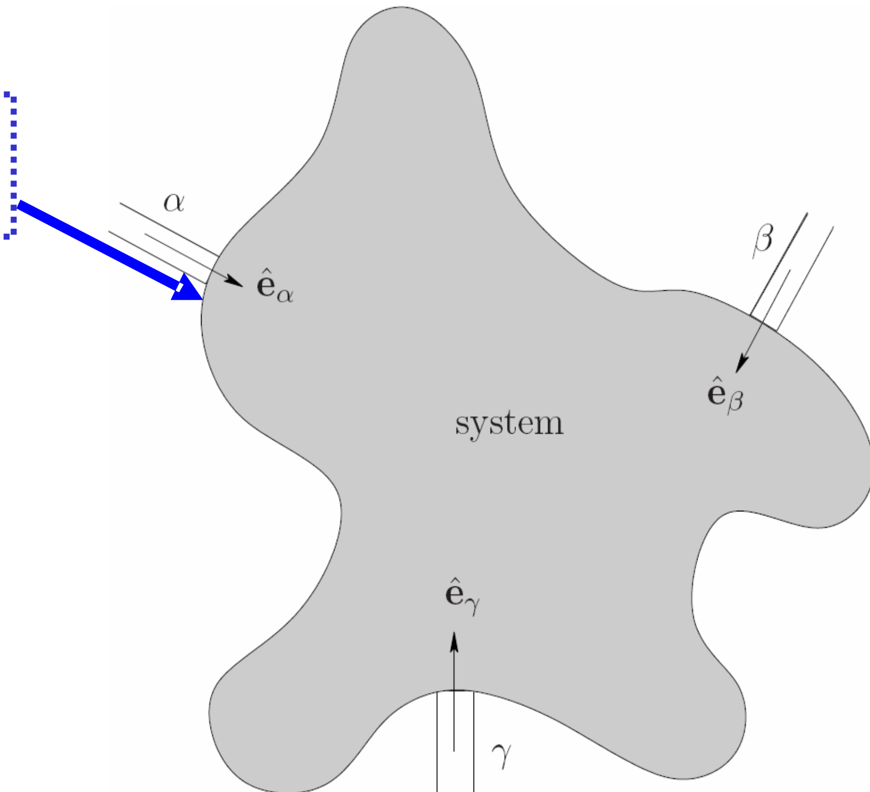
Computation of the scattering matrix

★ Disregard e–e interaction terms

★ No phonon scattering inside the device

★ use scattering configuration

$$\Rightarrow M_{ij} = \delta_{ij} f\left(\frac{\varepsilon_i - \varepsilon_{\mathrm{F}}^{(\alpha_i)}}{k_{\mathrm{B}} T}\right)$$



★ $\mathbf{M}$ is diagonal

★ Fermi function

★ $\langle \mathbf{j} \rangle = \sum_i \langle i | \mathbf{j} | i \rangle f\left(\frac{\varepsilon_i - \varepsilon_{\mathrm{F}}^{(\alpha_i)}}{k_{\mathrm{B}} T}\right)$

Application to two-terminal devices

⋆ Coherent transport

- $\nexists$ inelastic scattering.
- An e^- remains in a fixed Ψ (solution of Schrödinger eq.ⁿ).
- When occupied, Ψ carries a current $I(\Psi) \propto$ transmission probability $T(\epsilon)$.

⋆ Thermal carrier injection at the contacts.

⇒ Landauer–Büttiker formula:

$$I = -\frac{2e}{h} \sum_{v,i} \int_{\epsilon^0_{v,i}}^{\infty} \mathrm{d}\epsilon \, T_{v,i}(\epsilon) \Big(f\big(\beta(\epsilon - \epsilon^{\mathrm{src}}_{\mathrm{Fermi}})\big) - f\big(\beta(\epsilon - \epsilon^{\mathrm{drn}}_{\mathrm{Fermi}})\big) \Big) \quad \text{1D}$$

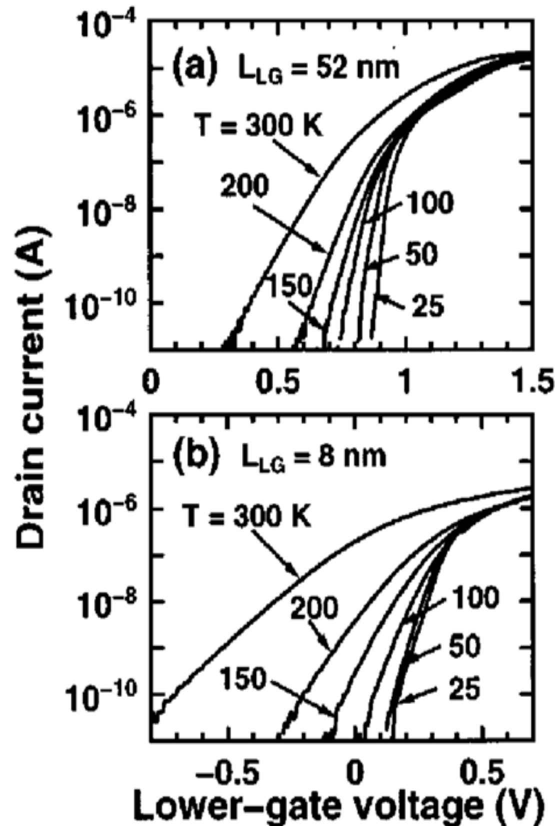
$$I = -\frac{2e}{h} \sqrt{\pi} \frac{W}{\lambda_{\mathrm{th}}} \sum_{v,i} \int_{\epsilon^0_{v,i}}^{\infty} \mathrm{d}\epsilon \, T_{v,i}(\epsilon) \Big(\mathfrak{F}_{-\frac{1}{2}}\big(\beta(\epsilon^{\mathrm{src}}_{\mathrm{Fermi}} - \epsilon)\big) - \mathfrak{F}_{-\frac{1}{2}}\big(\beta(\epsilon^{\mathrm{drn}}_{\mathrm{Fermi}} - \epsilon)\big) \Big) \quad \text{2D}$$

W: width of the device

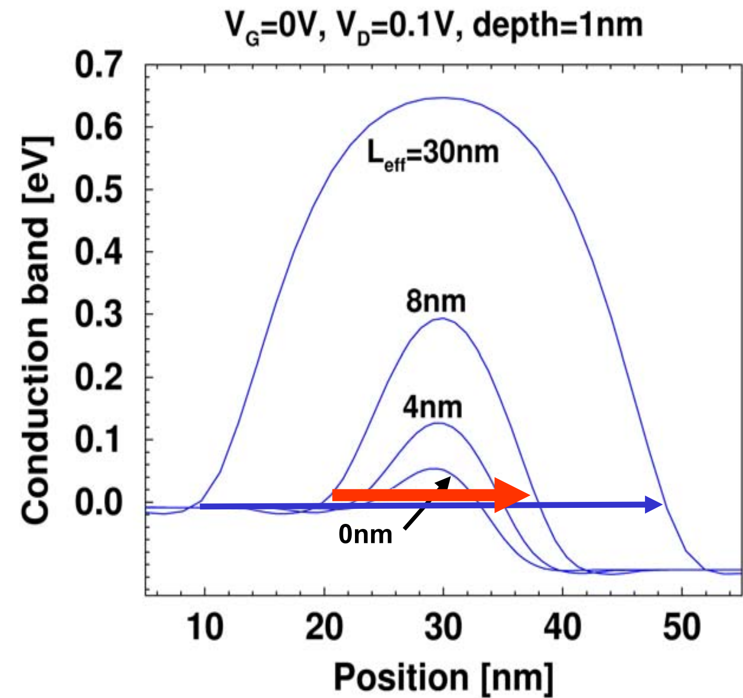
λ_{th}: electron thermal wave–length $h/\sqrt{2m^* k_{\mathrm{B}} T}$

The effect of source-to-drain tunneling

Experiment:

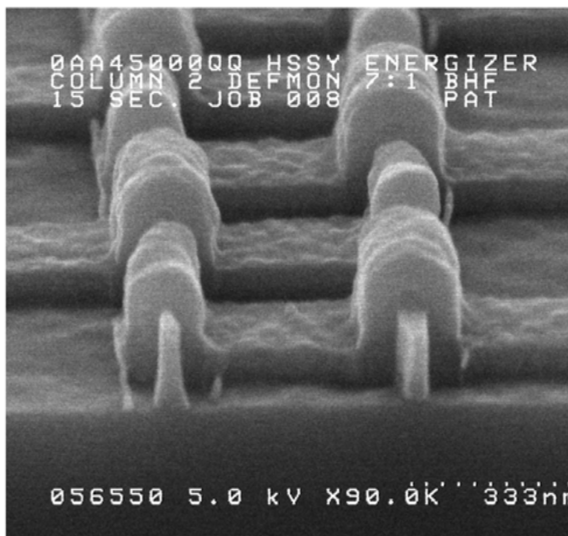


H. Kawaura et al., APL 76(25) (2000)



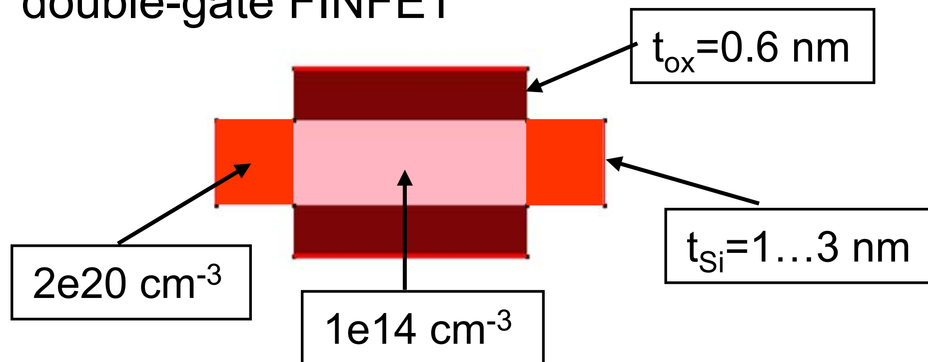
Is source-to-drain tunneling a fundamental limitation to CMOS scaling?

The effect of source-to-drain tunneling (2)

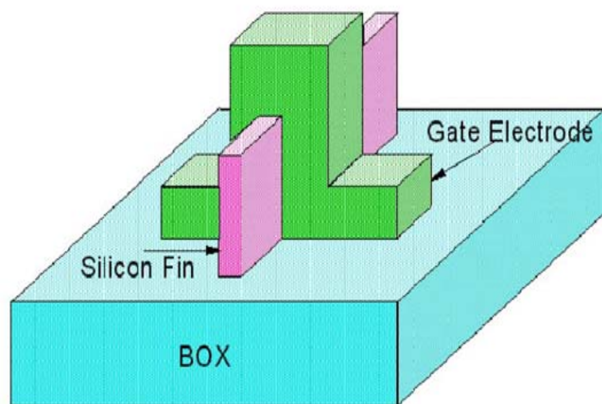


test device:

double-gate FINFET



J. Wang and M. Lundstrom, Proc. IEDM 2003

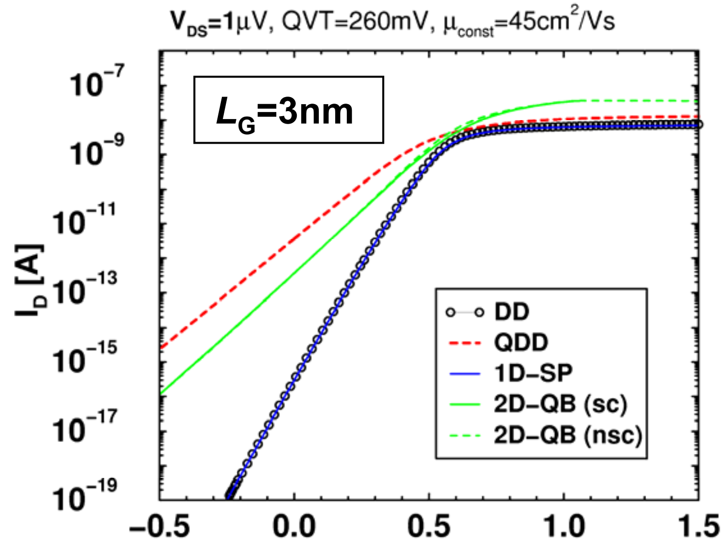


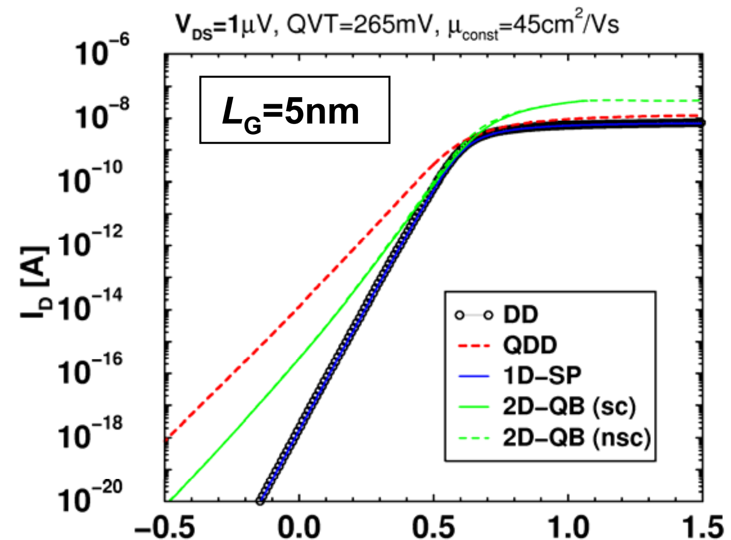
in simulation:

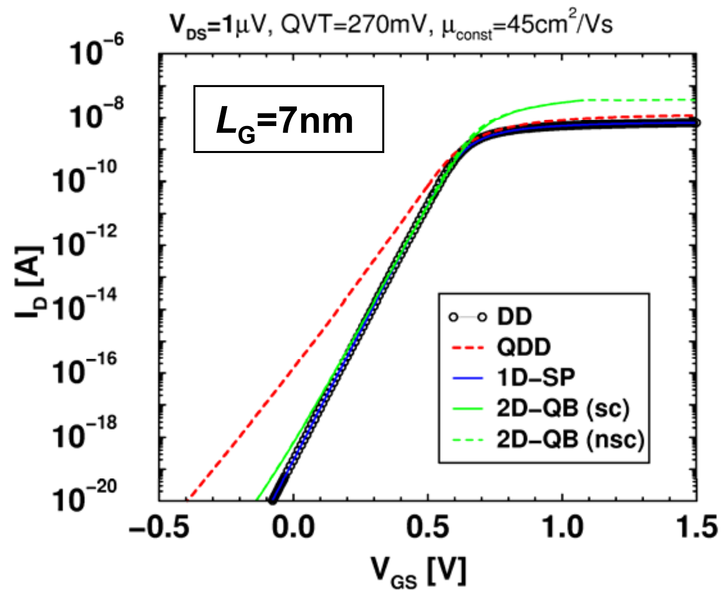
longer S/D, full oxide coverage

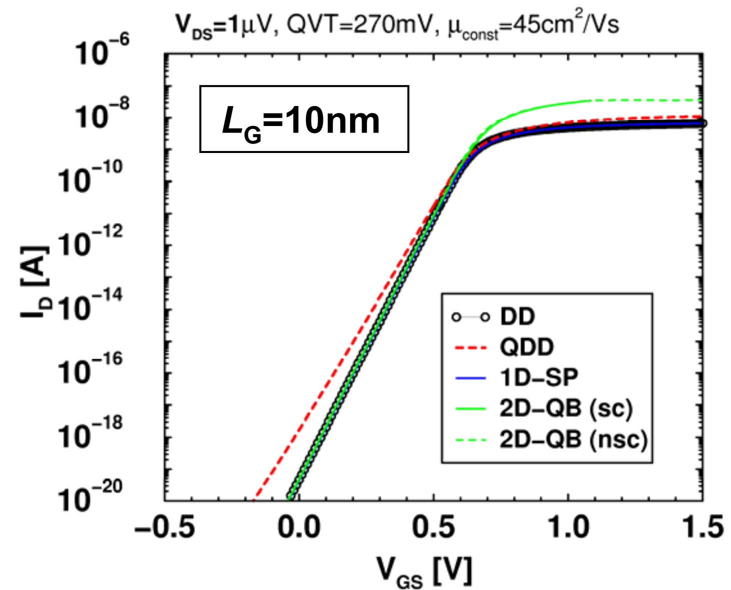
The effect of source-to-drain tunneling (3)

DGSOI with t_{Si}=1nm, transport in <100>



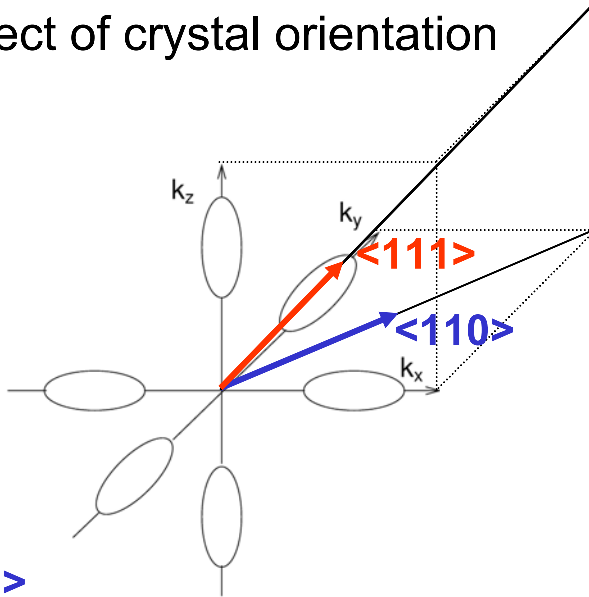




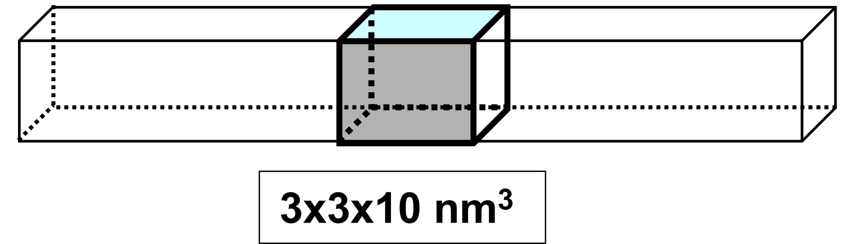


Crystal orientation and gate configuration

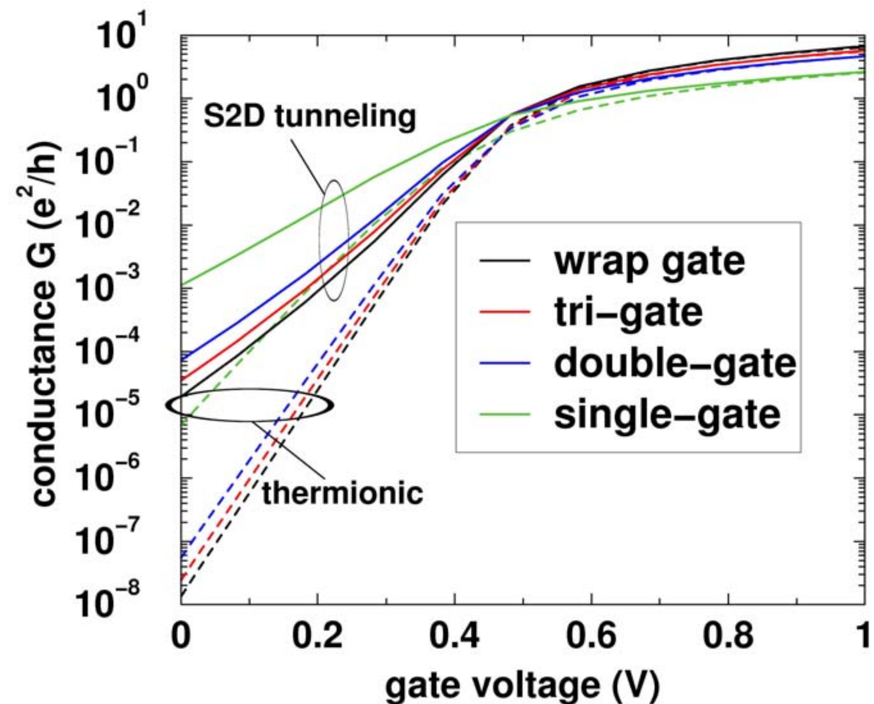
Effect of crystal orientation



Effect of gate configuration



3x3x10 nm^3



<110>

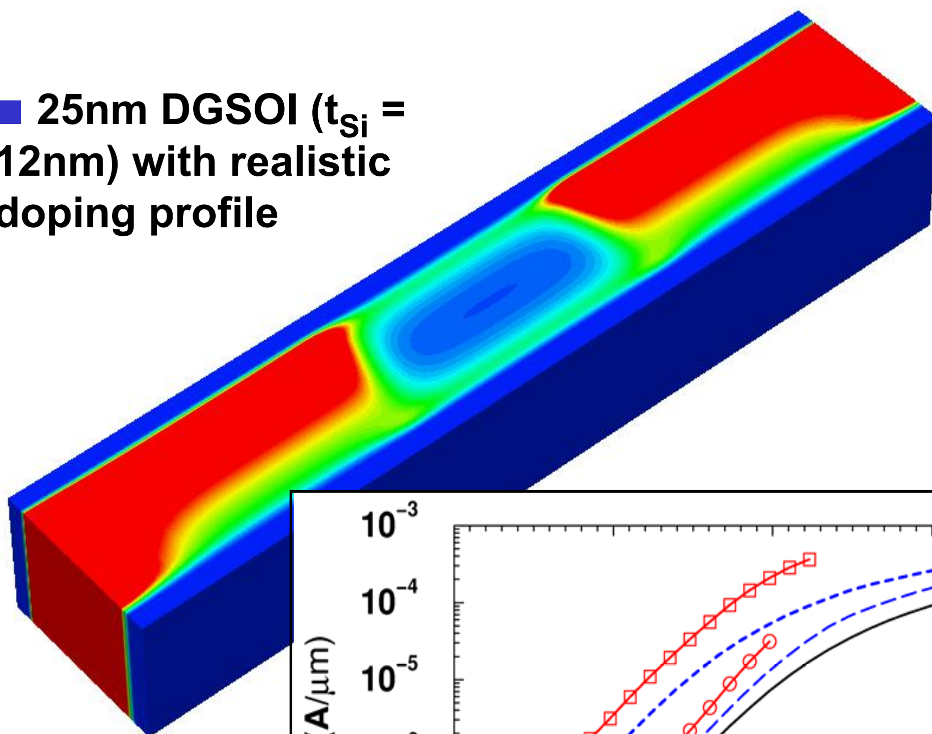
4 in-plane valleys with $2m_l m_t/(m_l+m_t)$ = $0.31m_0$, but 2 valleys with $m_t = 0.19m_0$ → no advantage

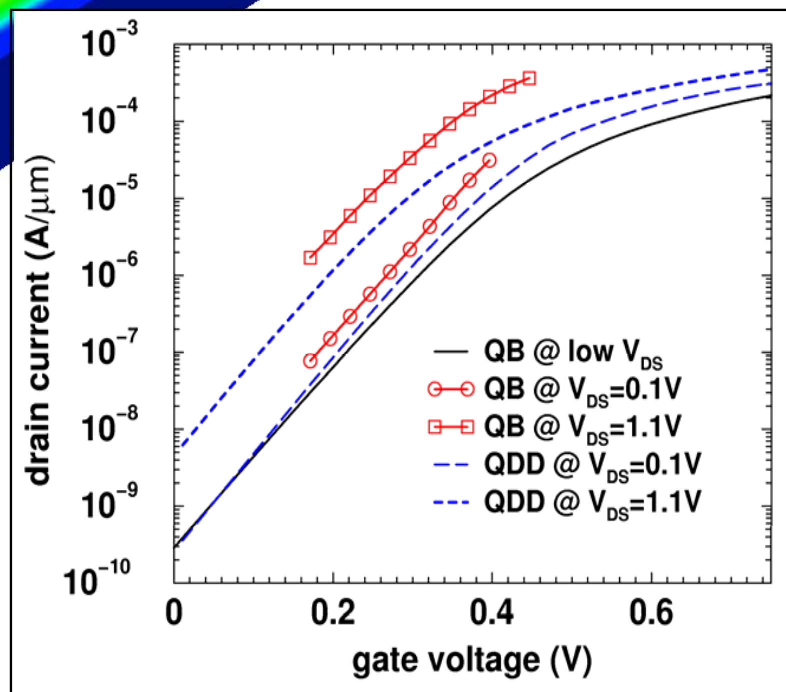
<111>

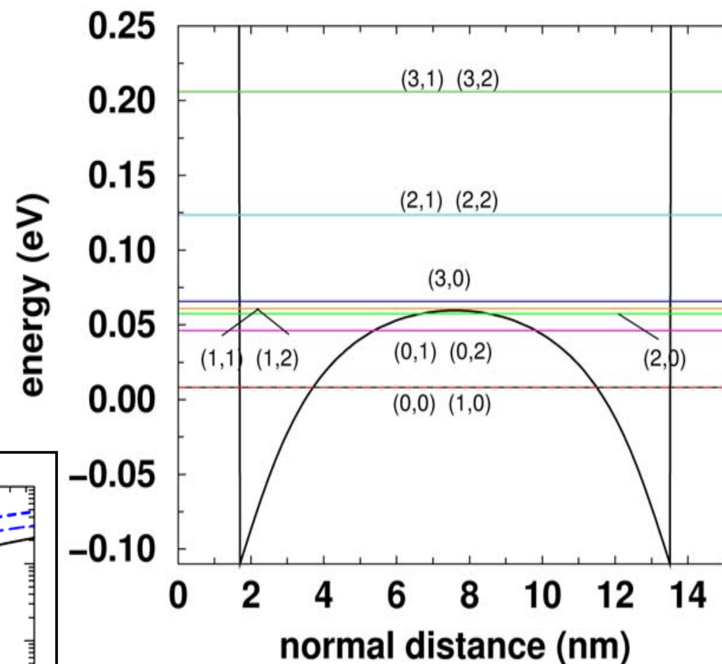
all six valleys with $3m_l m_t/(2m_l+m_t)$ = $0.26m_0$ → strong suppression of S2D-tunneling

Quantum-ballistic MOSFET: bulk *vs* DGSOI

- 25nm DGSOI (t_{Si} = 12nm) with realistic doping profile



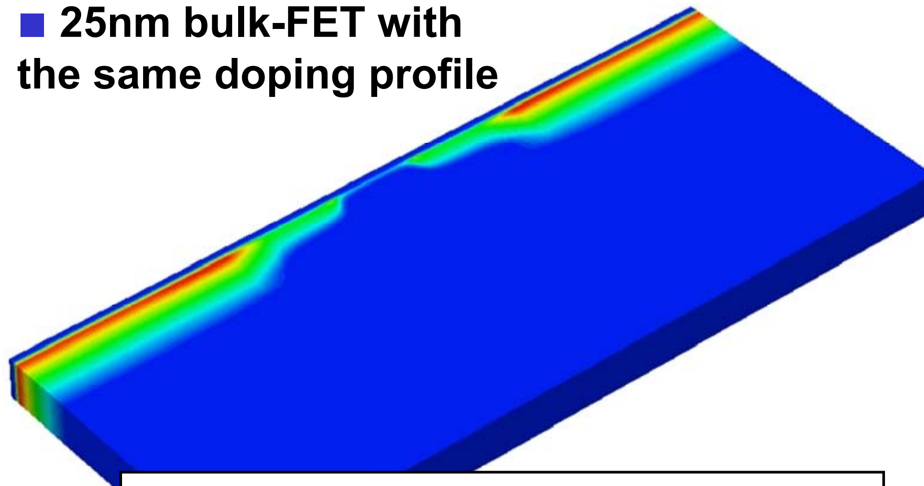


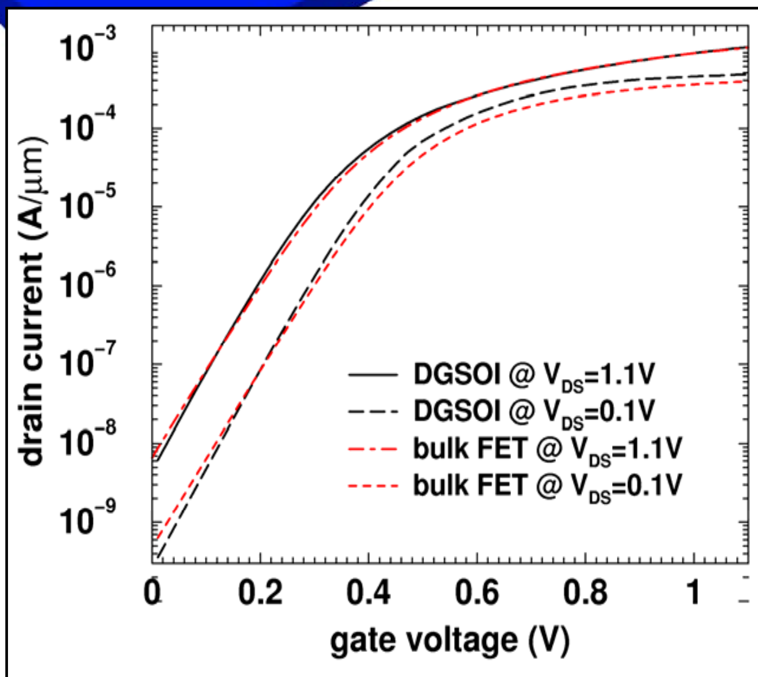


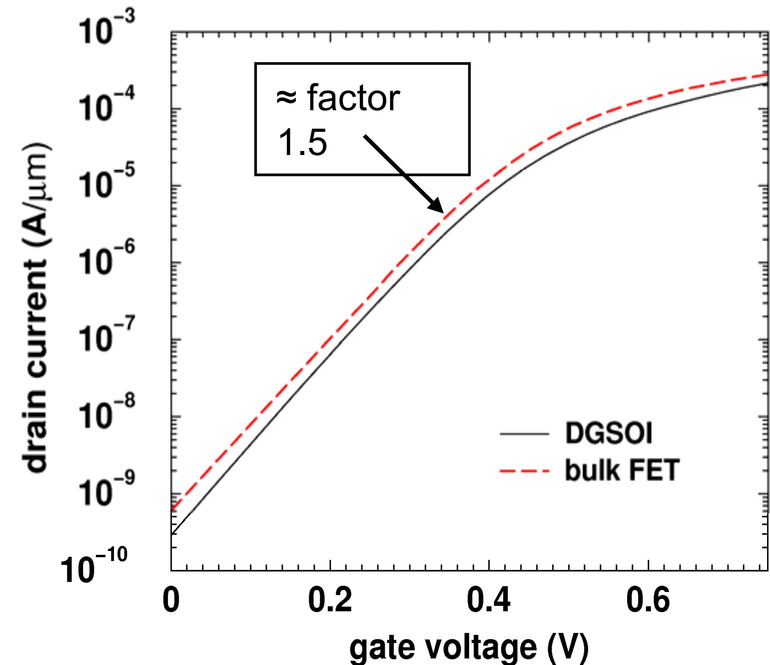
- Band edge profile and eigen-energies of the 4 lowest sub-bands at a sheet density of 10^{13} cm^{-2}

Quantum-ballistic MOSFET: bulk *vs* DGSOI (2)

- 25nm bulk-FET with the same doping profile







- Comparison of quantum-ballistic currents at low V_{DS} (for DGSOI: current per channel)

- Comparison of quantum-drift-diffusion currents (for DGSOI: current per channel)