Modeling and Simulation of SOI Devices

Andreas Schenk

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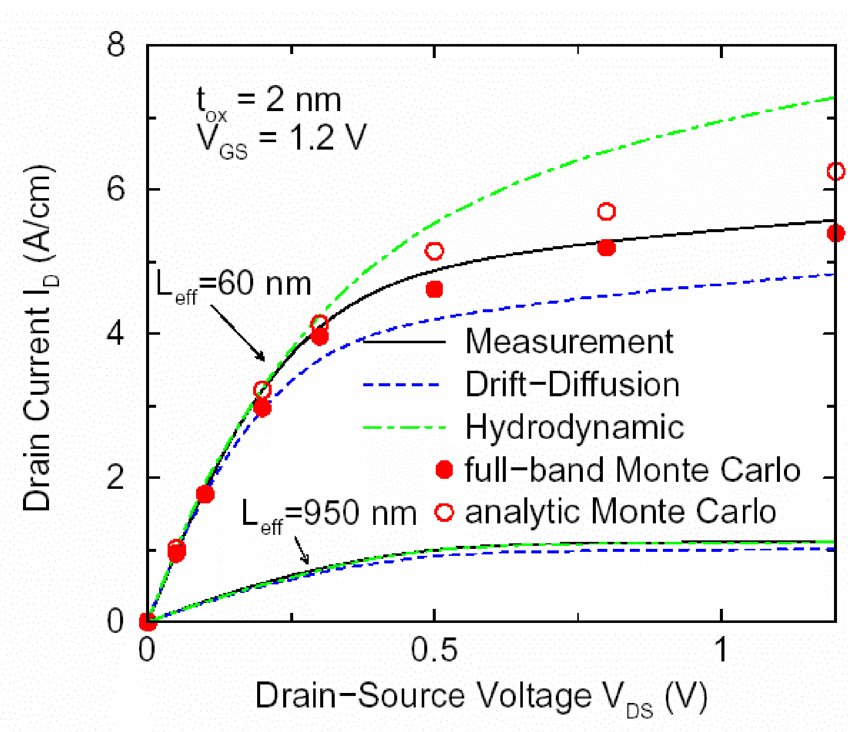
Taxonomy of simulation models

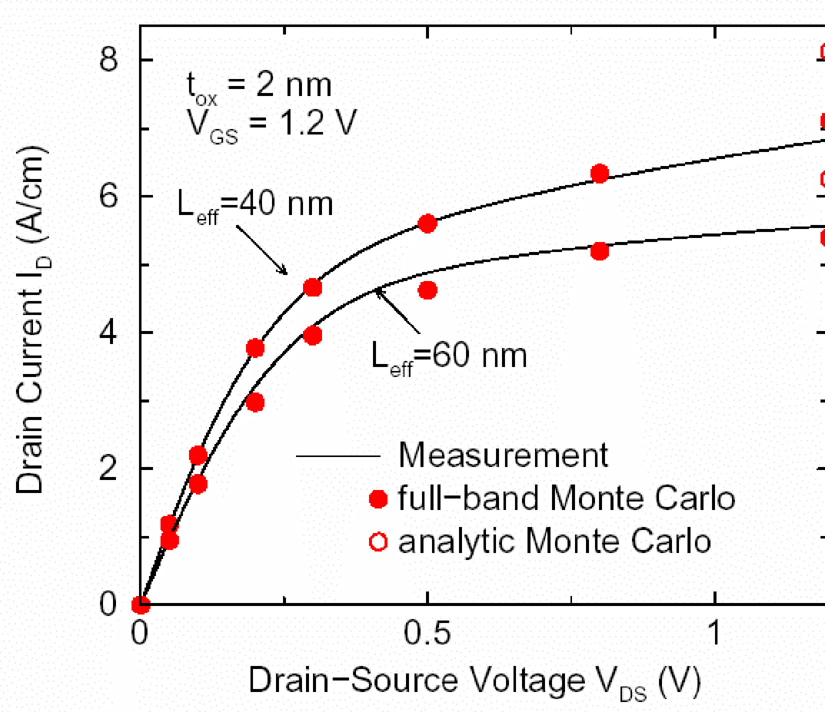
	near equilibrium dissipative	quasi–ballistic	fully ballistic
quantum mechanics	Quantum drift–diffusion	NEGF with Büttiker probes Wigner eq$^{\underline{n}}$	NEGF without $S_{scatter}$ Scattering matrix
classical mechanics	Drift–diffusion Hydro	Boltzmann eq$^{\underline{n}}$ (full band MC)	scattering free Boltzmann (analytic)

v

Output characteristics

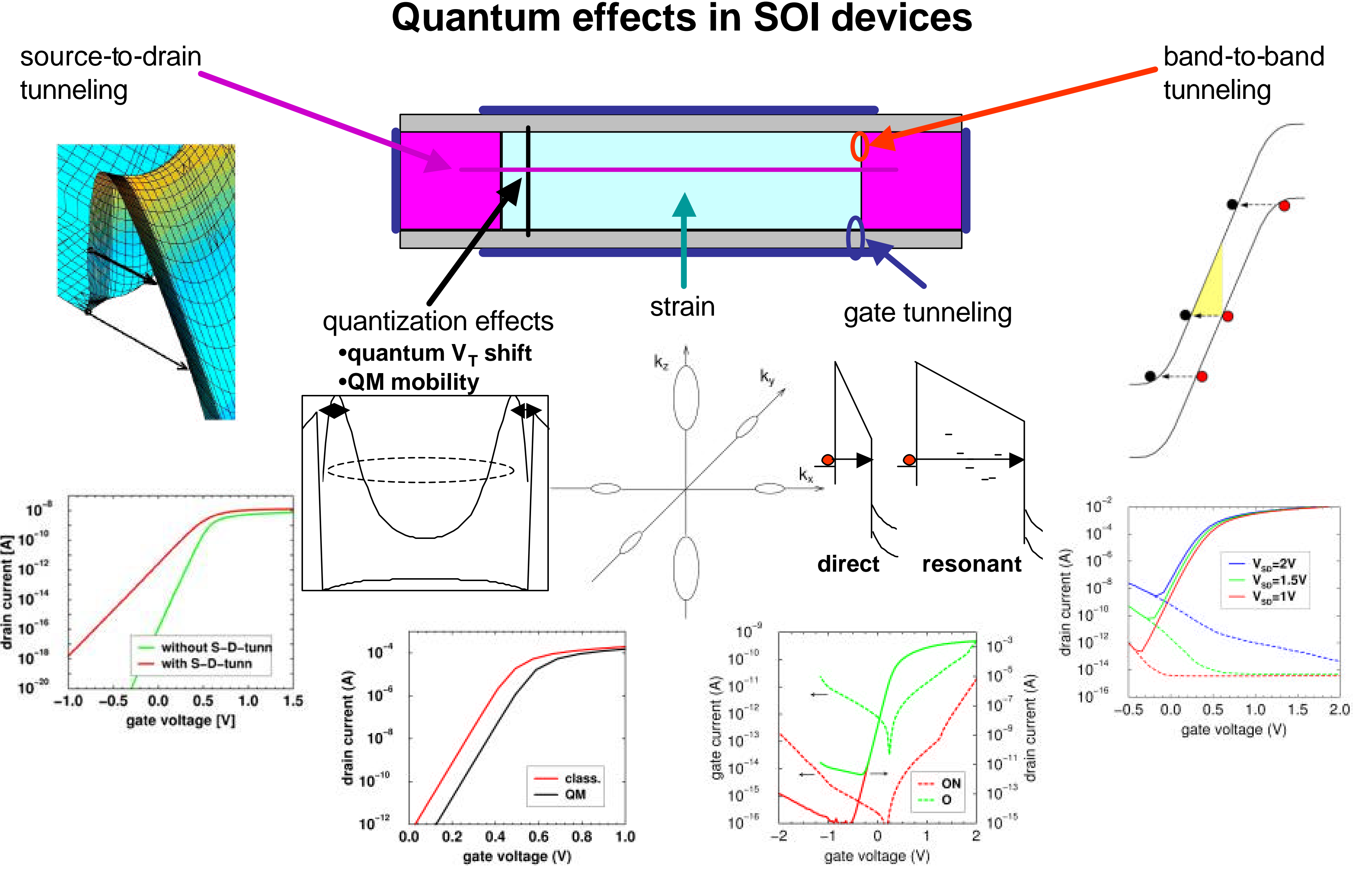


Different simulation models



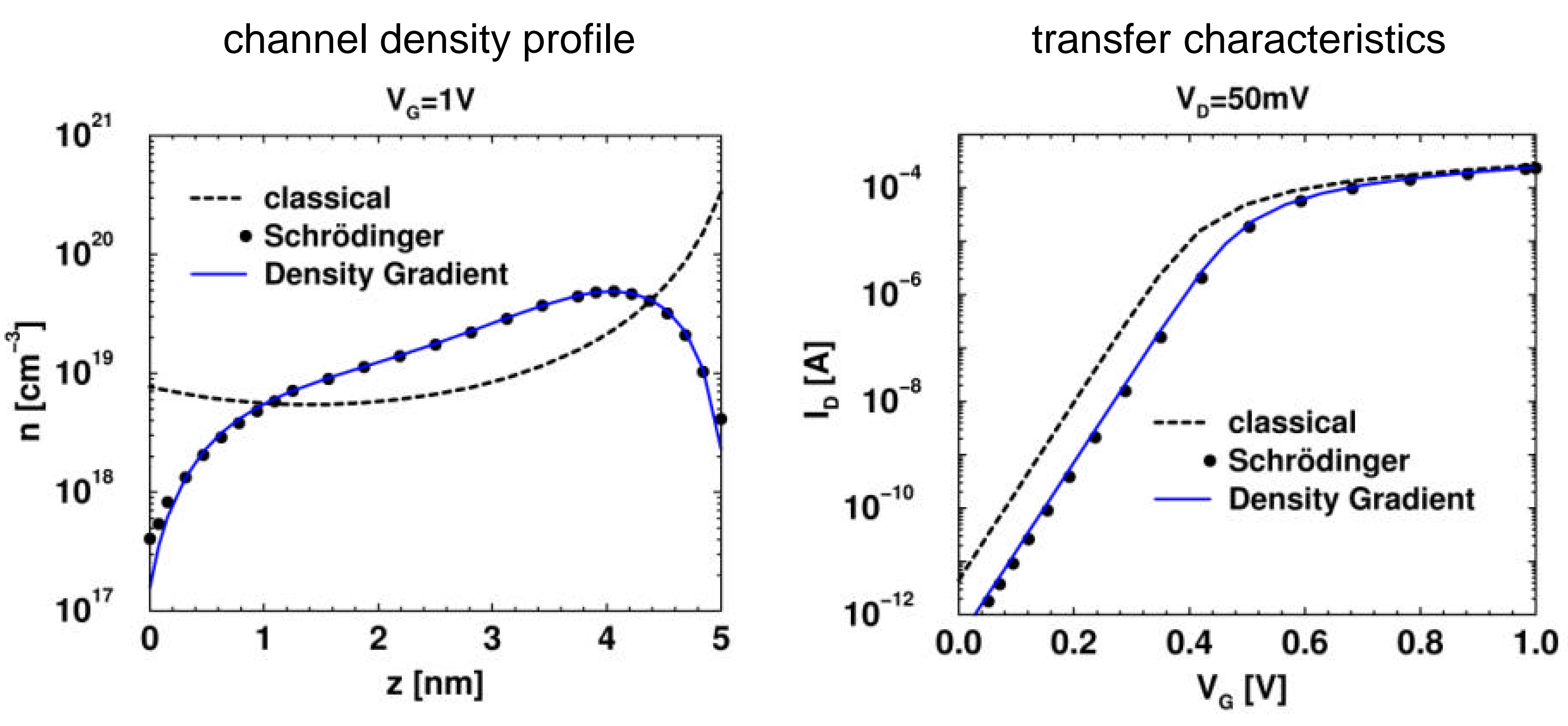
Different gate lengths

Quantum effects in SOI devices



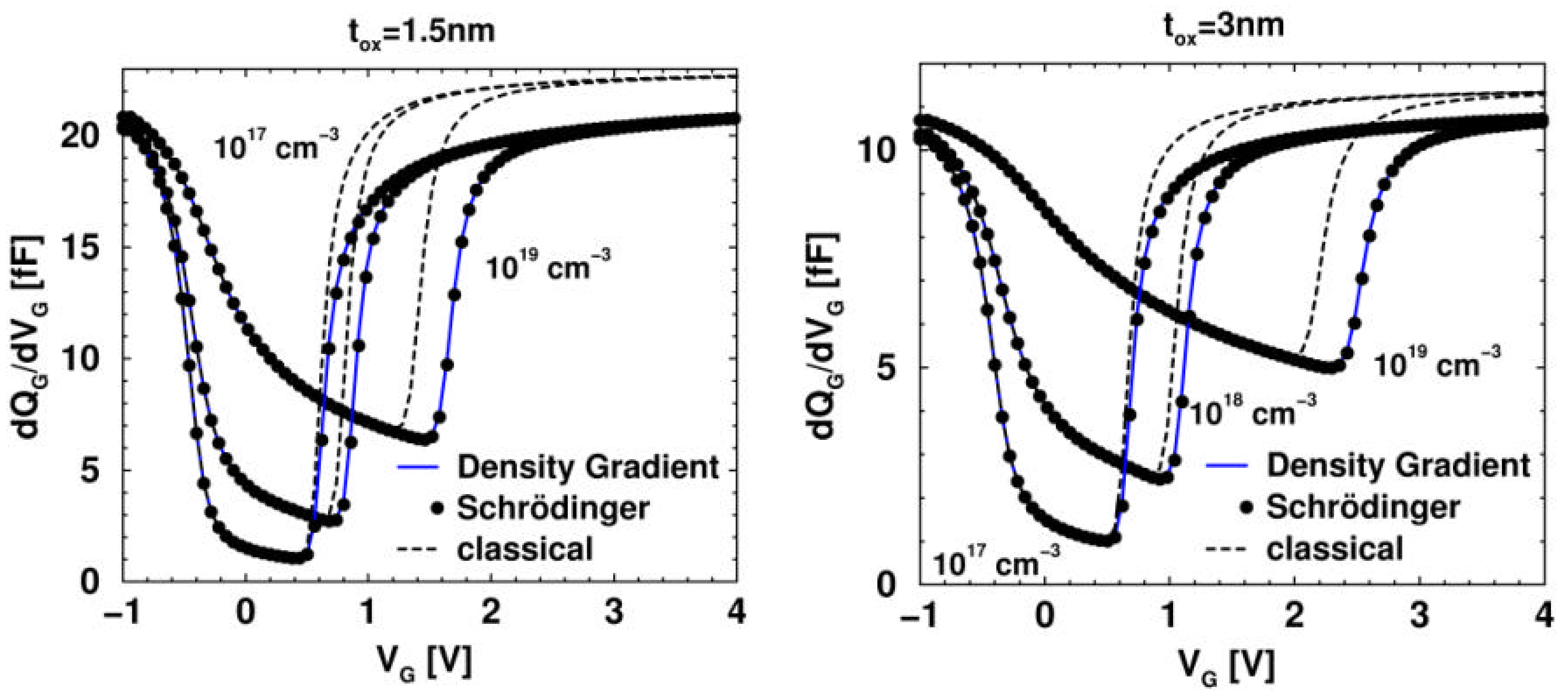
Quantum-mechanical confinement effects

Quantum V_T-shift



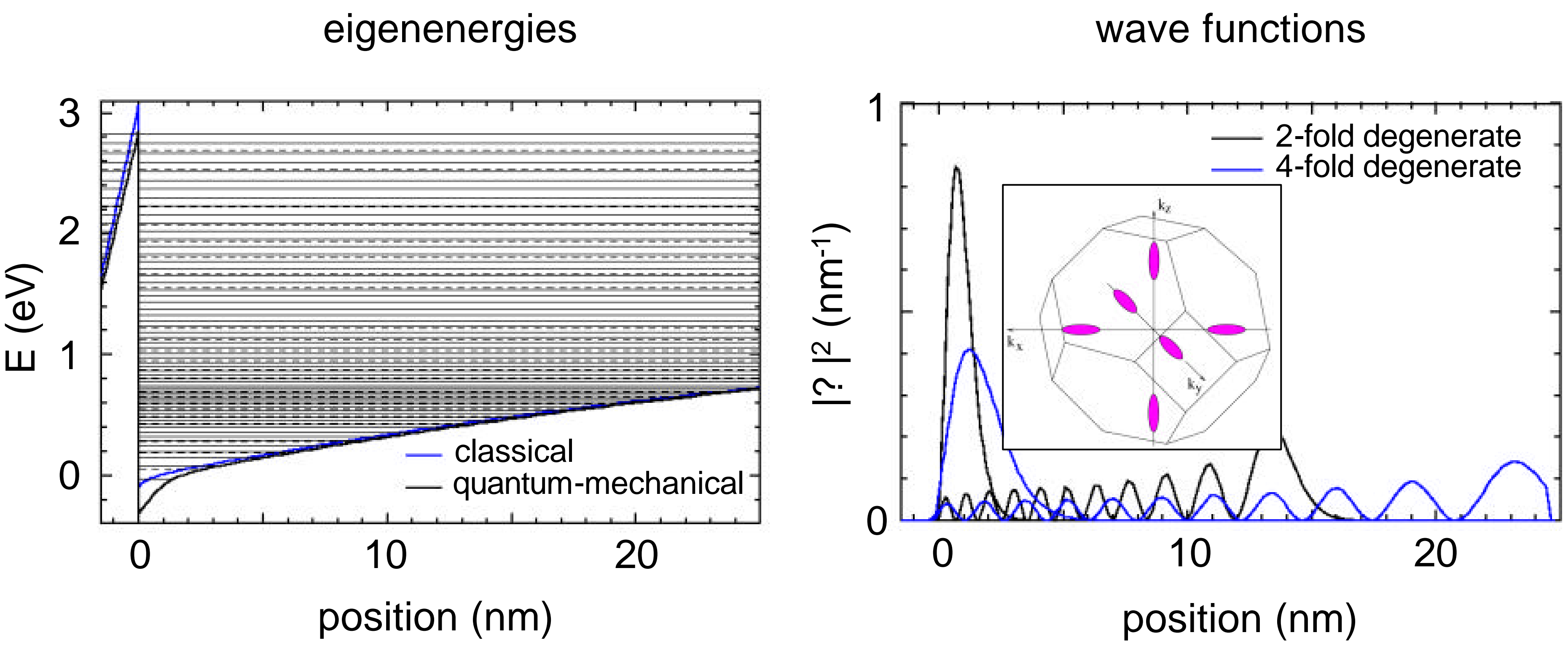
asymmetrical n^+p^+ DGSOI nMOSFET, t_{Si}=5 nm, t_{ox}=1.5 nm, L_G=90 nm

MOS (with poly) capacitor CV curves



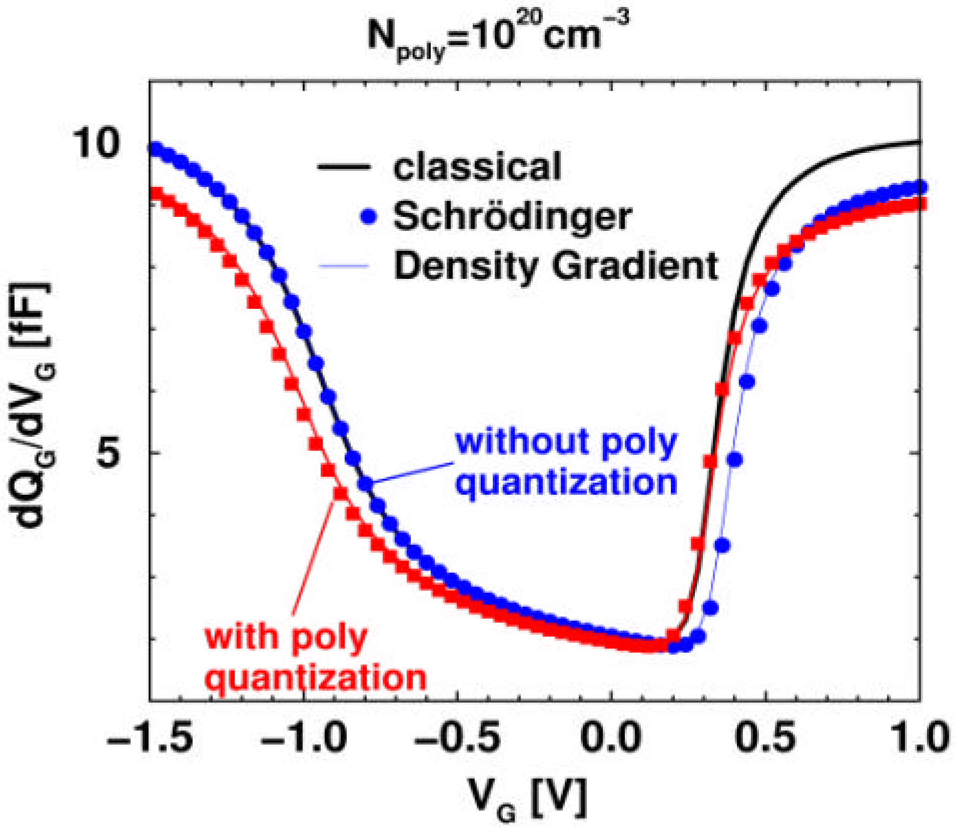
N_{poly}=1e20 cm^{-3}, A_G=1 µm^2

MOS (with poly) capacitor



N_A=5e17 cm^{-3}, t_{ox}=3 nm, V_G=3 V

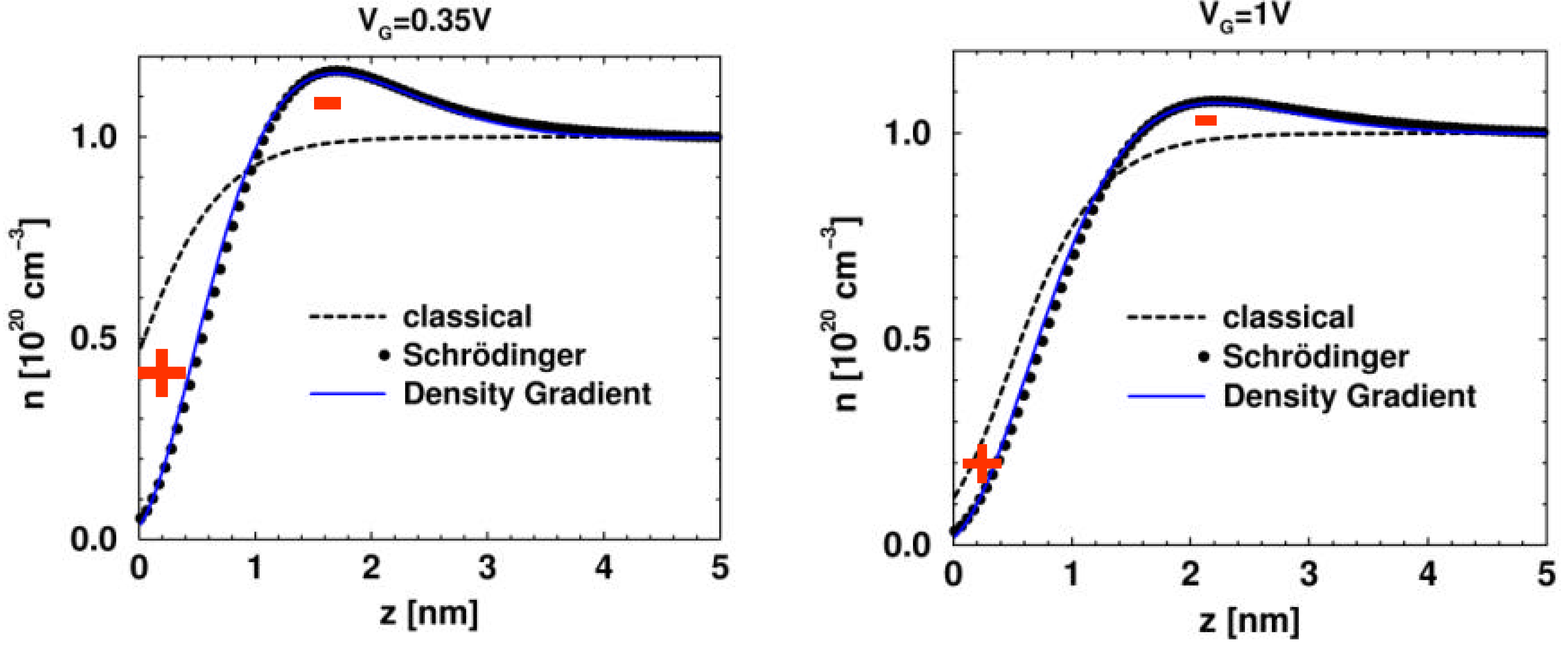
Quantum depletion at poly-SiO_2 interface



compensation of quantum shift at threshold for high poly doping (~1e20 cm^{-3})!

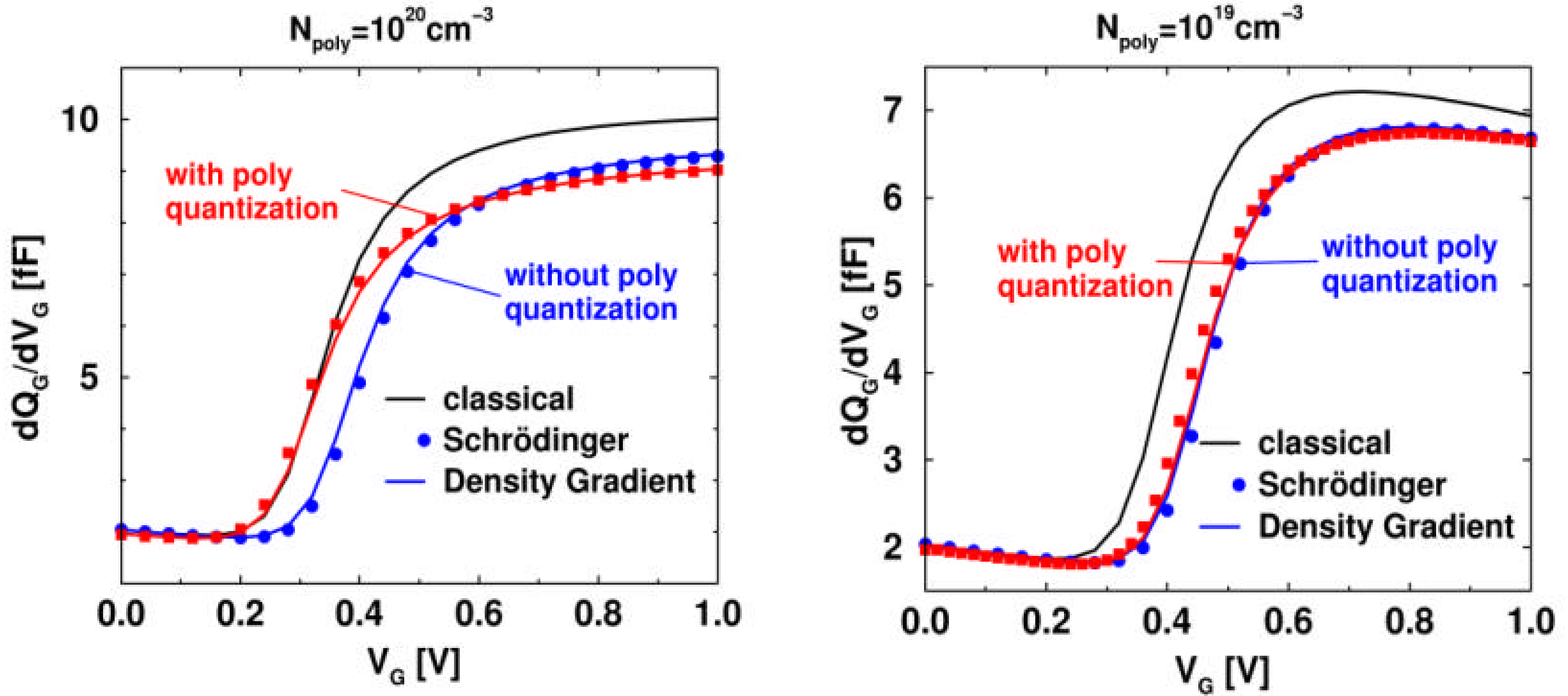
N_A=5e17 cm^{-3}, t_{ox}=3 nm, A_G=1 μm^2

Electron density profile at poly-SiO_2 interface



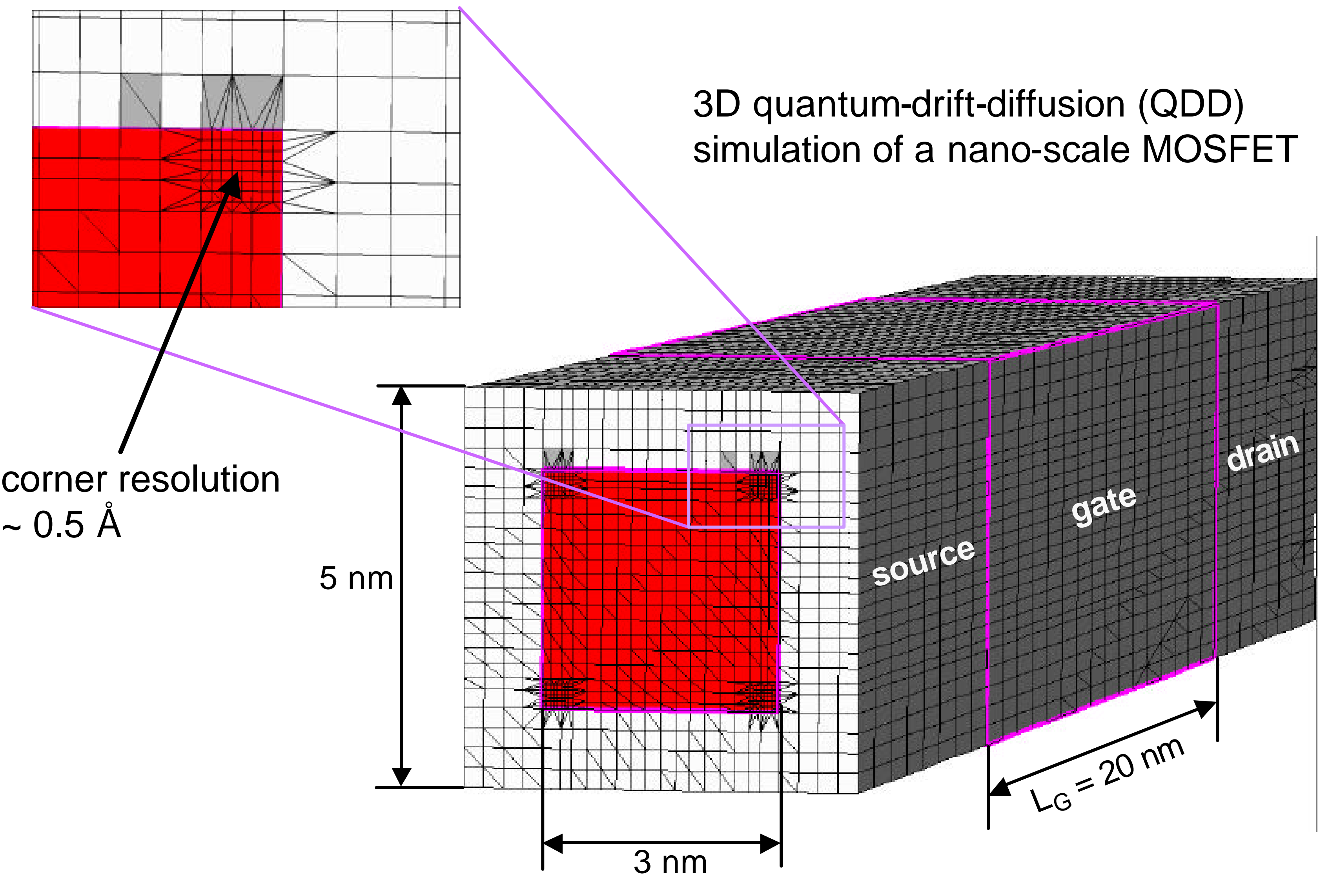
- a "quantum dipole" forms as the electron waves are repelled from the poly-SiO_2 interface
- poly quantum depletion disappears with rising V_G (smoother poly band edge curvature)

Effect on CV curves

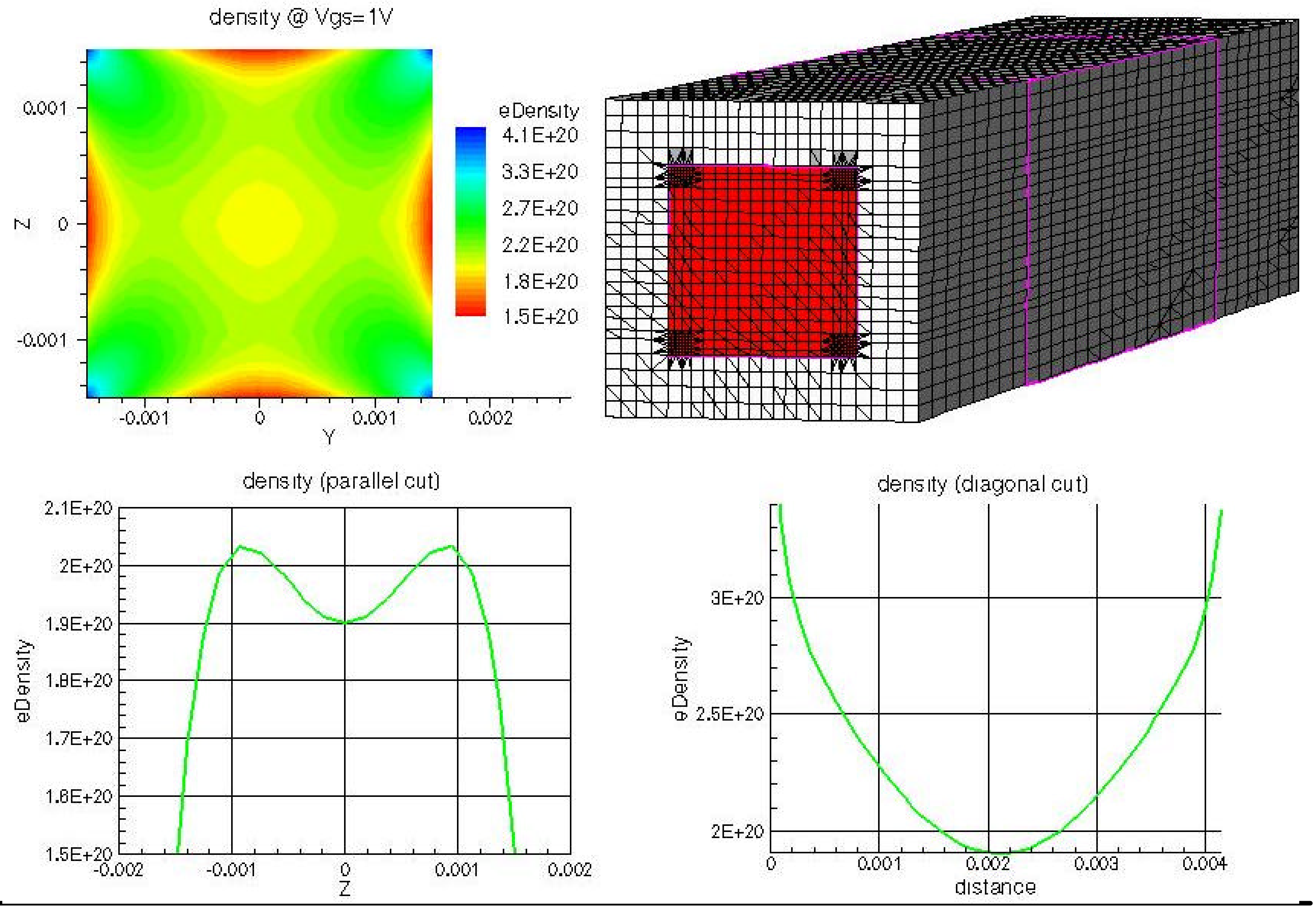


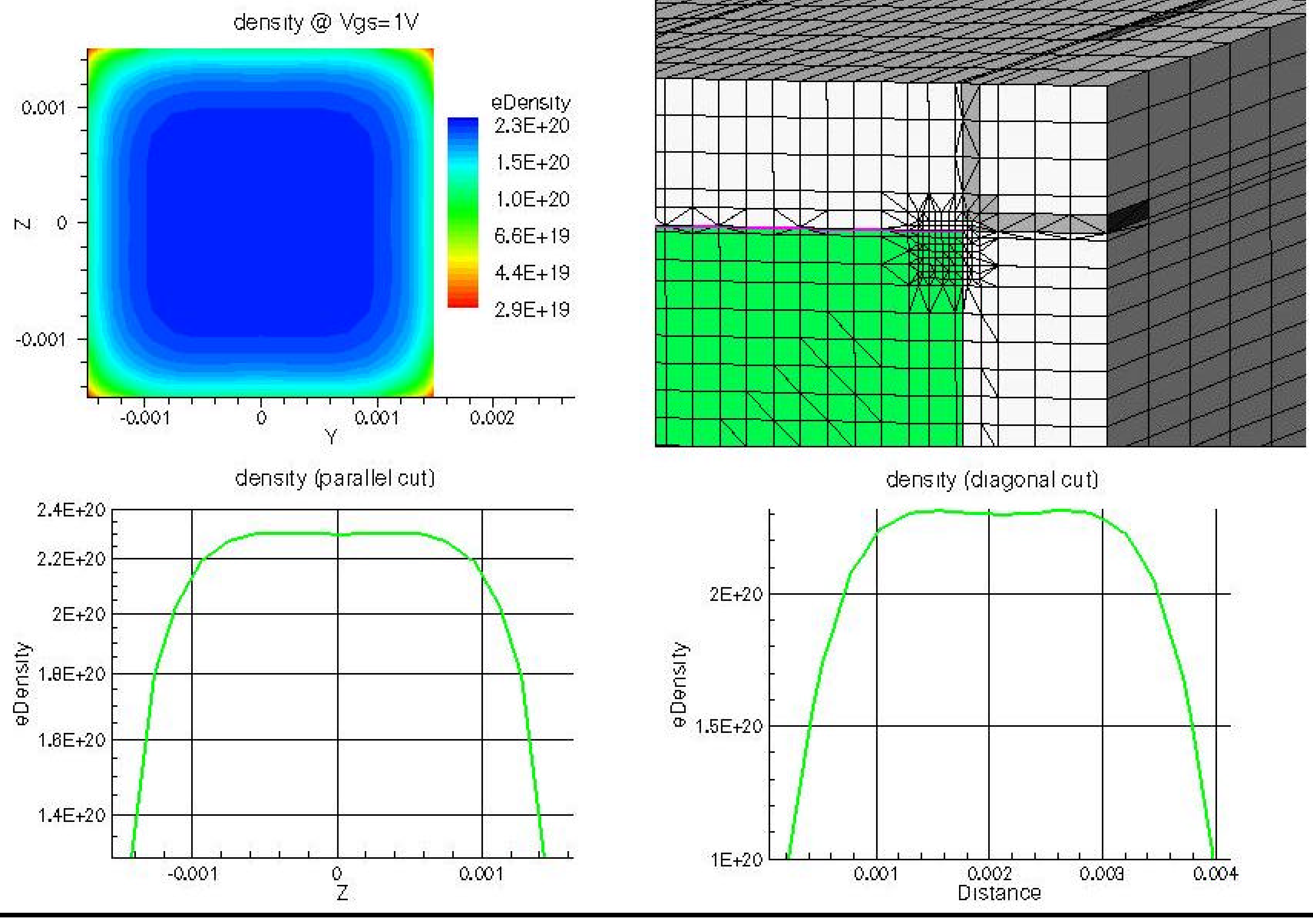
- **strength of the quantum dipole depends on doping level within the first few nanometers**
- **no effect on CV, if N_{poly} < 1e19 cm^{-3} at the interface**

Comparison single, double, triple, and surround gate

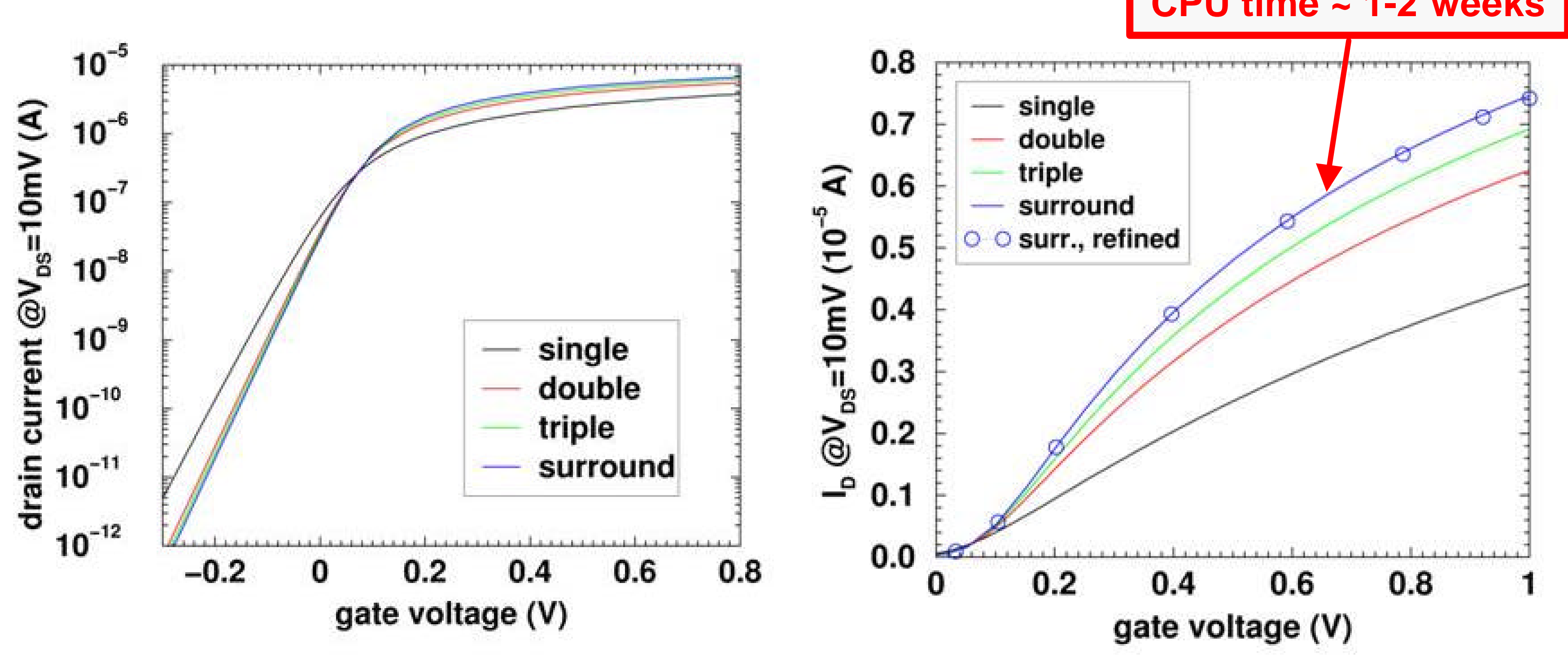


Influence of mesh refinement




density @ Vgs=1V
eDensity
2.3E+20
1.5E+20
1.0E+20
6.6E+19
4.4E+19
2.9E+19
0.001
Z 0
-0.001
-0.001
0
0.001
0.002
Y
density (parallel cut)
2.4E+20
2.2E+20
2E+20
1.8E+20
1.6E+20
1.4E+20
eDensity
-0.001
0
0.001
Z
density (diagonal cut)
2E+20
1.5E+20
1E+20
eDensity
0.001
0.002
0.003
0.004
Distance

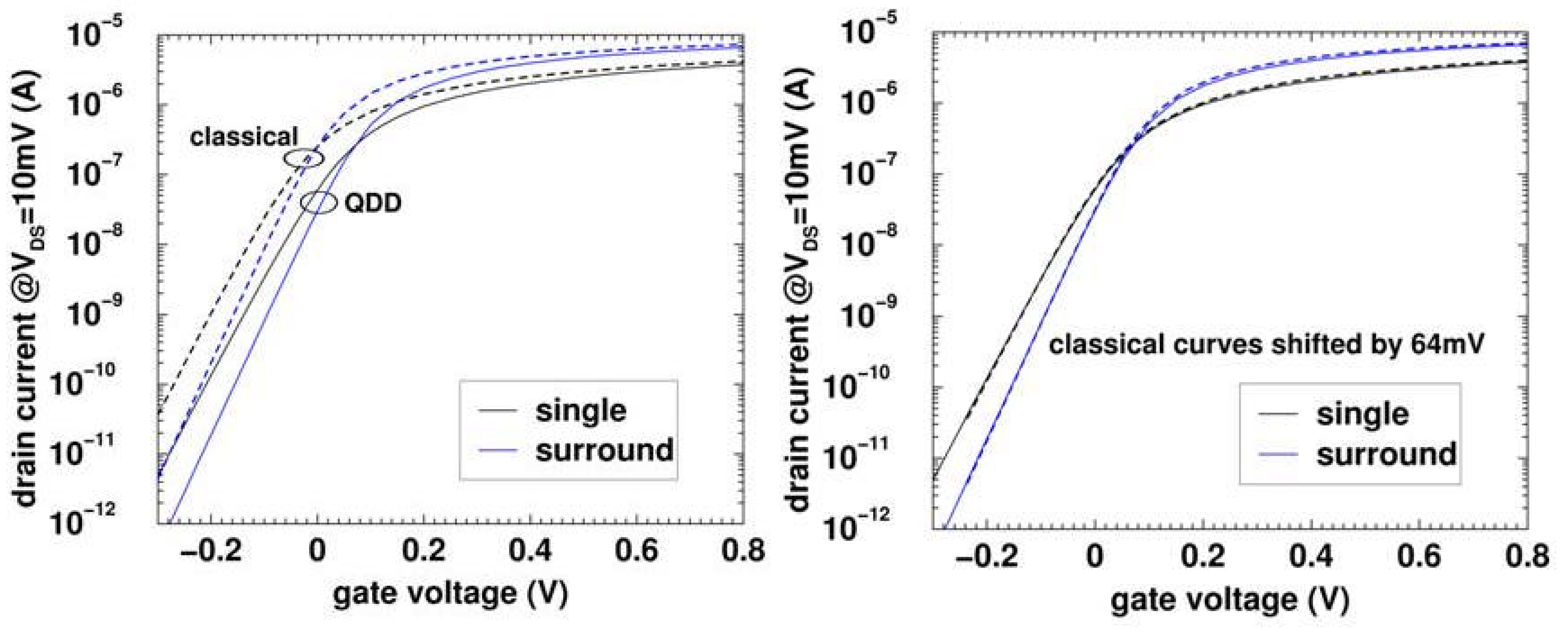
Transfer characteristics



assumption: isotropic, classical mobility

- **no corner effect (FD, no channel doping, 3x3 nm wire)**
- **only little improvement from double ? surround (gate overlap, e.g. triple gate is an effective ?-gate)**

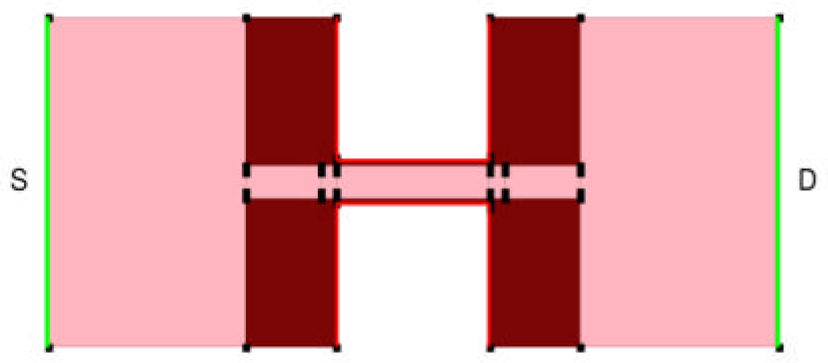
Transfer characteristics (contd.)



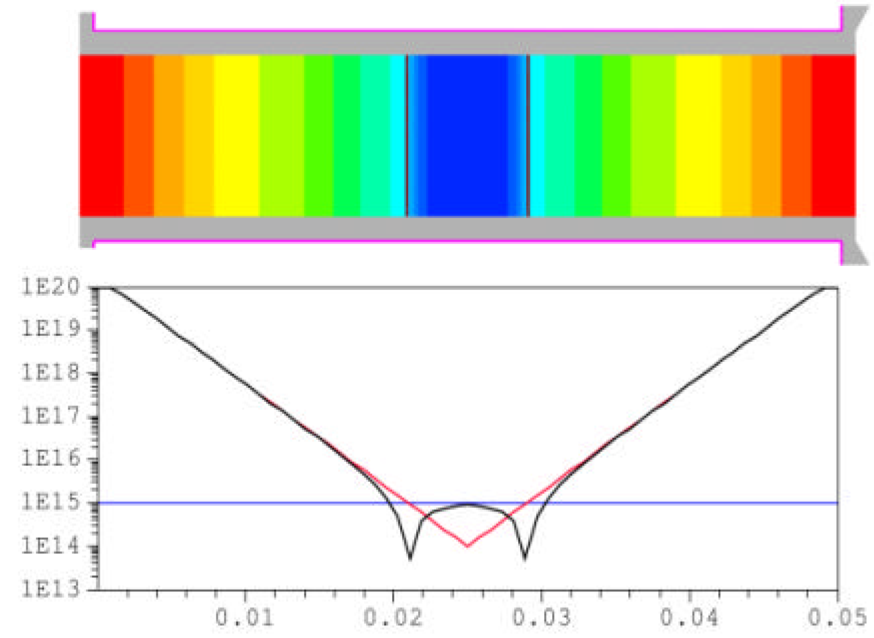
- quantum V_T-shift of ~ 64 mV, independent of gate configuration
- almost perfect shift on V_{GS}-axis ? quantum V_T-shift can be translated into work function difference

Quantum-mechanical mobility in DG SOI MOSFETs

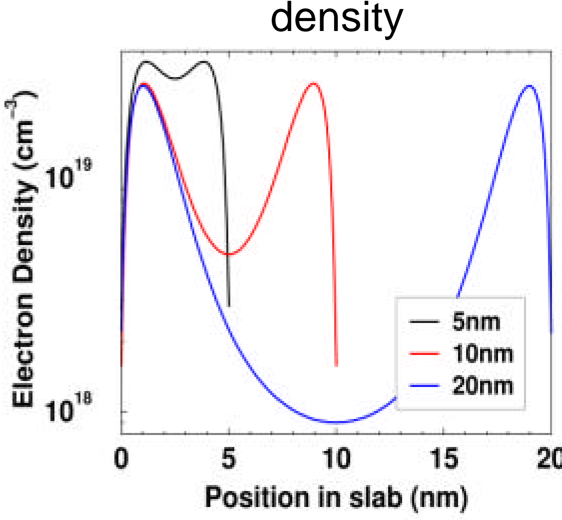
"FINFET" with L_G=50 nm

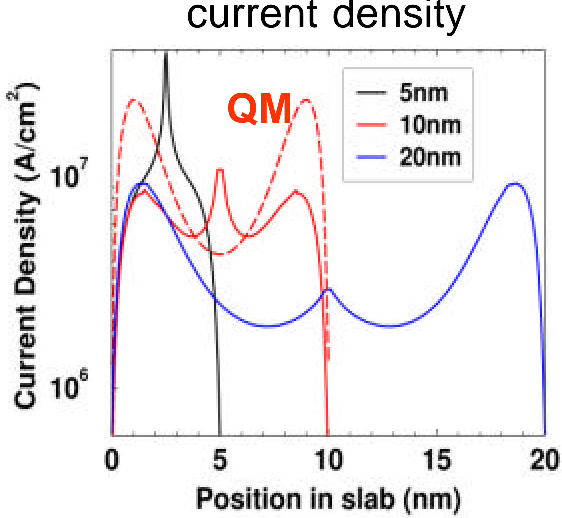


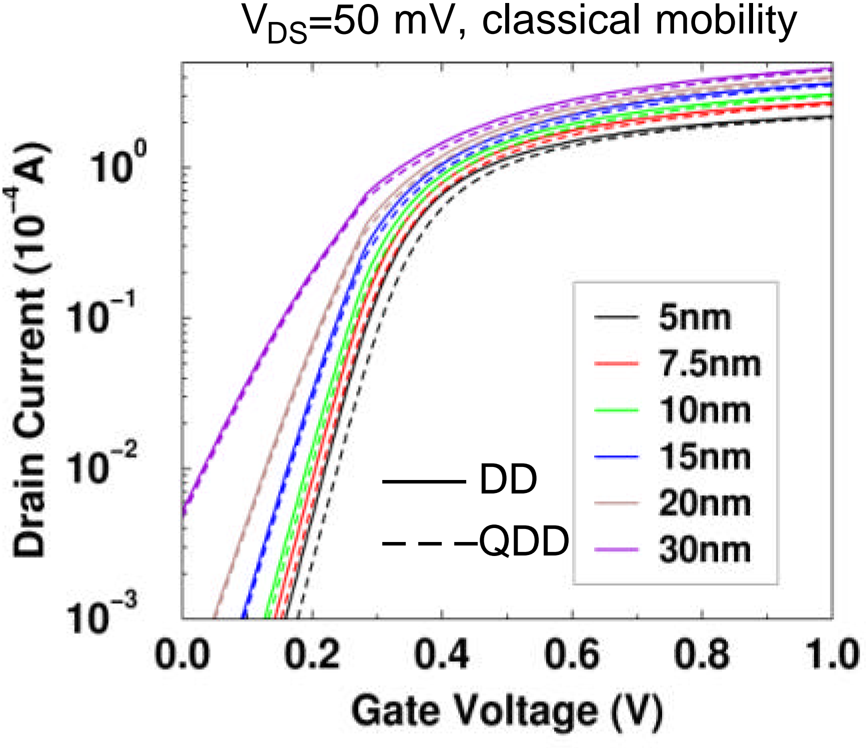
P. M. Solomon and S. E. Laux, Proc. IEDM 2001, pp. 95-98



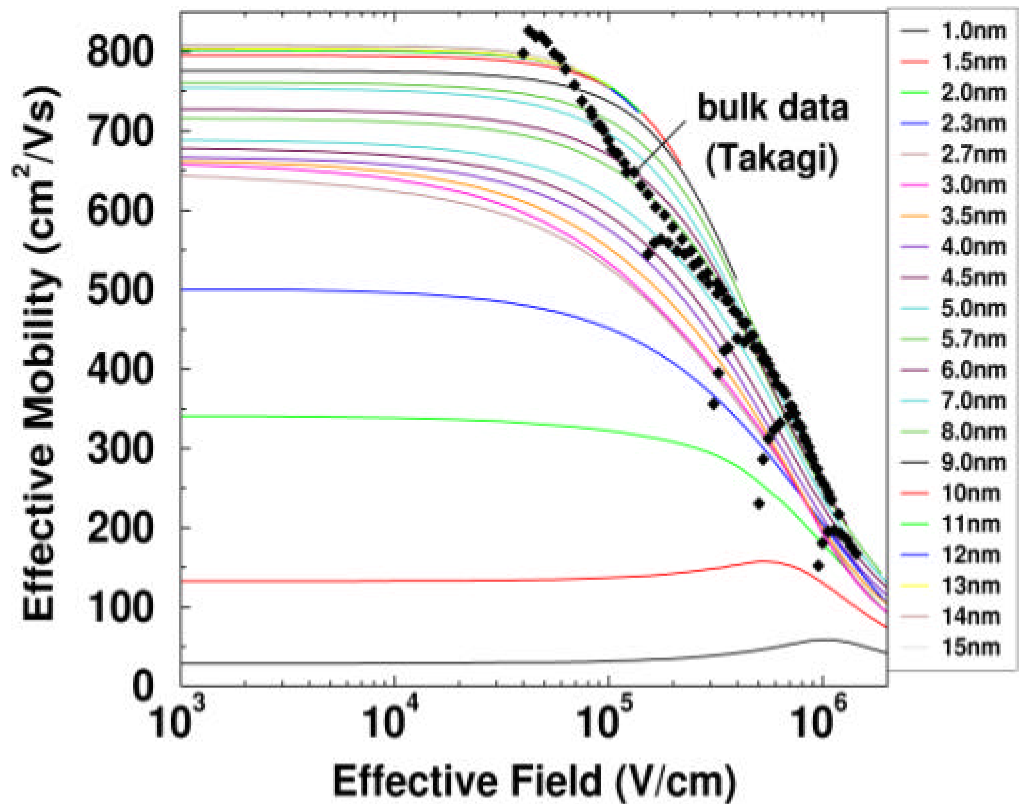
- doping gradient = 1 decade over 4 nm
- distance between pn-junctions = 8 nm
- length of source-drain barrier = 43 nm
- gate overlap = 21 nm







- **degradation of slope for t_{Si} > 12 nm (4:1 rule violated)**
- **QM V_T-shift increases with decreasing slab thickness (stronger confinement)**



QM mobility model

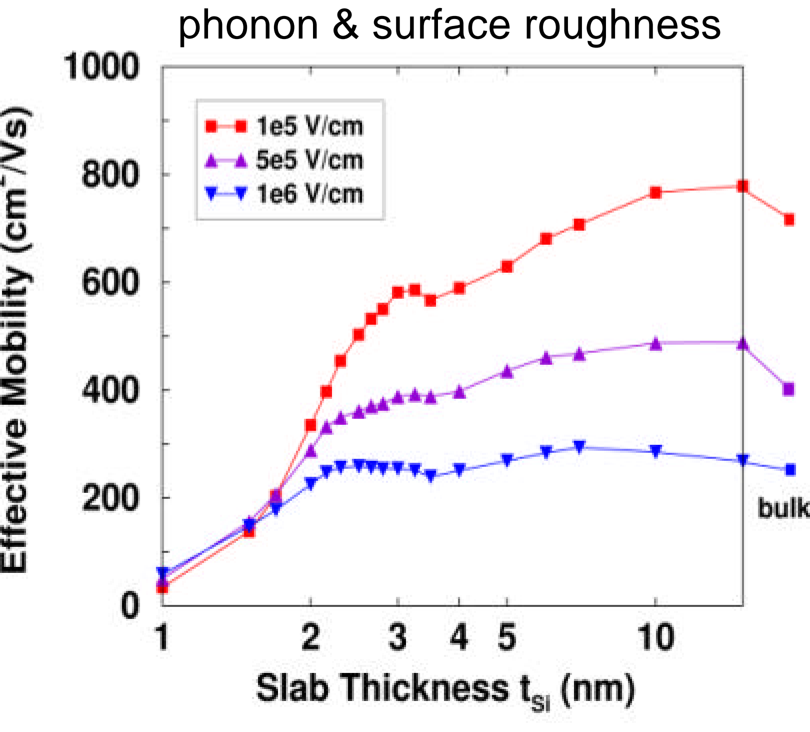
phonon & surface roughness scattering yields $\mu_{eff}(E_{eff})$ as function of T, t_{Si}, t_{ox}, t_{box}

Coulomb scattering (roll-off) in channel, remote, and interface under development

Quantity	Front Interface	Back Interface
?	0.32 nm	0.32 nm
L_{corr}	1.5 nm	1.5 nm

only phonon scattering

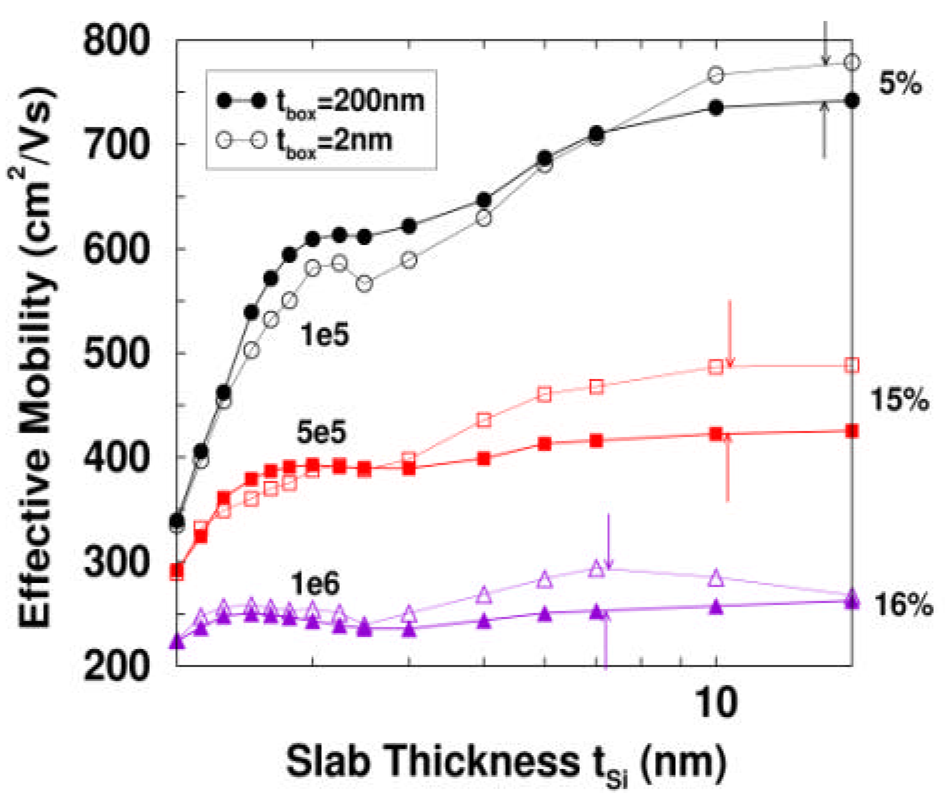
1000
800
600
400
200
0
Effective Mobility (cm^2/Vs)
1 2 3 4 5 10
Slab Thickness t_{Si} (nm)
1e3 V/cm
1e5 V/cm
5e5 V/cm
1e6 V/cm
bulk



- **broad local maxima at t_{Si} ~ 10 nm caused by volume inversion**
- **reason: reduction of form factors $a_{N'N}=\int dz\,|\psi_{N'}(z)|^2\,|\psi_N(z)|^2$**
- **peaks at t_{Si} ~ 2 nm due to valley splitting, population, and form factor effects**

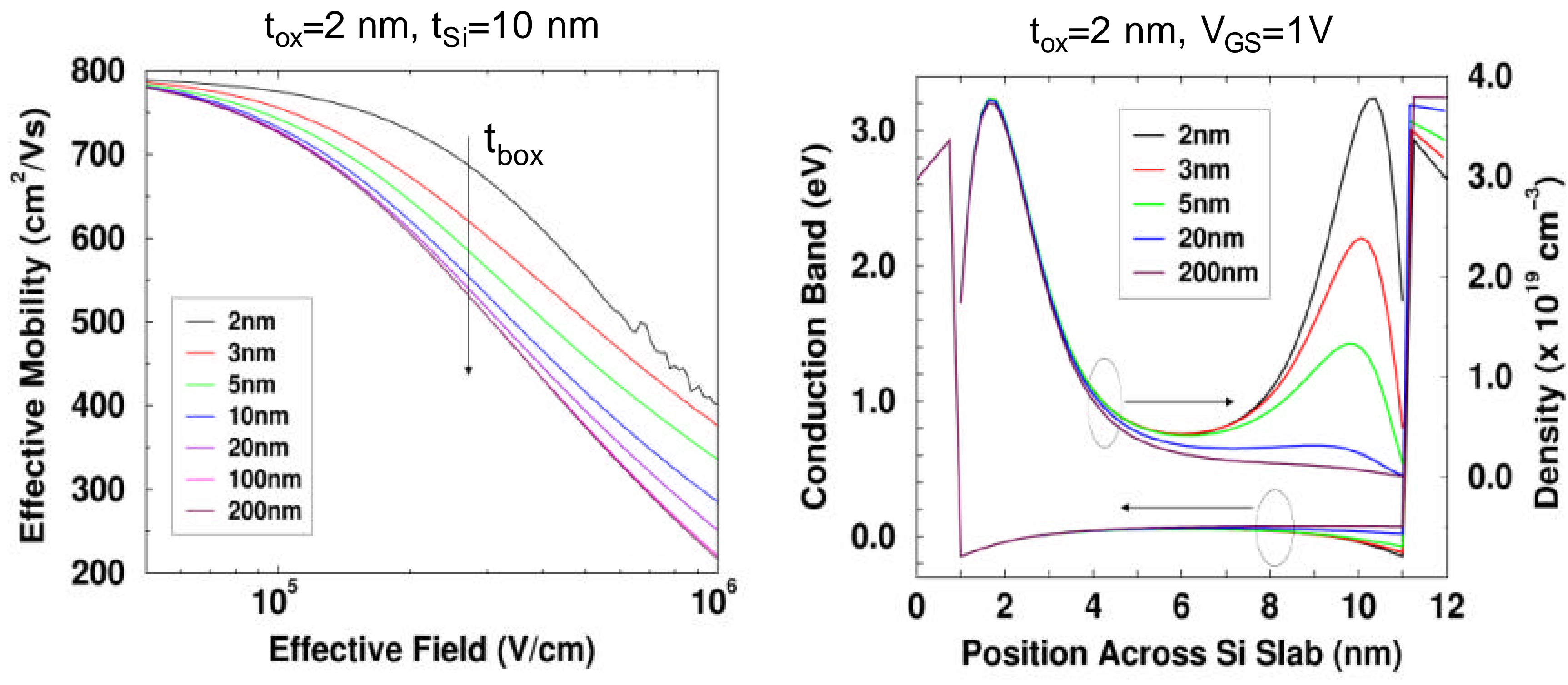
- **mobility enhancement around t_{Si} ~ 10 nm survives**
- **surface-roughness scattering flattens the curves**
- **mobility independent of E_{eff} for t_{Si}<2 nm**

Comparison between FINFET and FD DGSOI with t_{box}=200 nm



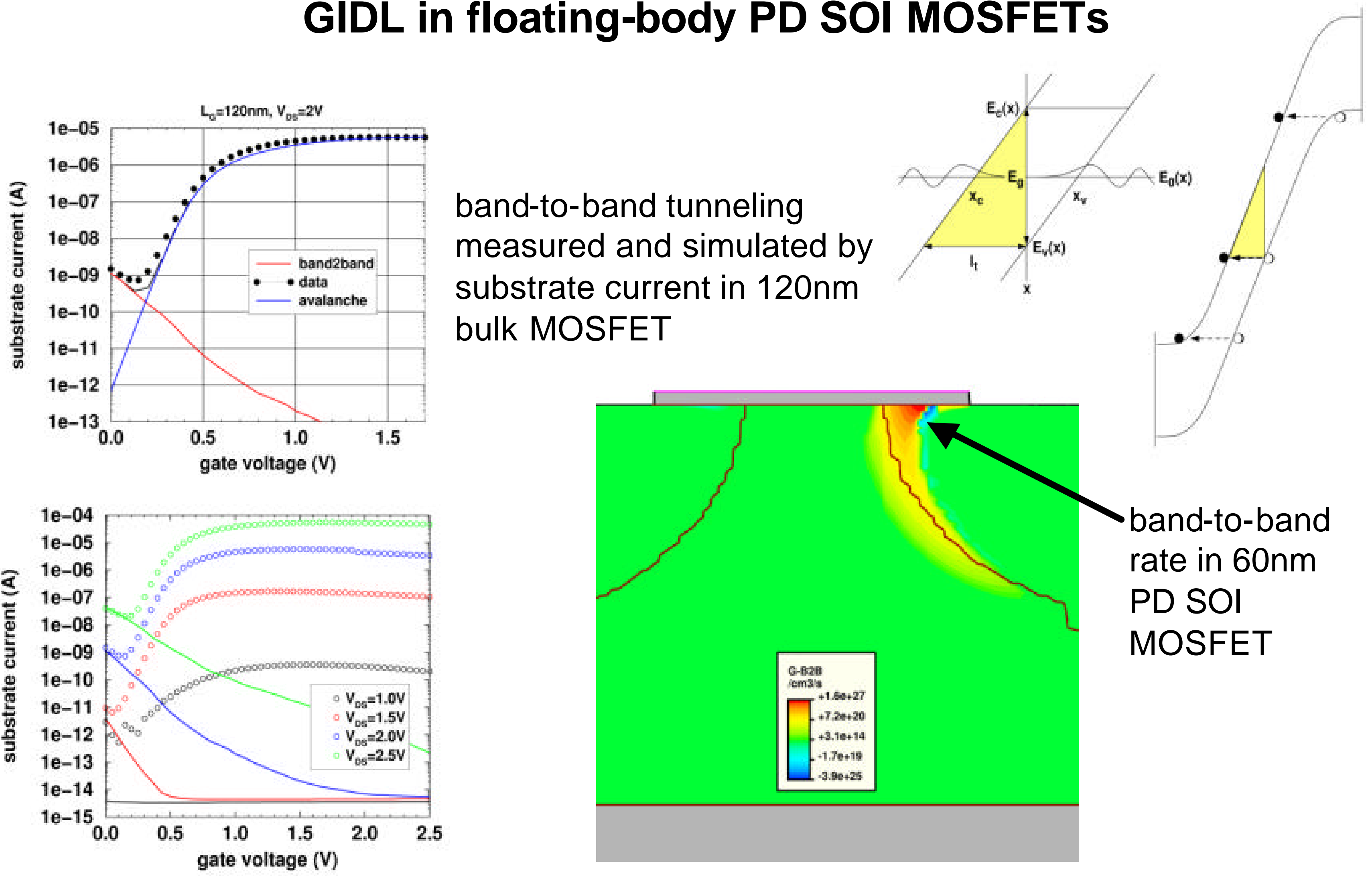
- **mobility enhancement in FINFETs amounts to 15% at E_{eff}=5x10^{5} V/cm (depending on S-R scattering parameters)**
- **no enhancement in FD DGSOI**
- **FD DGSOI is almost identical to single-gate SOI MOSFETs**

Dependence of effective mobility on t_{box}

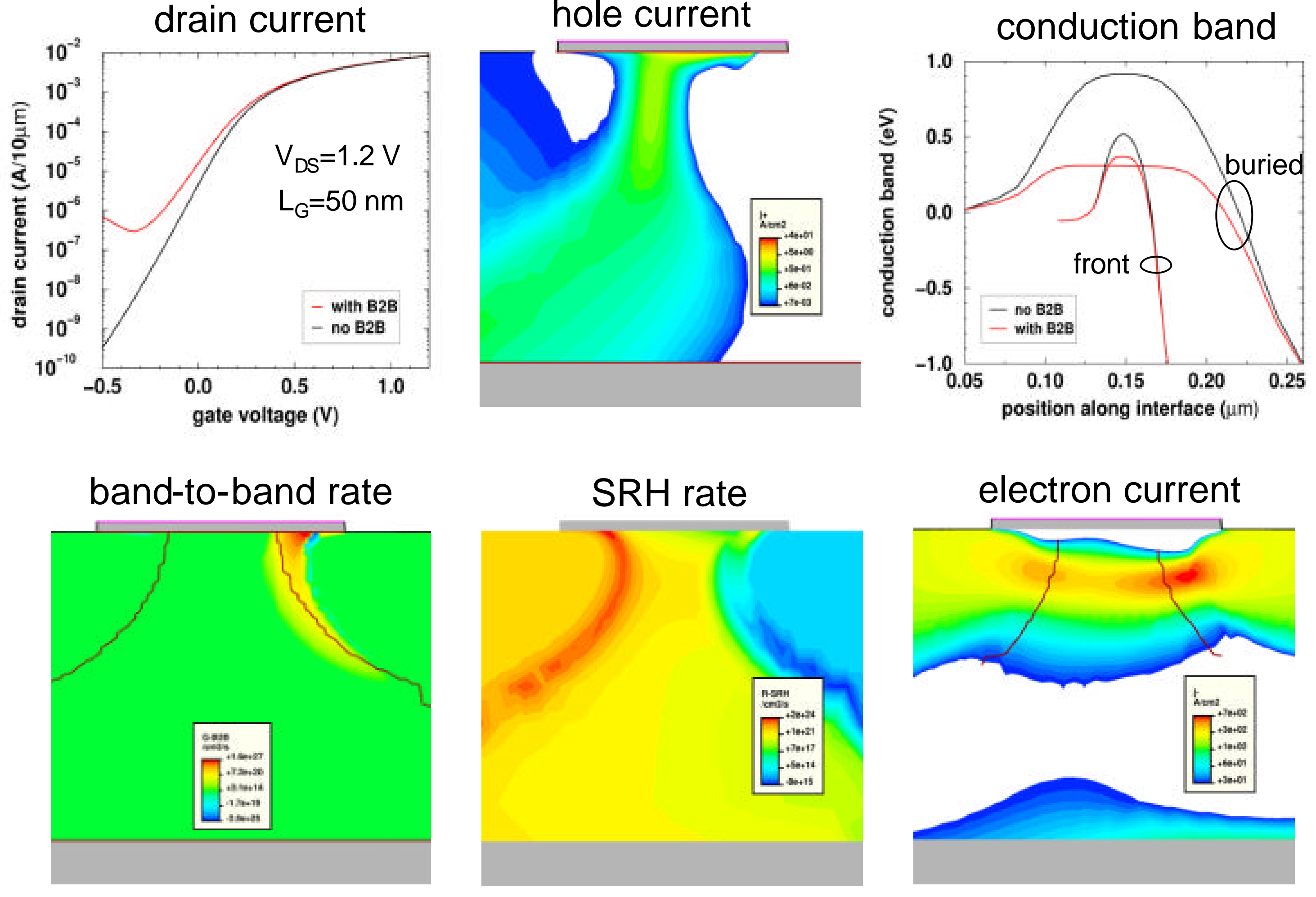


- **decrease of effective mobility towards bulk value with increasing t_{box}**
- **two equally filled channels are precondition for enhancement**
- **density of upper channel almost unaffected by an increase of t_{box}**

Tunnel generation in the drain-body junction

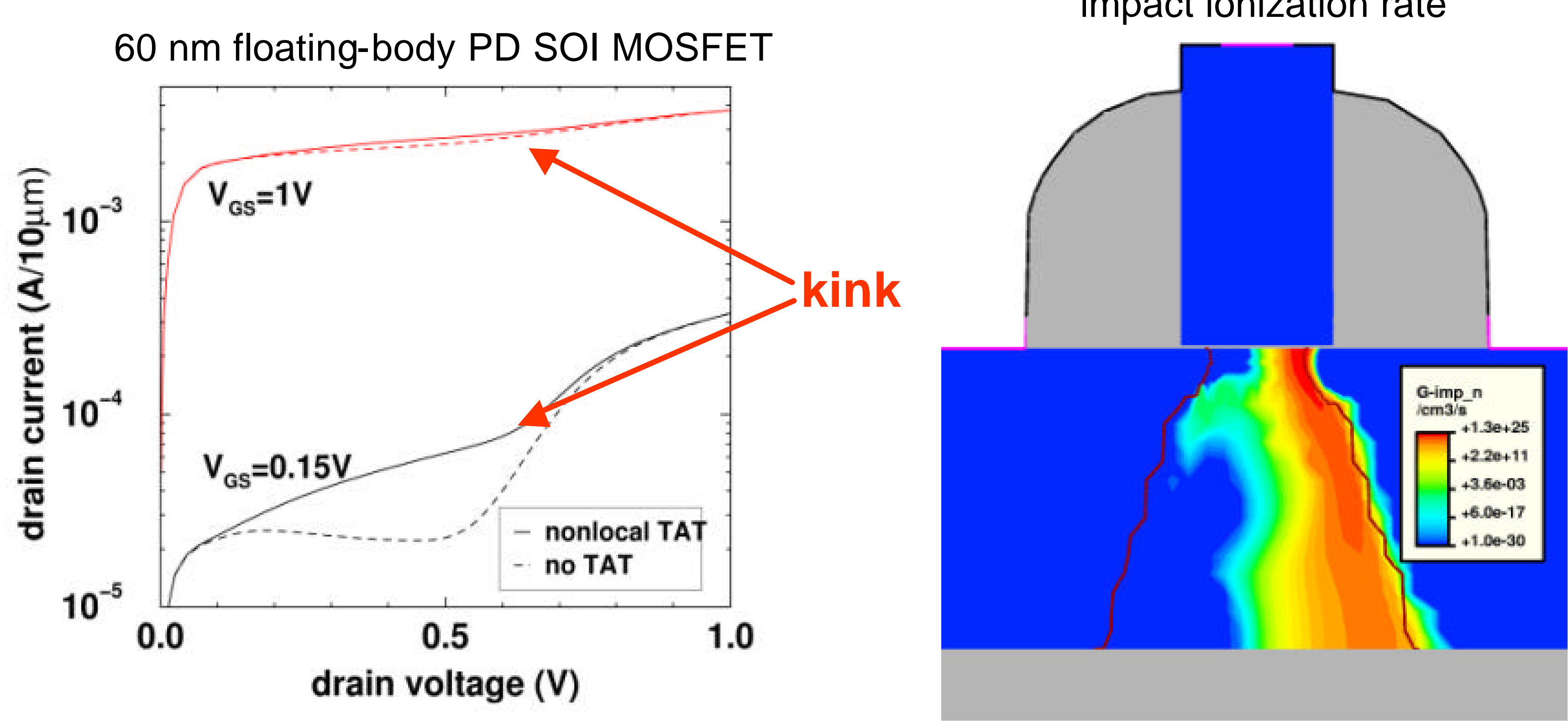


Floating-body PD SOI MOSFETs: where does the GIDL current go to?



band-to-band rate acts like base current in a parasitic bipolar!

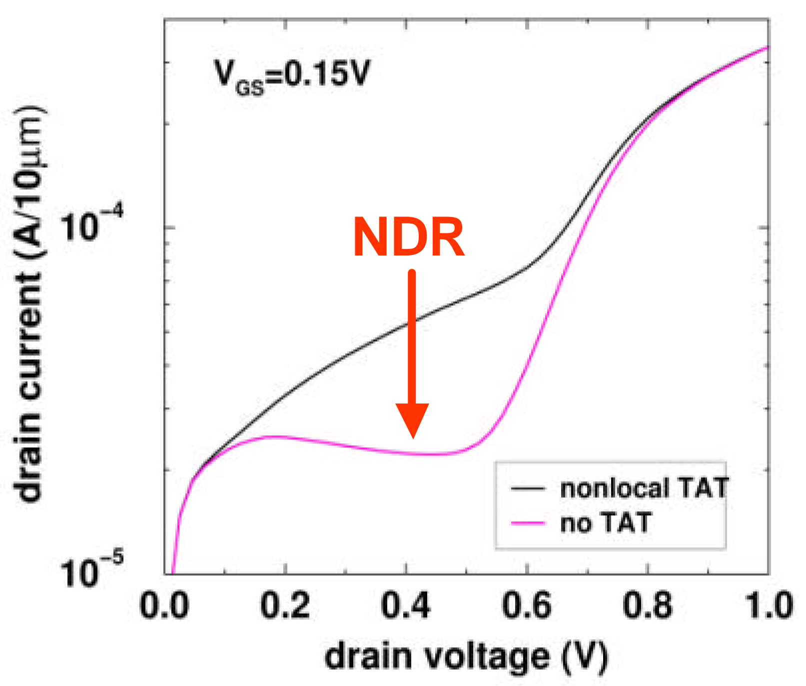
Trap-assisted tunneling and the kink effect in PD SOI MOSFETs



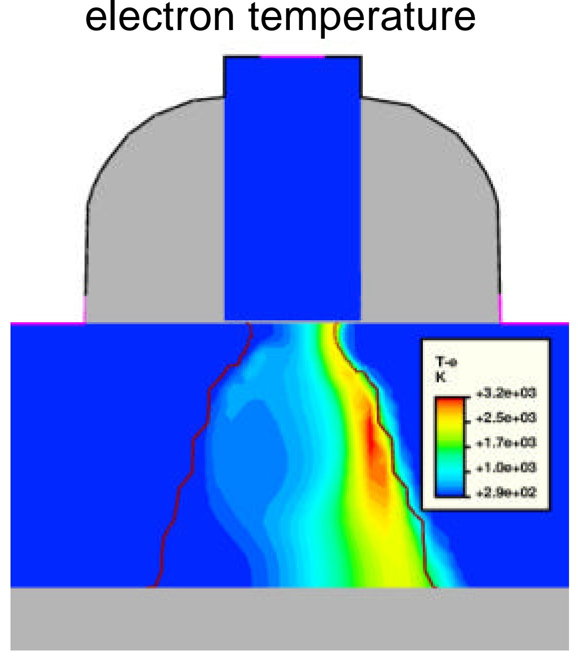
- **generated holes lower the body potential (in eV)**

? drain current increases

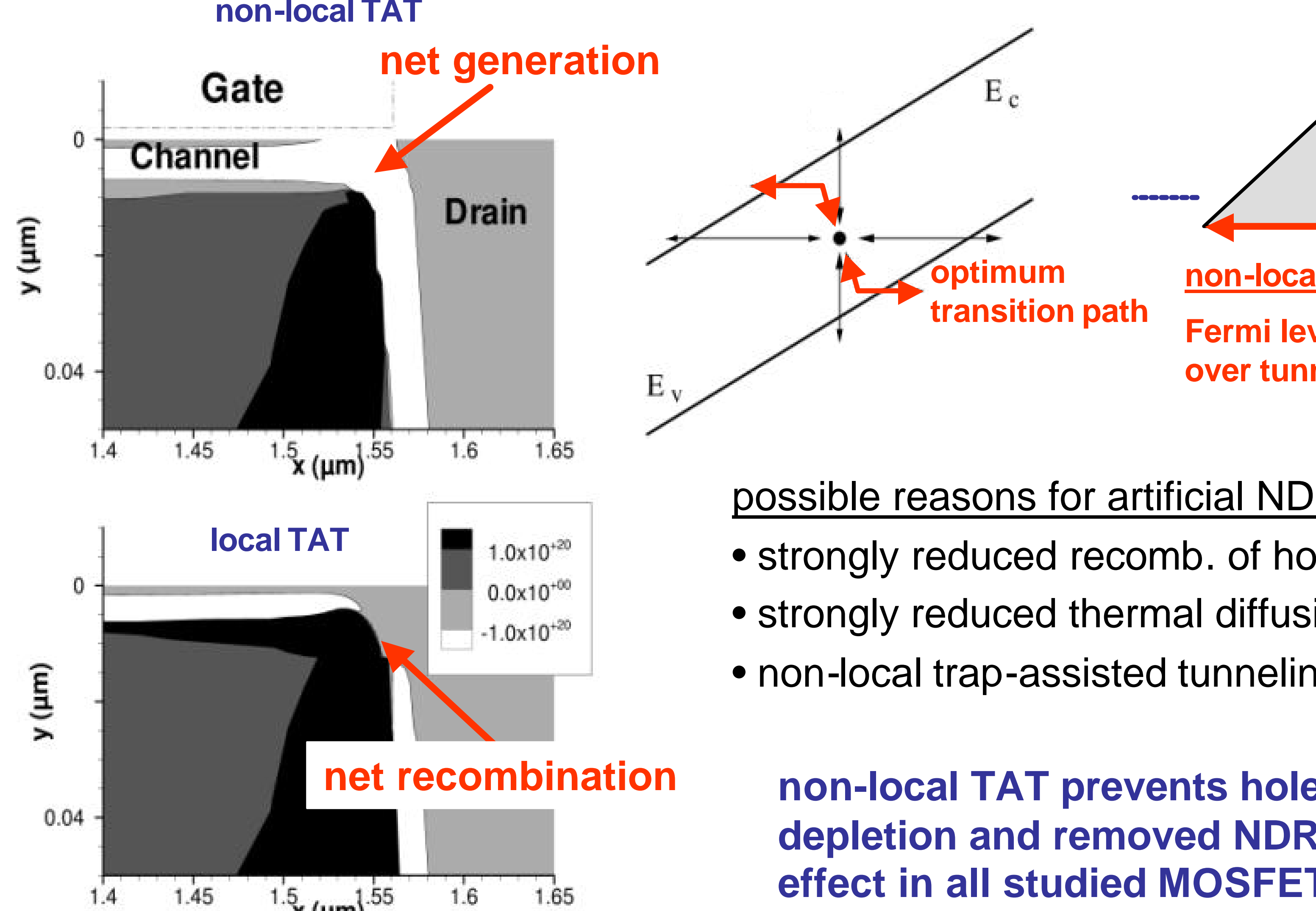
Artificial NDR effect in floating-body SOI MOSFETs by “hydrodynamic” simulation



electron temperature



- hot electrons diffuse (~?T_n/?r) into the body and recombine with holes
- the potential (in eV) increases ? drain current decreases
- impact ionization generates holes which remove hole depletion in the body ? the potential decreases ? drain current increases (kink effect)



possible reasons for artificial NDR

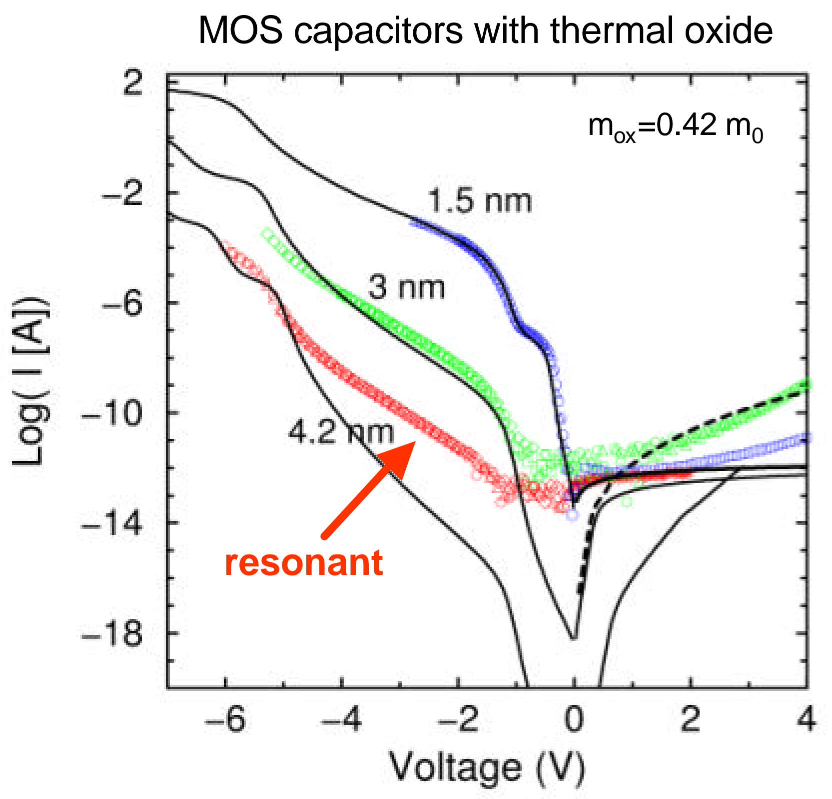
- strongly reduced recomb. of hot carriers
- strongly reduced thermal diffusion
- non-local trap-assisted tunneling

non-local TAT prevents hole depletion and removed NDR effect in all studied MOSFETs!

Gate tunneling

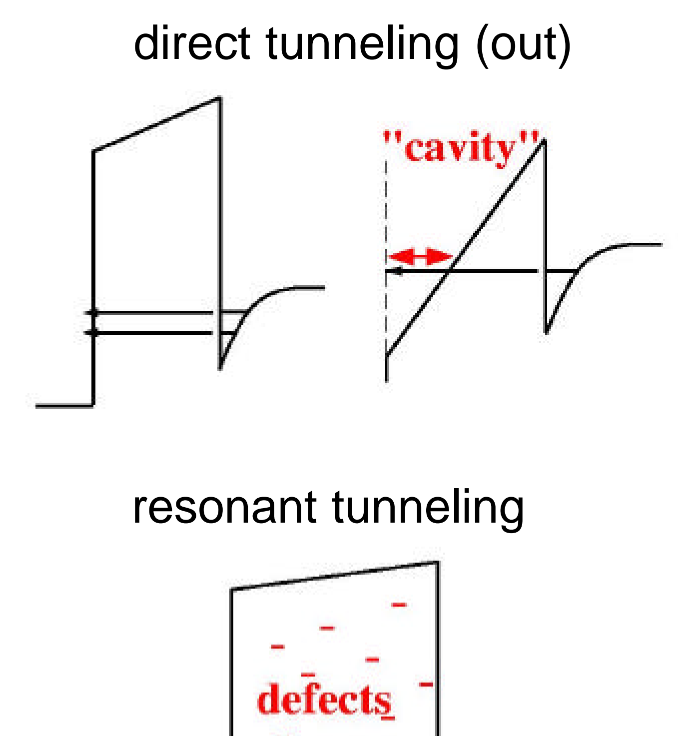
direct and resonant tunneling leakage

MOS capacitors with thermal oxide

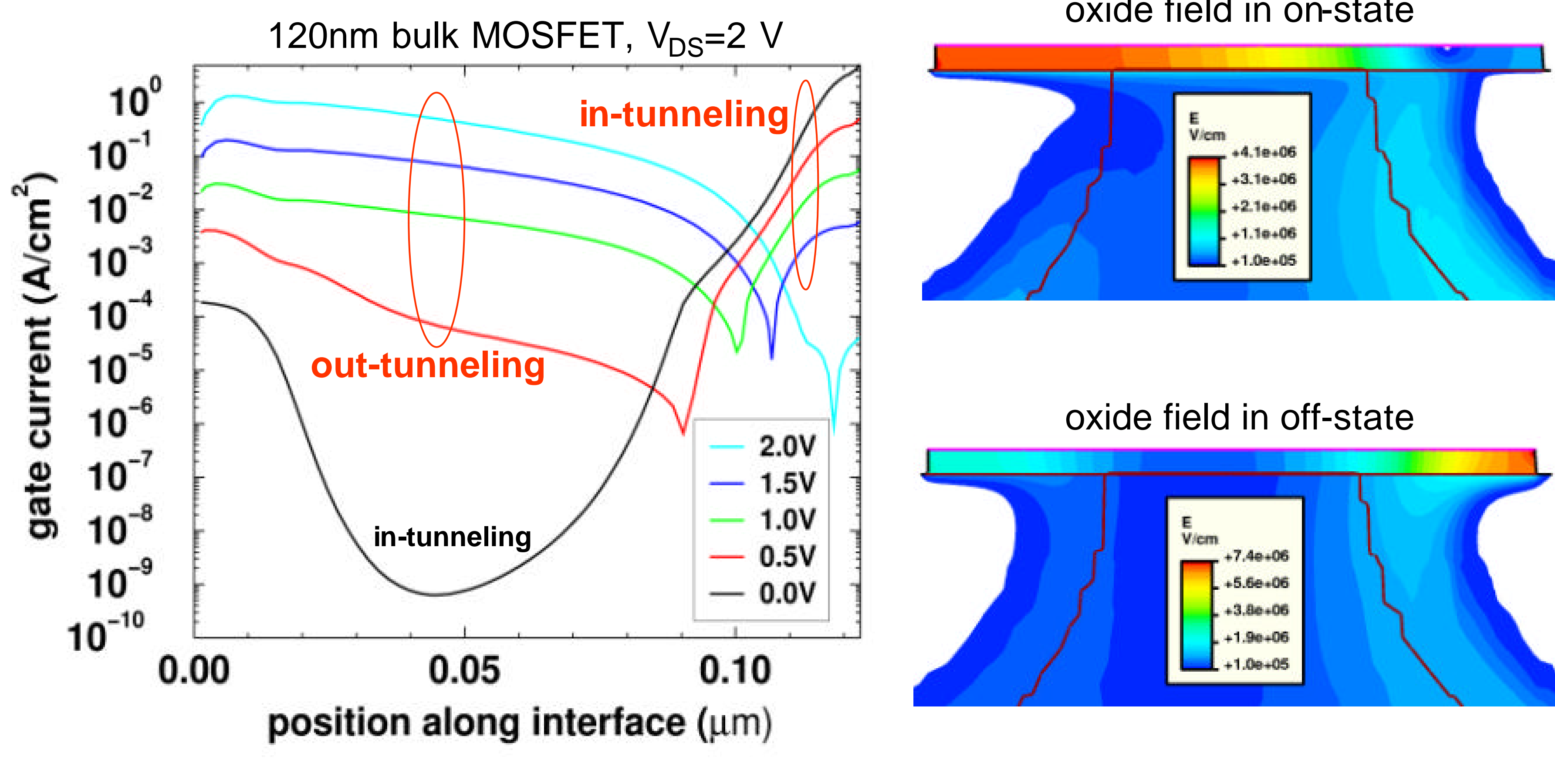


H. S. Momose et al., IEEE TED 43, 1233 (1996)

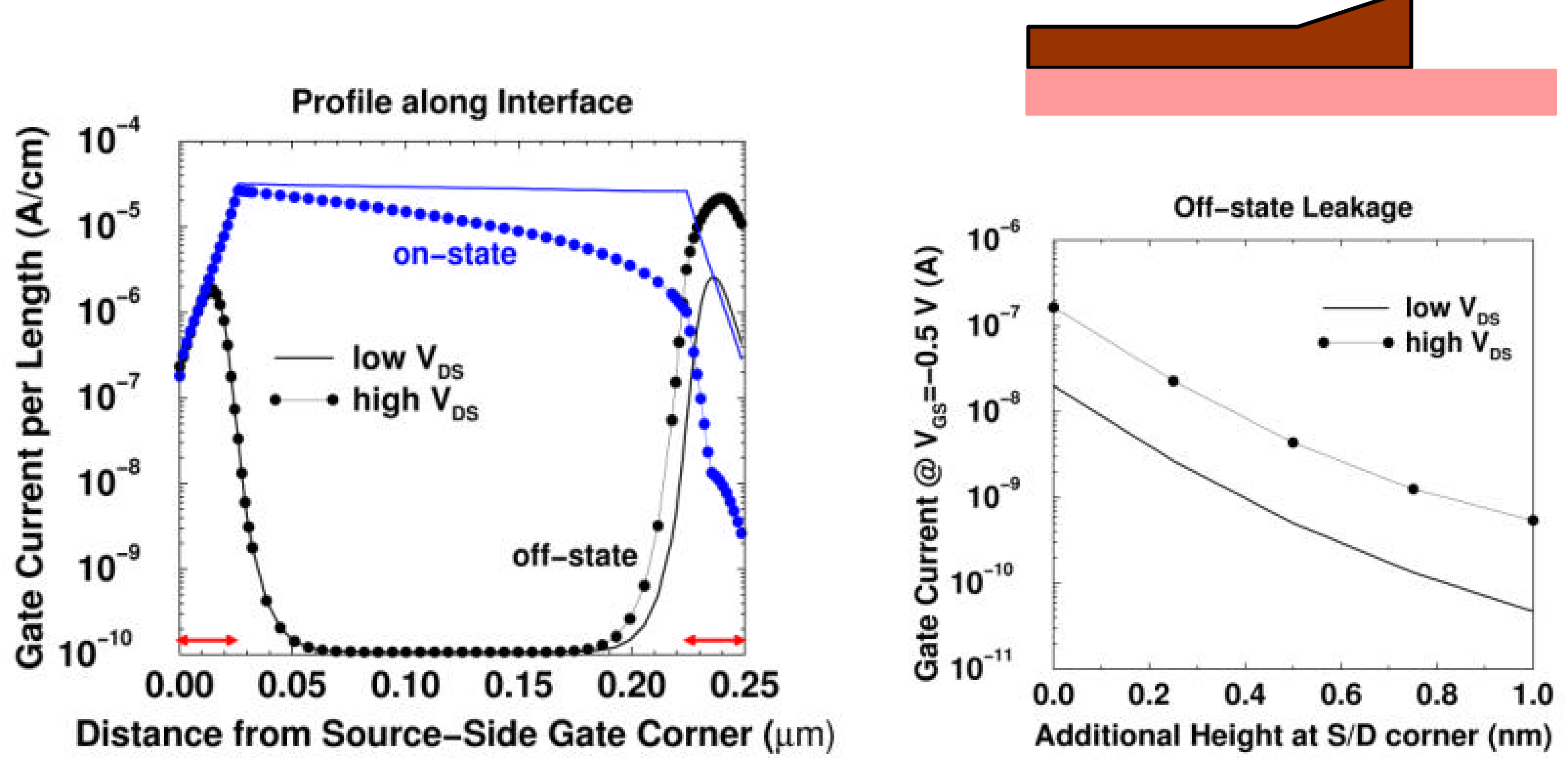
direct tunneling (out)



Gate current profiles in a MOSFET

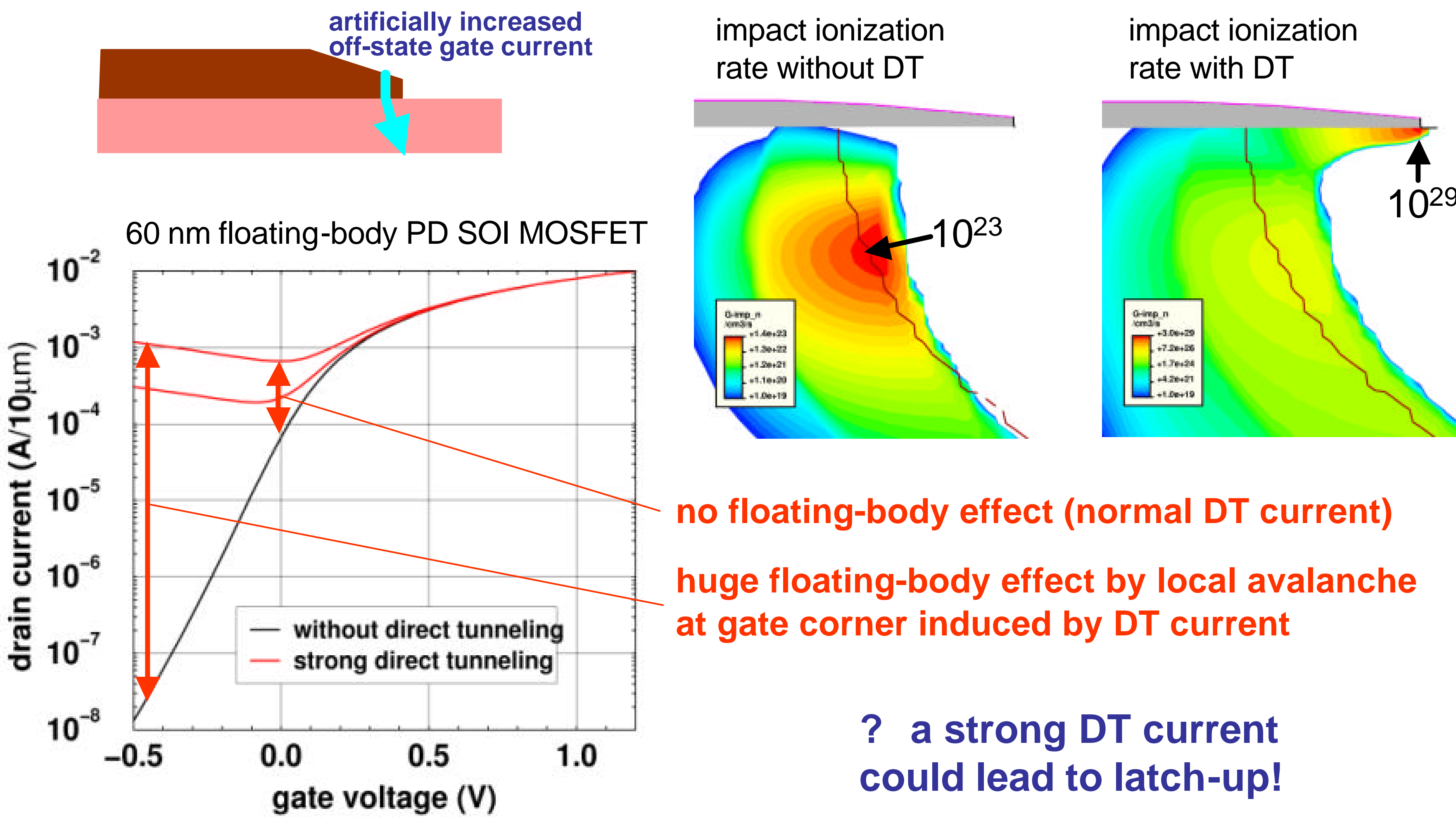


Sensitivity on oxide shape at drain



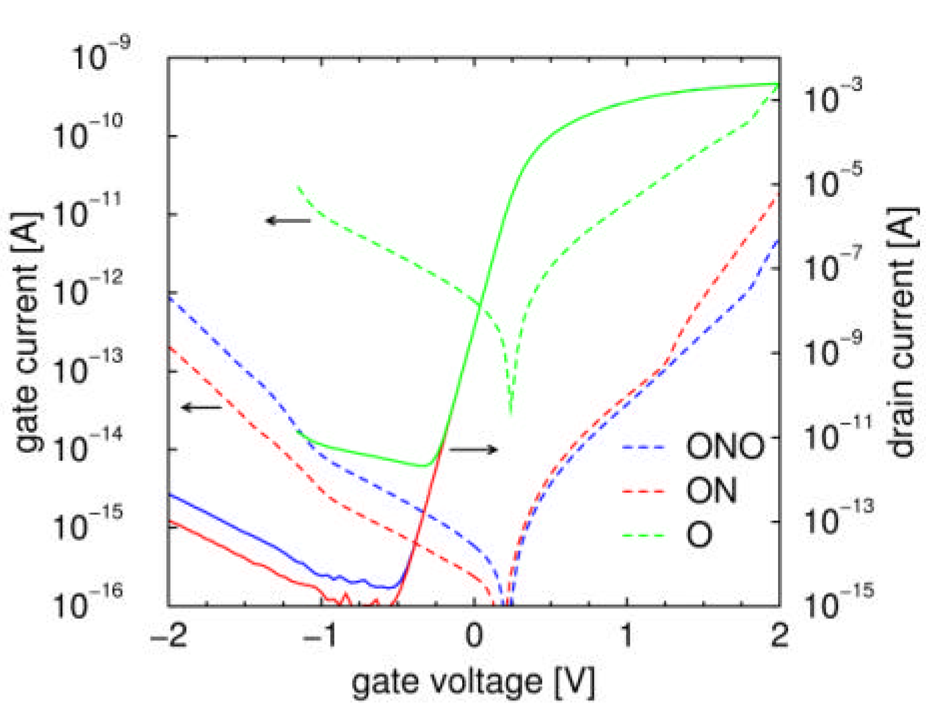
poly re-oxidation can strongly reduce in-tunneling (and hence off-state power consumption)

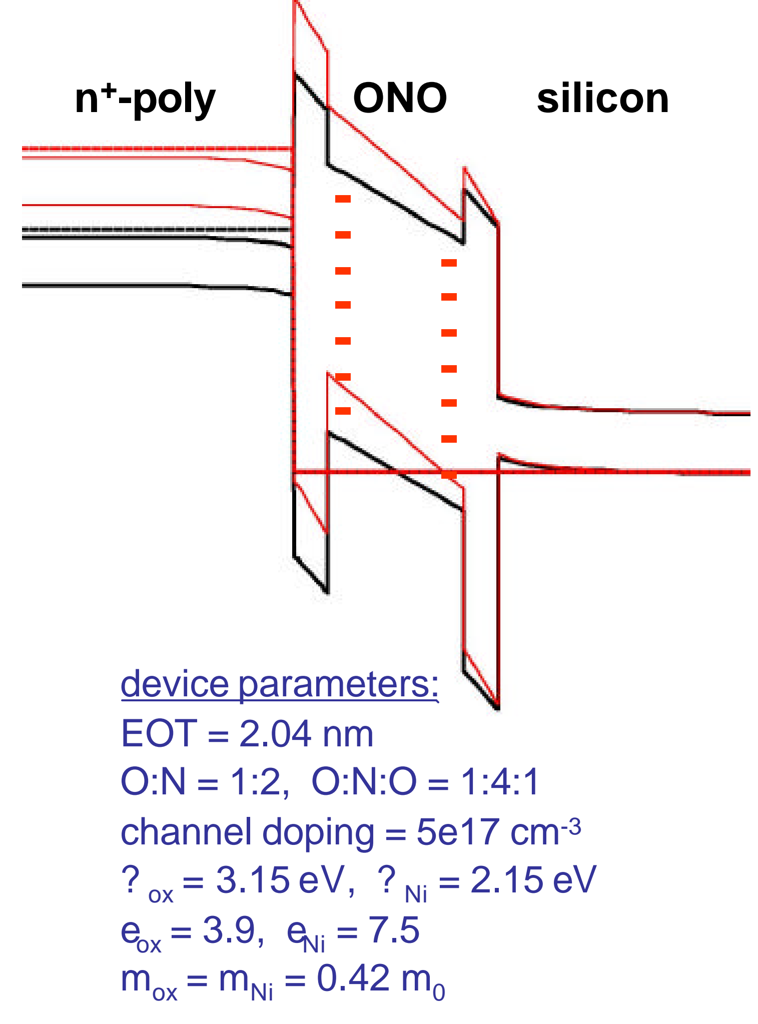
gate-current-induced junction leakage in floating-body PD SOI MOSFETs



stack dielectrics

Example: ON and ONO stack





direct tunneling: 3 orders reduction both for ON and for ONO

drain current only affected for strong in-tunneling

more likely: resonant tunneling

device parameters:

EOT = 2.04 nm

O:N = 1:2, O:N:O = 1:4:1

channel doping = 5e17 cm^{-3}

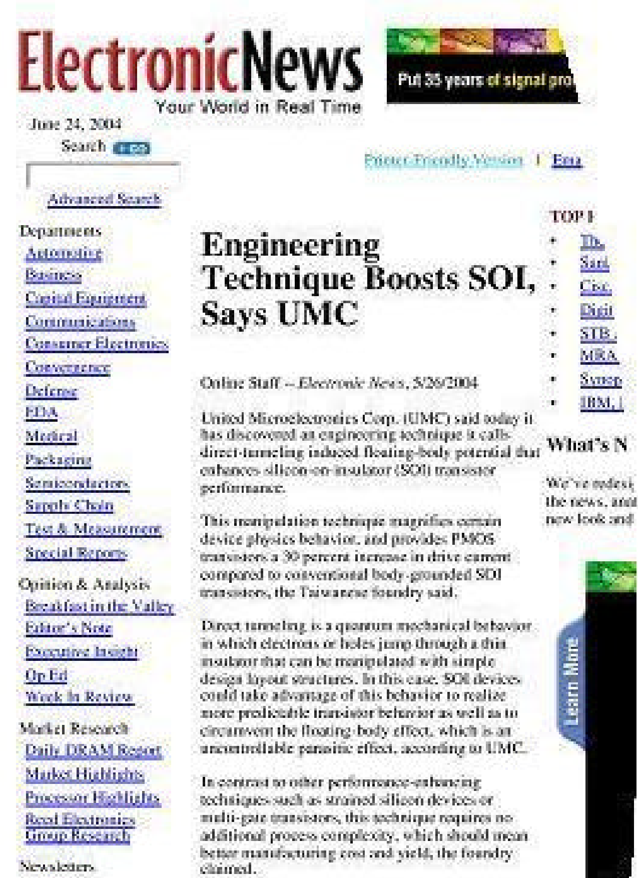
$?_{ox}$ = 3.15 eV, $?_{Ni}$ = 2.15 eV

e_{ox} = 3.9, e_{Ni} = 7.5

$m_{ox} = m_{Ni} = 0.42\ m_0$

valence-electron tunneling (?)

UMC claims 30% enhancement of PMOS drive current by direct tunneling



ElectronicNews
Your World in Real Time

June 24, 2004

Engineering Technique Boosts SOI, Says UMC

Online Staff -- *Electronic News*, 5/26/2004

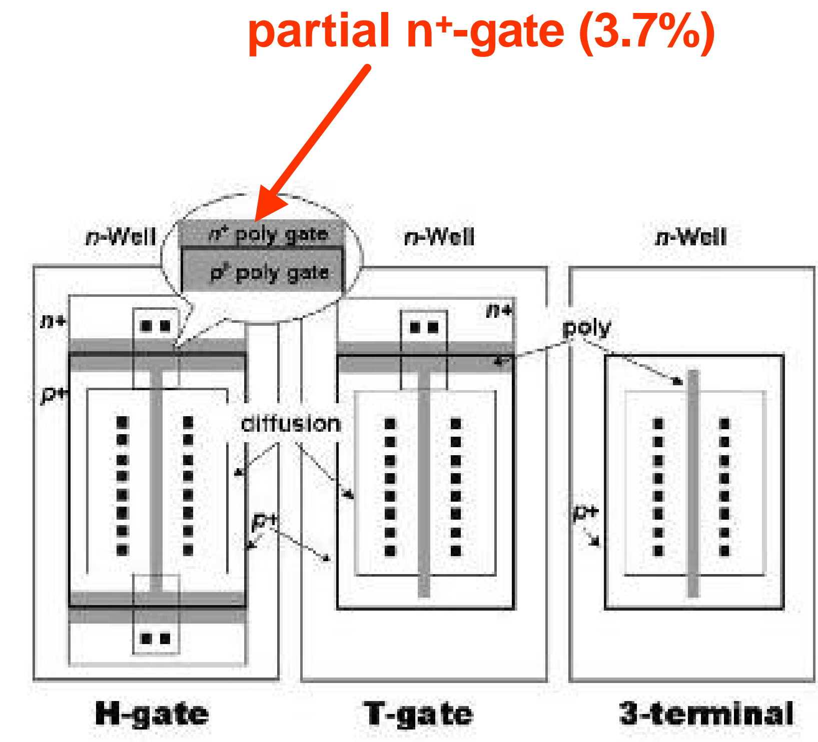
United Microelectronics Corp. (UMC) said today it has discovered an engineering technique it calls direct-tunneling induced floating-body potential that enhances silicon-on-insulator (SOI) transistor performance.

This manipulation technique magnifies certain device physics behavior, and provides PMOS transistors a 30 percent increase in drive current compared to conventional body-grounded SOI transistors, the Taiwanese foundry said.

Direct tunneling is a quantum mechanical behavior in which electrons or holes jump through a thin insulator that can be manipulated with simple design layout structures. In this case, SOI devices could take advantage of this behavior to realize more predictable transistor behavior as well as to circumvent the floating-body effect, which is an uncontrollable parasitic effect, according to UMC.

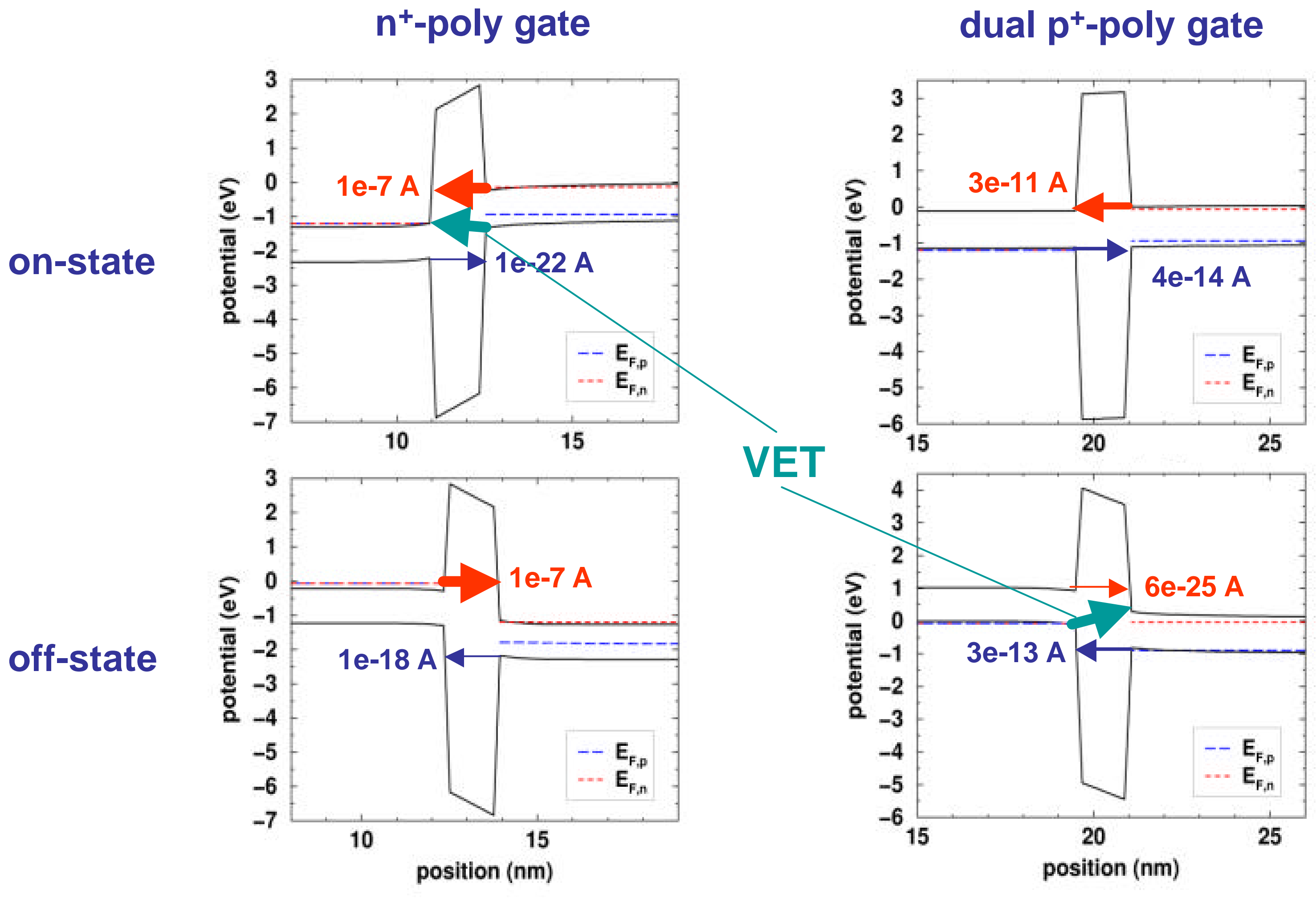
In contrast to other performance-enhancing techniques such as strained silicon devices or multi-gate transistors, this technique requires no additional process complexity, which should mean better manufacturing cost and yield, the foundry claimed.

partial n+-gate (3.7%)



S. S. Chen et al., IEEE TED 51(5) 2004, pp. 709-714

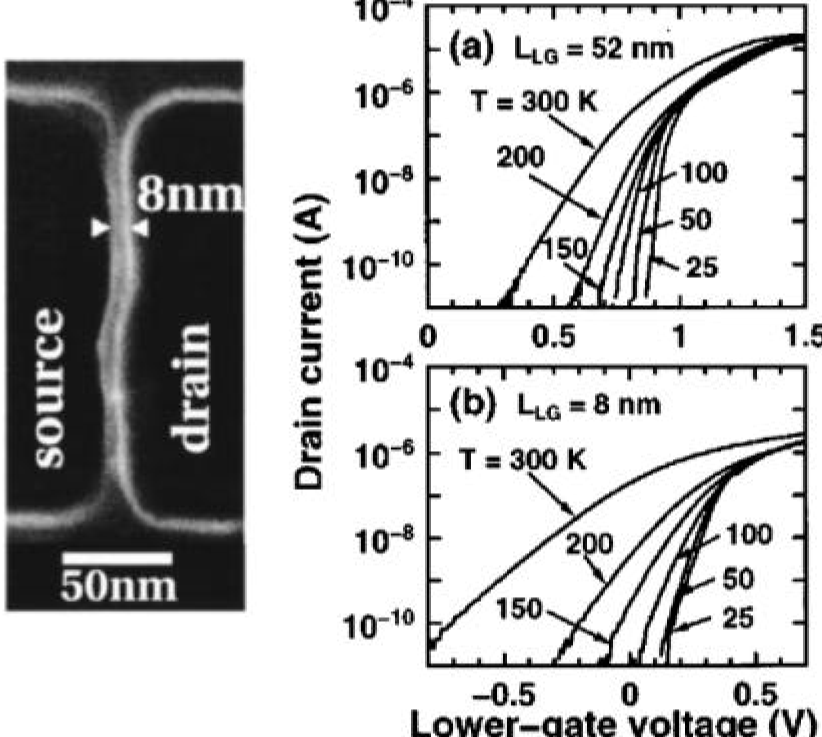
Floating-body PD SOI nMOSFET, $t_{ox} = 1.6nm$, $V_{DS} = 1.2$ V



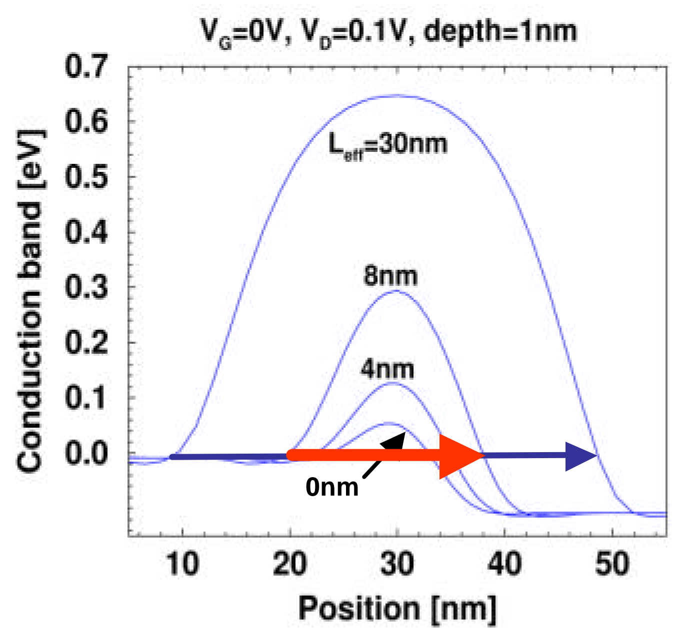
Source-to-drain tunneling

quantum-ballistic simulations of FD DGSOI MOSFETs at the limit of scaling

Experiment:



H. Kawaura et al., APL 76(25) (2000)



Is source-to-drain tunneling a fundamental limitation to CMOS scaling?

- ⋆ Coherent transport
  - $\nexists$ inelastic scattering.
  - An e^- remains in a fixed Ψ (solution of Schrödinger eq$^{\underline{n}}$).
  - When occupied, Ψ carries a current $I(\Psi) \propto$ transmission probability $T(\epsilon)$.
- ⋆ Thermal carrier injection at the contacts.

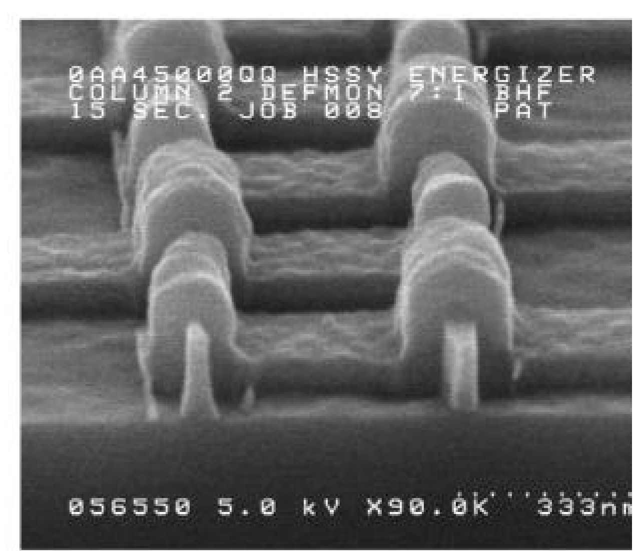
$\Rightarrow$ Landauer–Büttiker formula:

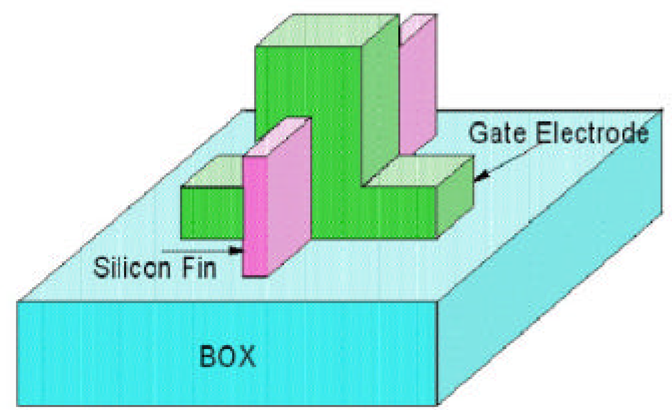
$$I = -\frac{2e}{h} \sum_{v,i} \int_{\epsilon^0_{v,i}}^{\infty} d\epsilon \; T_{v,i}(\epsilon) \Big(f\big(\beta(\epsilon - \epsilon^{\text{src}}_{\text{Fermi}})\big) - f\big(\beta(\epsilon - \epsilon^{\text{drn}}_{\text{Fermi}})\big) \Big) \qquad \text{1D}$$

$$I = -\frac{2e}{h}\sqrt{\pi}\frac{W}{\lambda_{\text{th}}} \sum_{v,i} \int_{\epsilon^0_{v,i}}^{\infty} d\epsilon \; T_{v,i}(\epsilon) \Big(\mathfrak{F}_{-\frac{1}{2}}\big(\beta(\epsilon^{\text{src}}_{\text{Fermi}} - \epsilon)\big) - \mathfrak{F}_{-\frac{1}{2}}\big(\beta(\epsilon^{\text{drn}}_{\text{Fermi}} - \epsilon)\big) \Big) \qquad \text{2D}$$

W: width of the device

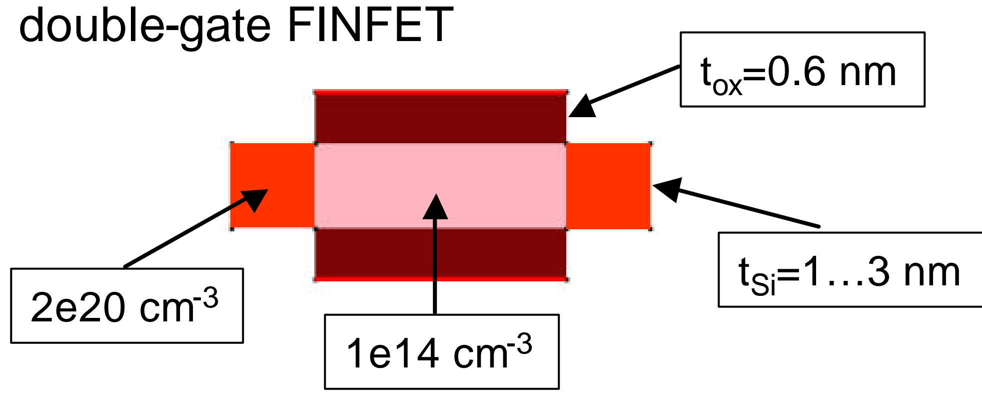
λ_{th}: electron thermal wave–length $h/\sqrt{2m^* k_{\text{B}} T}$





test device:

double-gate FINFET

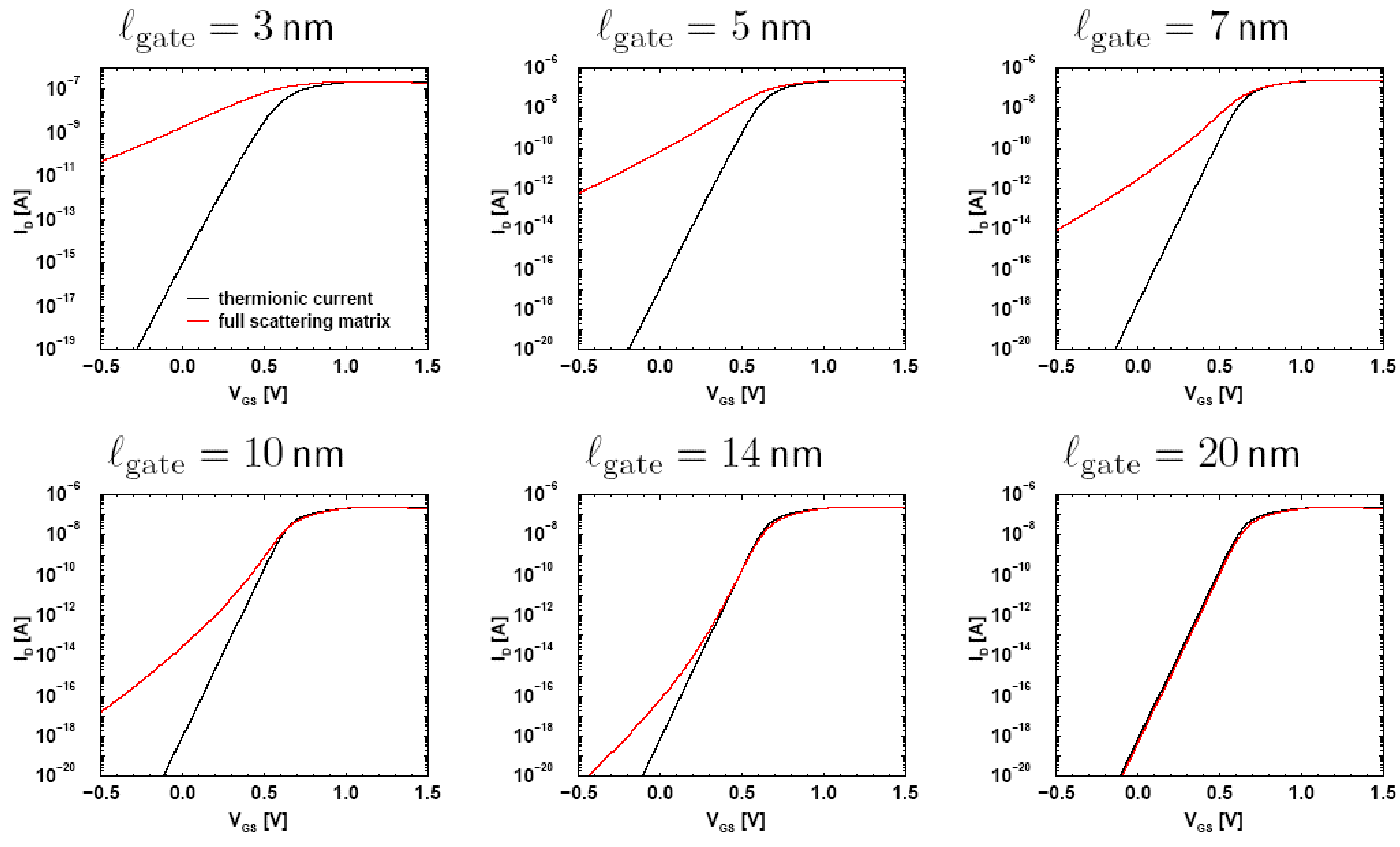


J. Wang and M. Lundstrom, Proc. IEDM 2003

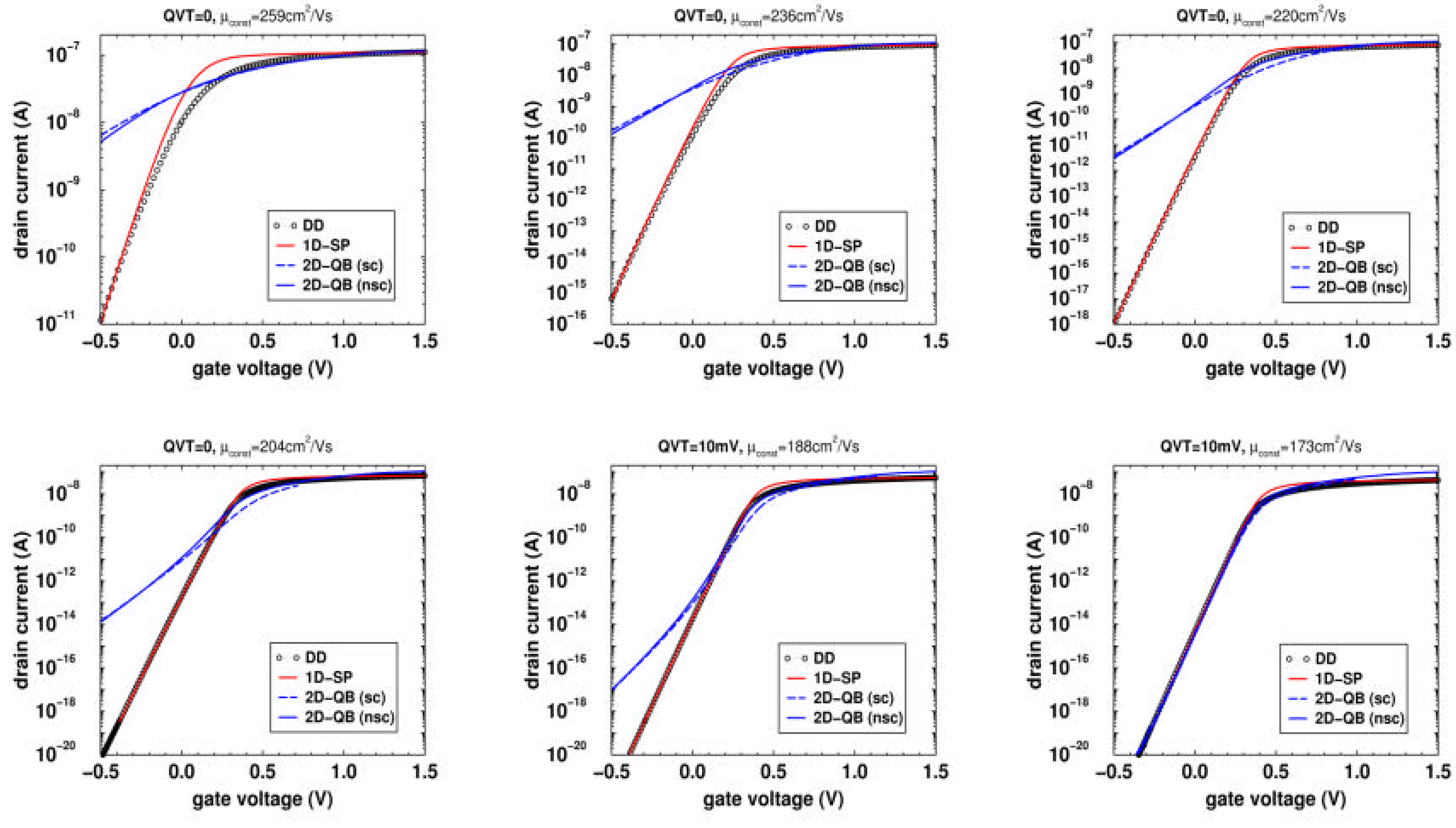
in simulation:

longer S/D, full oxide coverage

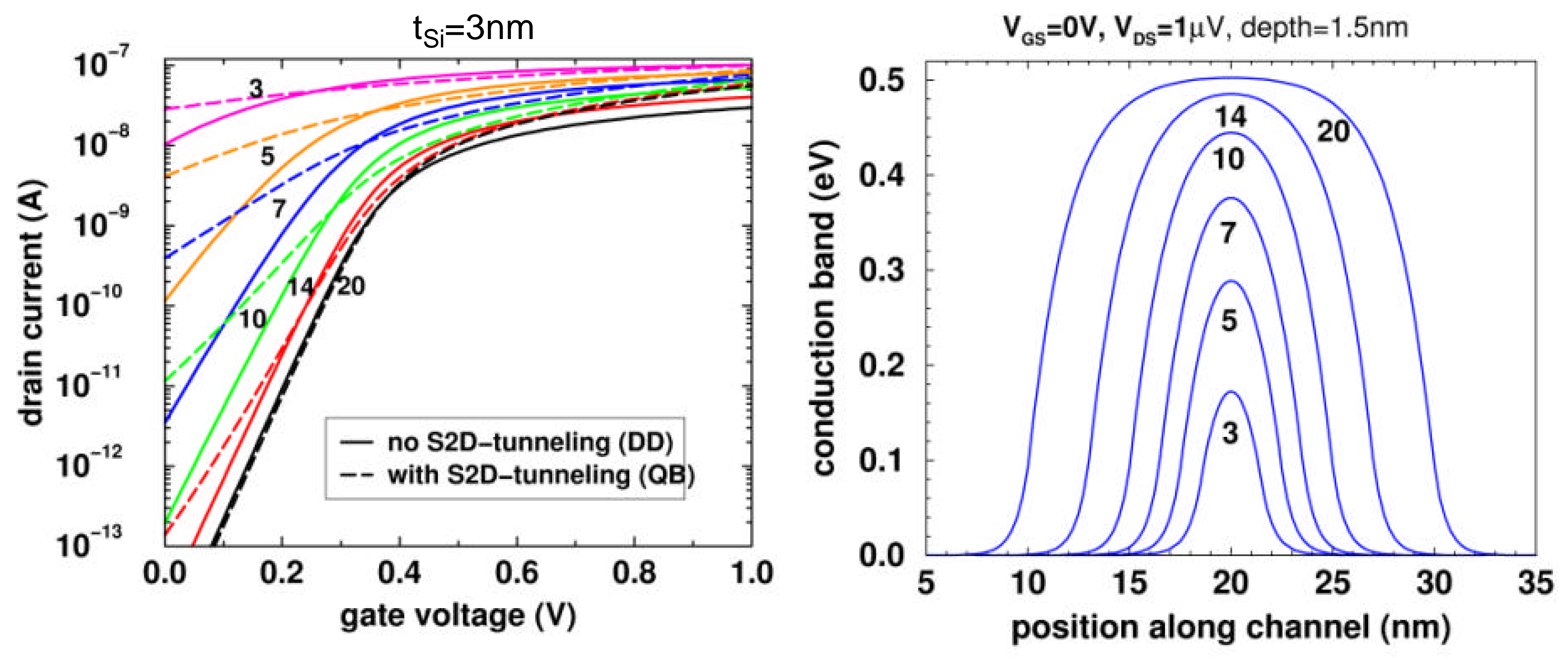
FINFET with (100)-SOI thickness of 1 nm, V_{SD}=1μV



FINFET with (100)-SOI thickness of 3 nm, V_{SD}=1μV

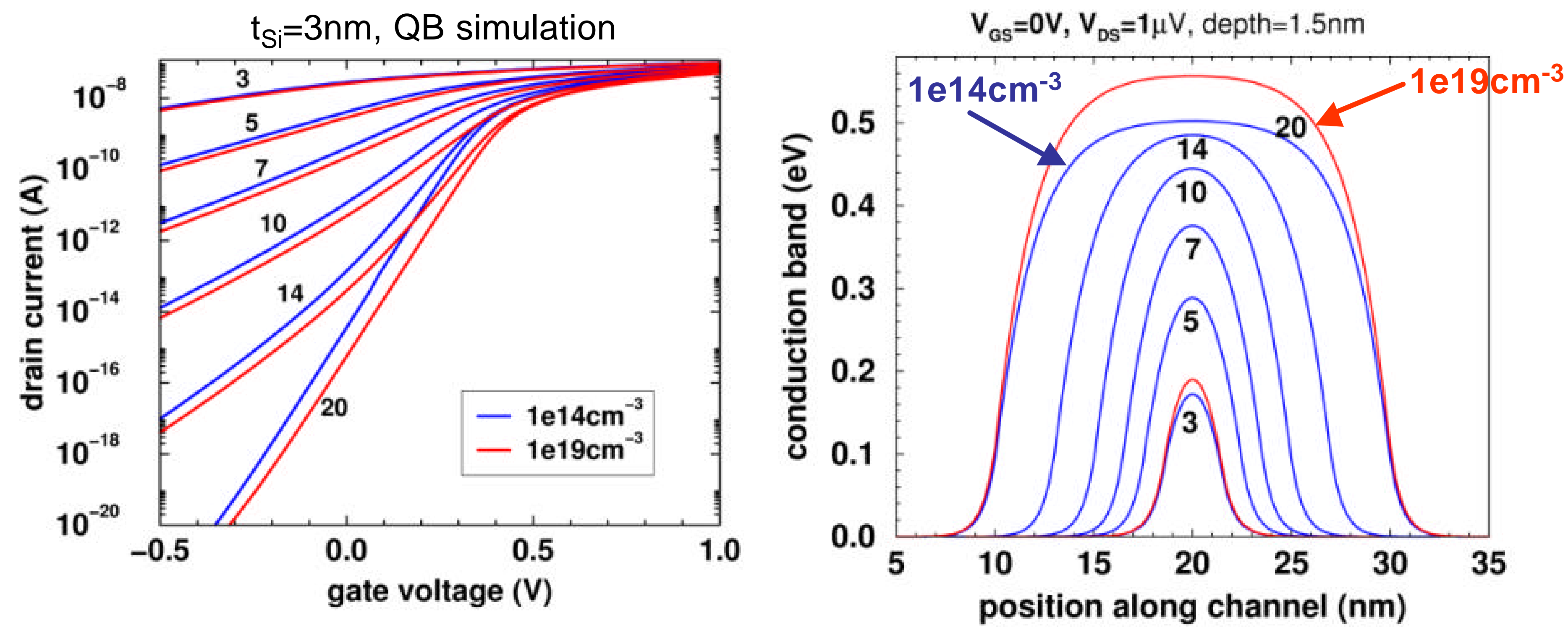


reason for the high off-current



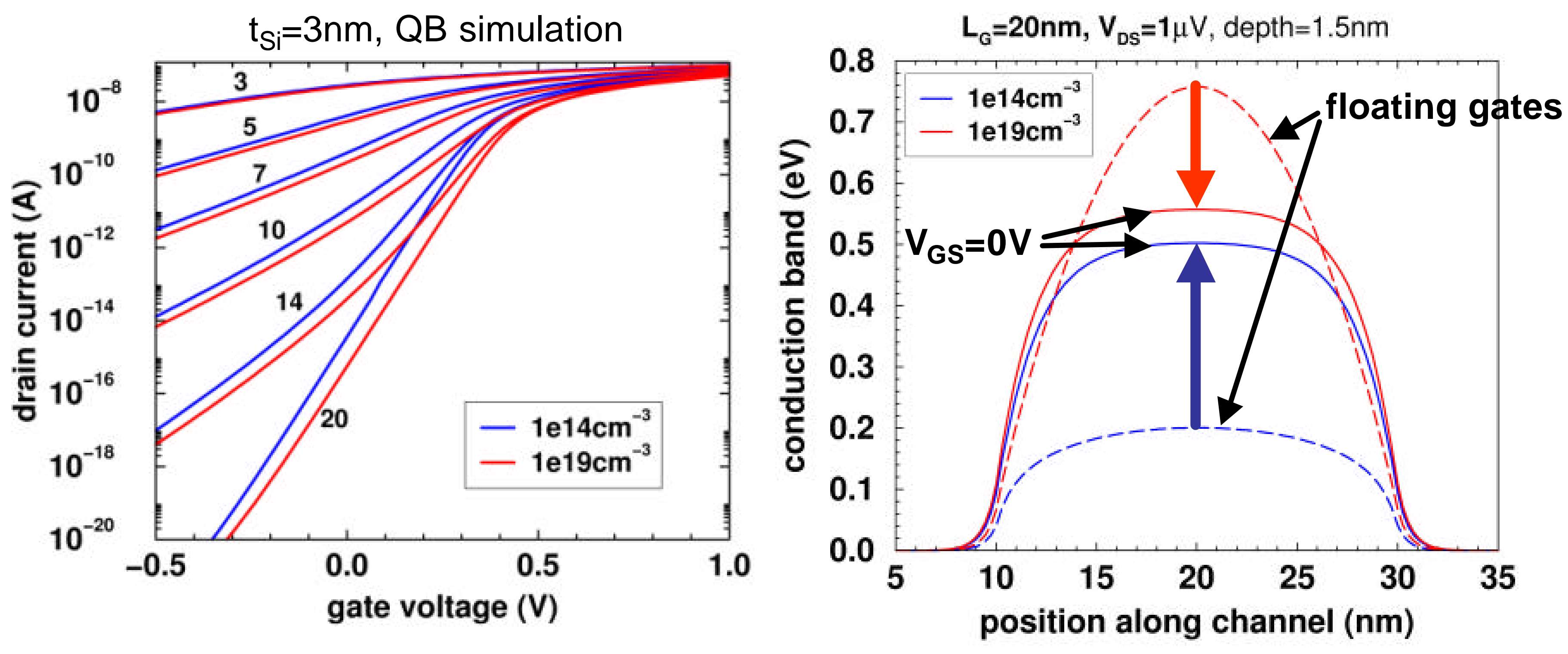
height and width of source-drain potential barrier decrease drastically with shrinking gate length!

Effect of channel doping



height of source-drain potential barrier only weakly dependent on channel doping!

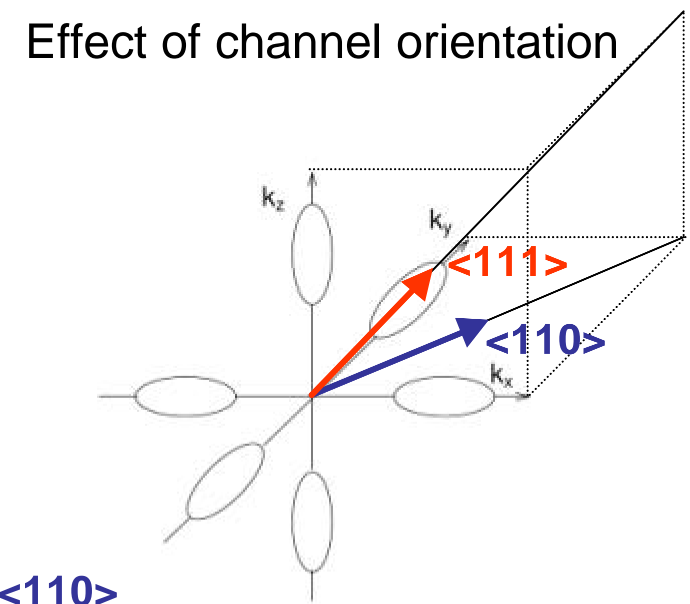
Effect of channel doping



height of source-drain potential barrier pinned by gate bias!

S2D-tunneling not significantly reduced by channel doping!

Effect of channel orientation



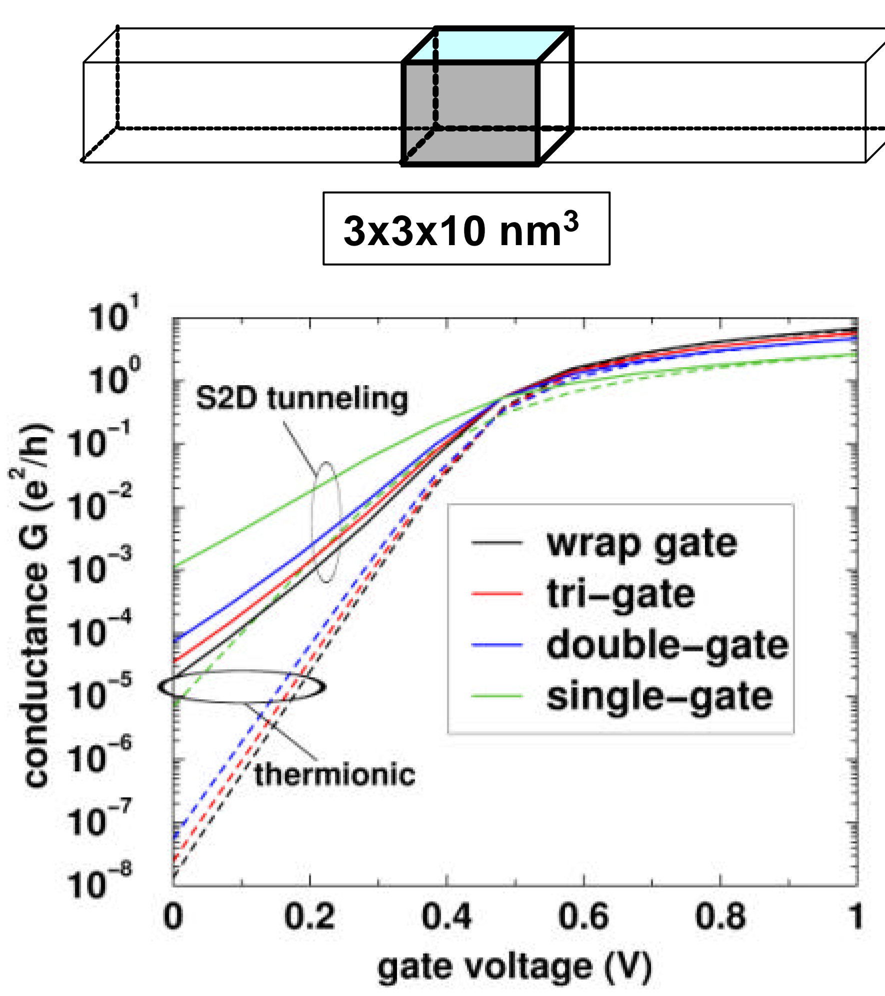
<u><110></u>

4 in-plane valleys with $2m_lm_t/(m_l+m_t)$ = $0.31m_0$, but 2 valleys with $m_t = 0.19m_0$? no advantage

<u><111></u>

all six valleys with $3m_lm_t/(2m_l+m_t)$ = $0.26m_0$? strong suppression of S2D-tunneling

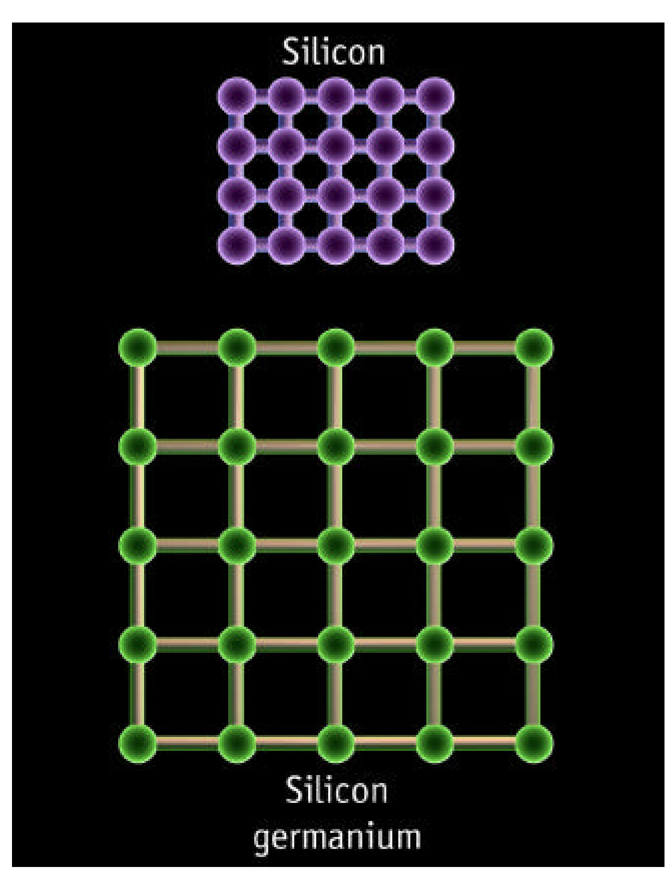
Effect of gate configuration

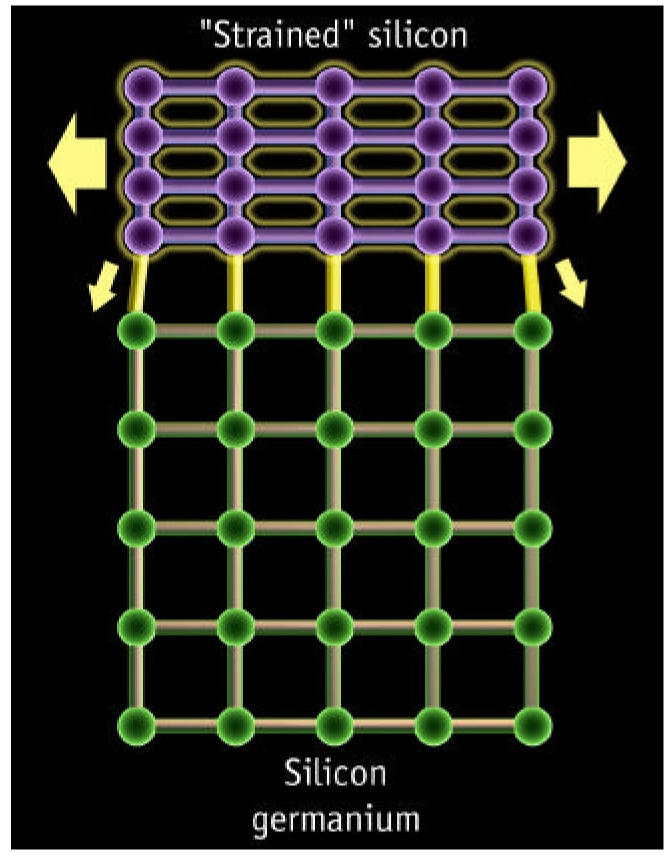


Quasi-ballistic effects

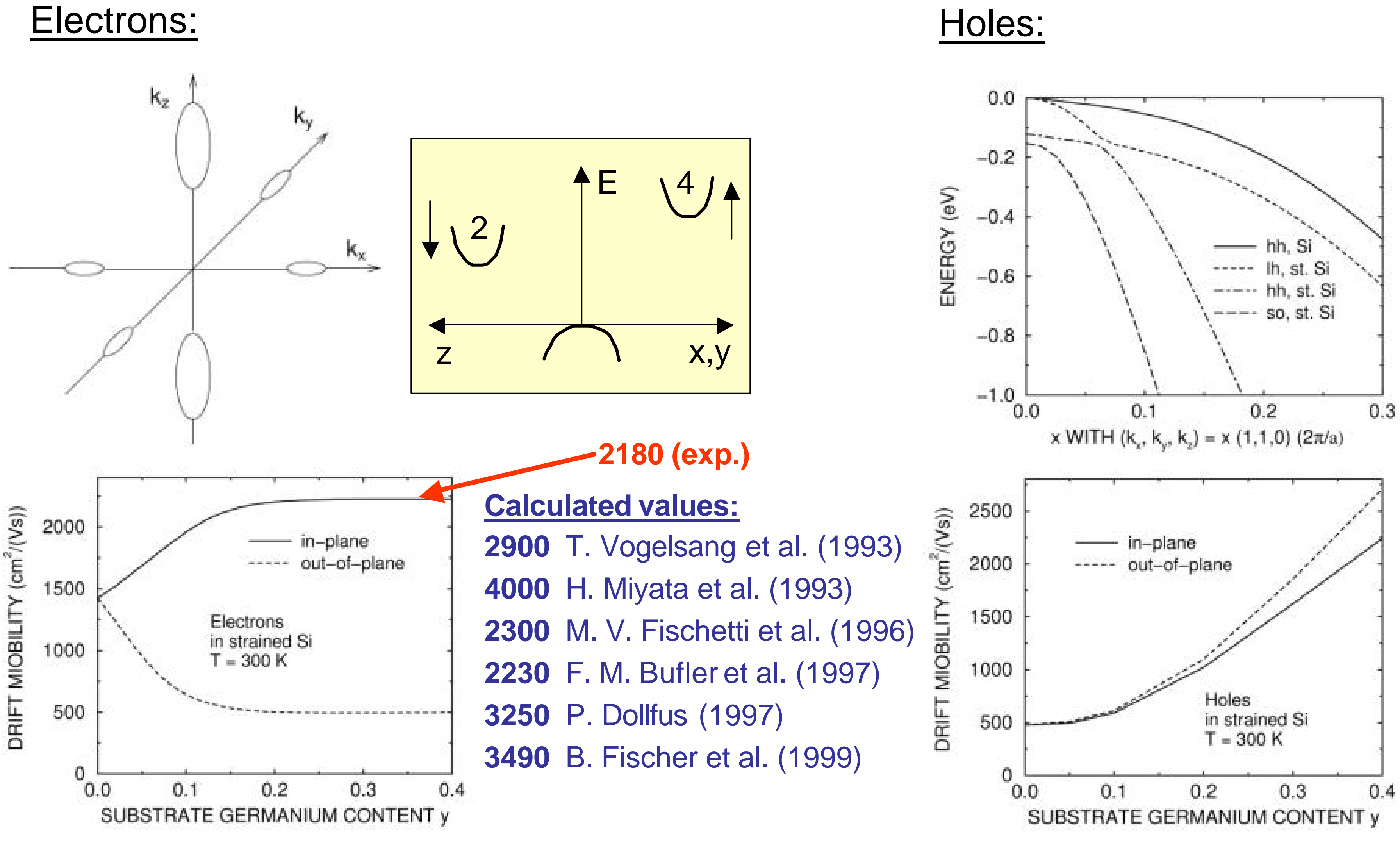
strained silicon

<u>biaxial tensile strain:</u>

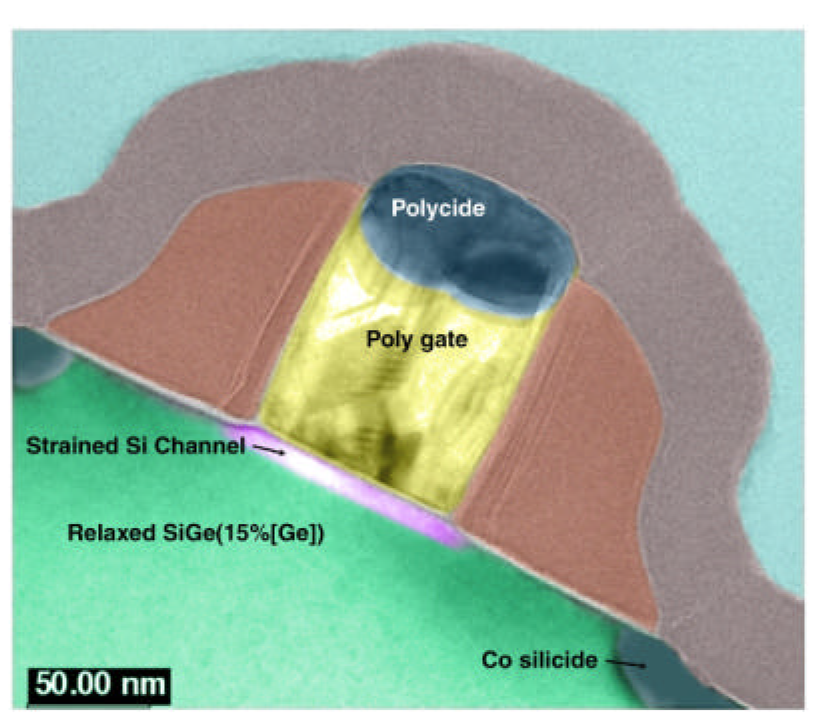


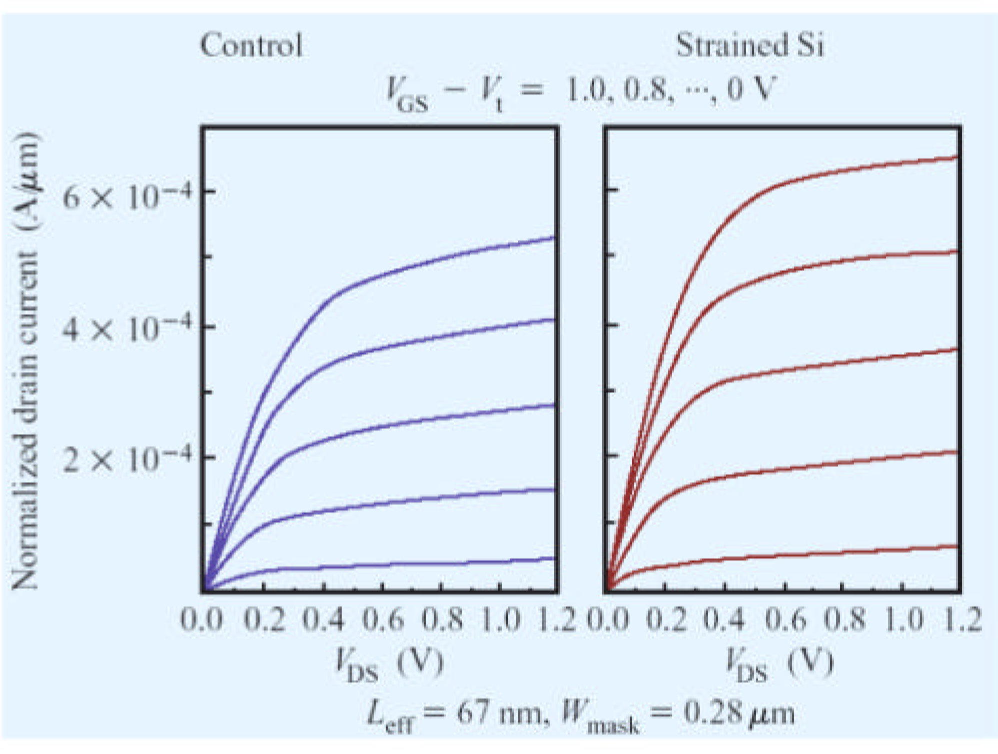


Effect on band structure and drift mobility



Measured current improvement (IBM)

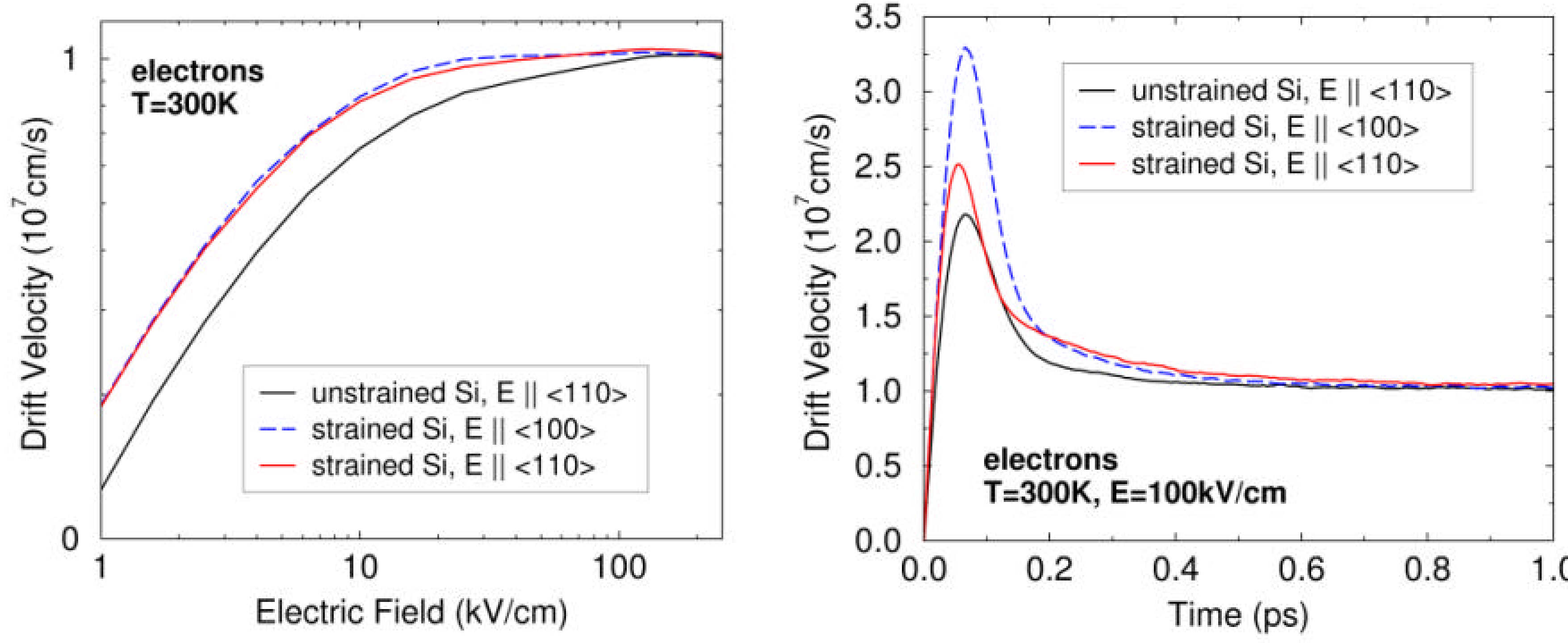




K. Rim et al., Symp. on VLSI Techn., 59 (2001)

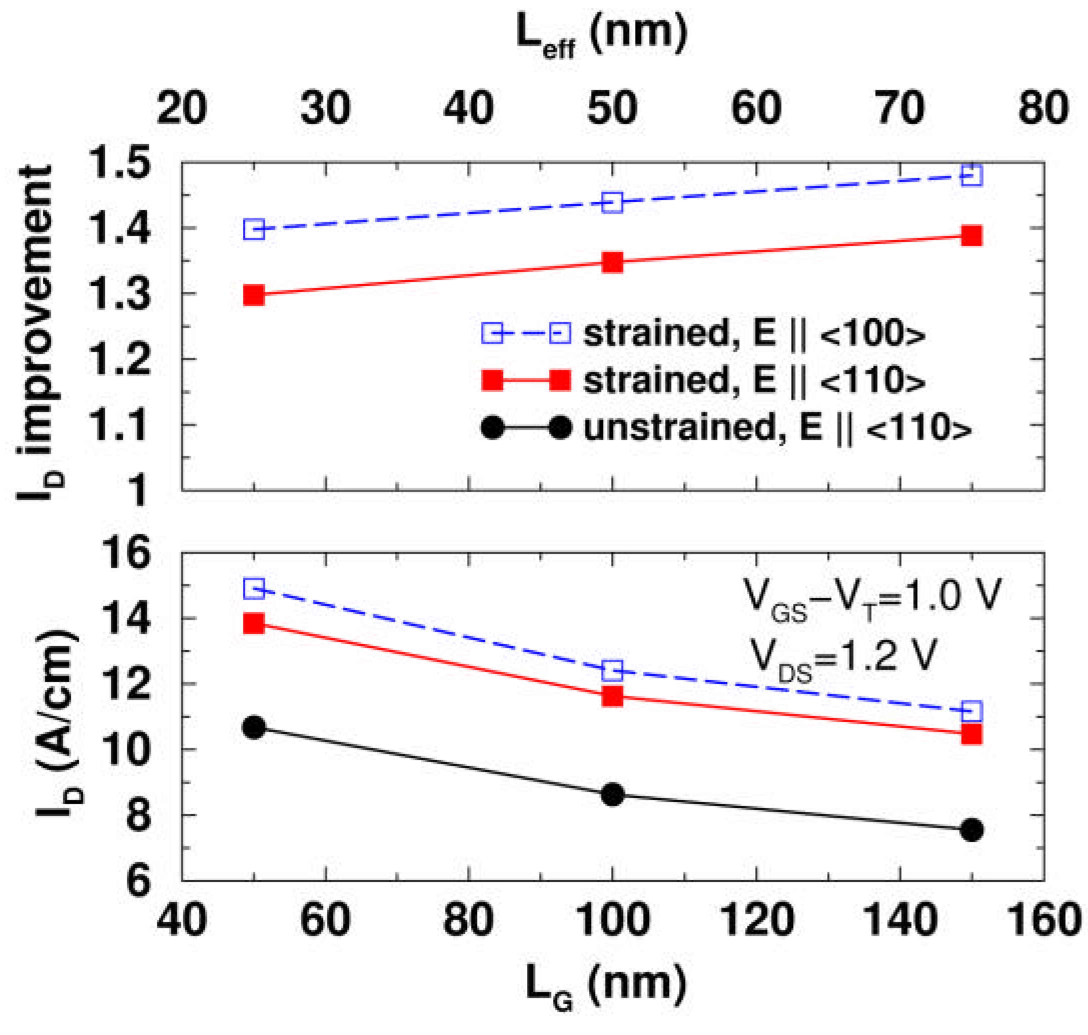
- **nMOSFET with strained Si channel, L_{eff}=67nm**
- **35% improvement at V_{GS}-V_{th}=1.0V, V_{DS}=1.2V**

Non-linear and quasi-ballistic transport



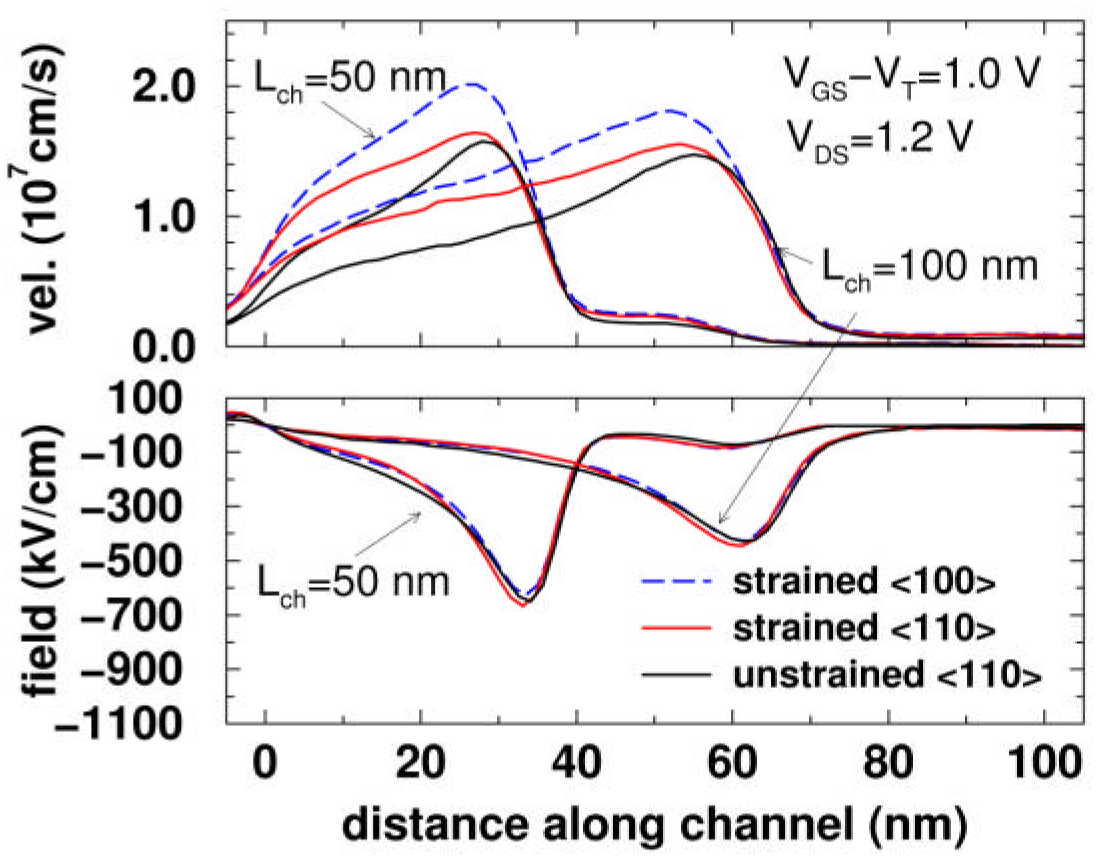
- **strain doesn't change *saturation* drift velocity**
- **4% anisotropic stationary velocity at the most**
- **35% anisotropic quasi-ballistic velocity**

FBMC simulation of current scaling



- **strain-induced current improvement**
- **10% anisotropy in strained silicon**

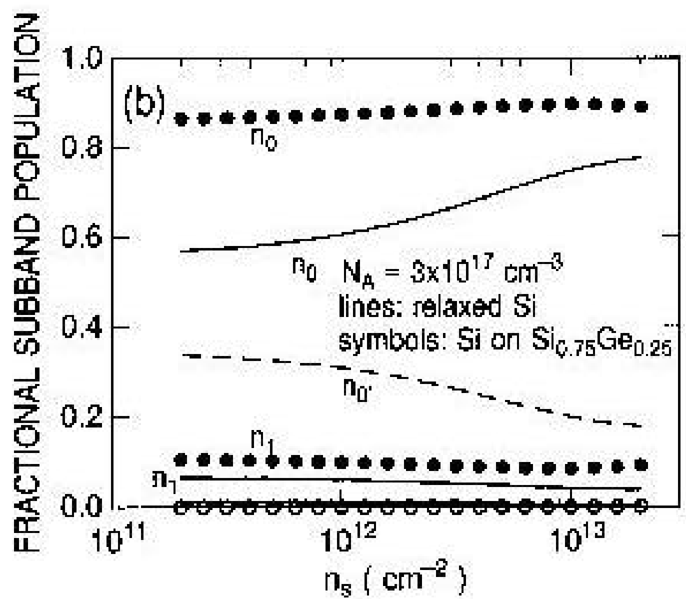
Velocity and field profiles

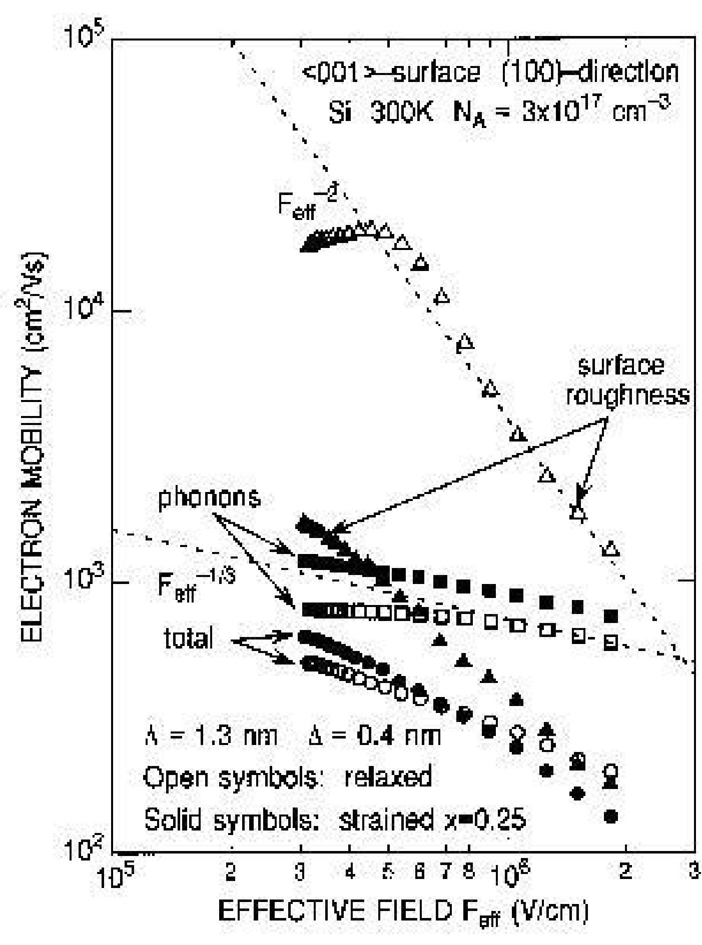


- **velocities at field peak are almost equal**
- **source-side velocity higher than saturation velocity**
- **anisotropic source-side velocity**
- **? quasi-ballistic transport near source is responsible for current improvement!**

Do we understand strained-Si MOSFETs?

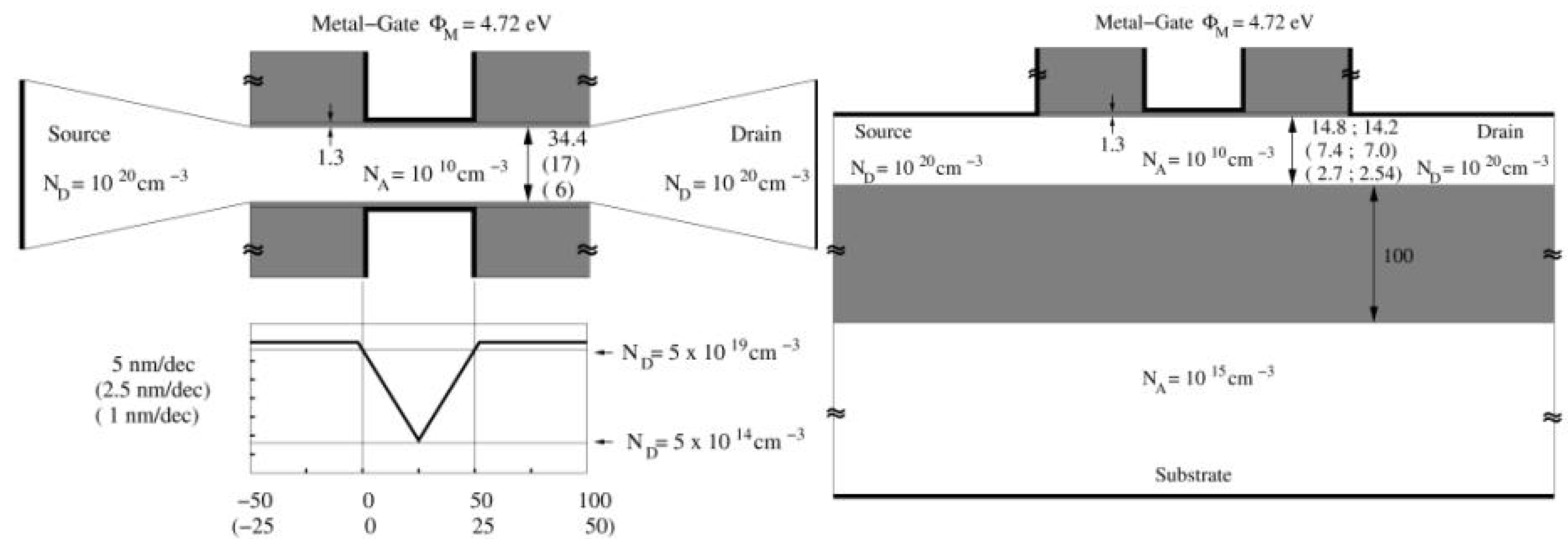
- **confinement already lifts valley degeneracy (as tensile strain does)**
- **population effect only ~15% larger**
- **stronger SR scattering (less screening) ? lower mobility at higher E_{eff}**





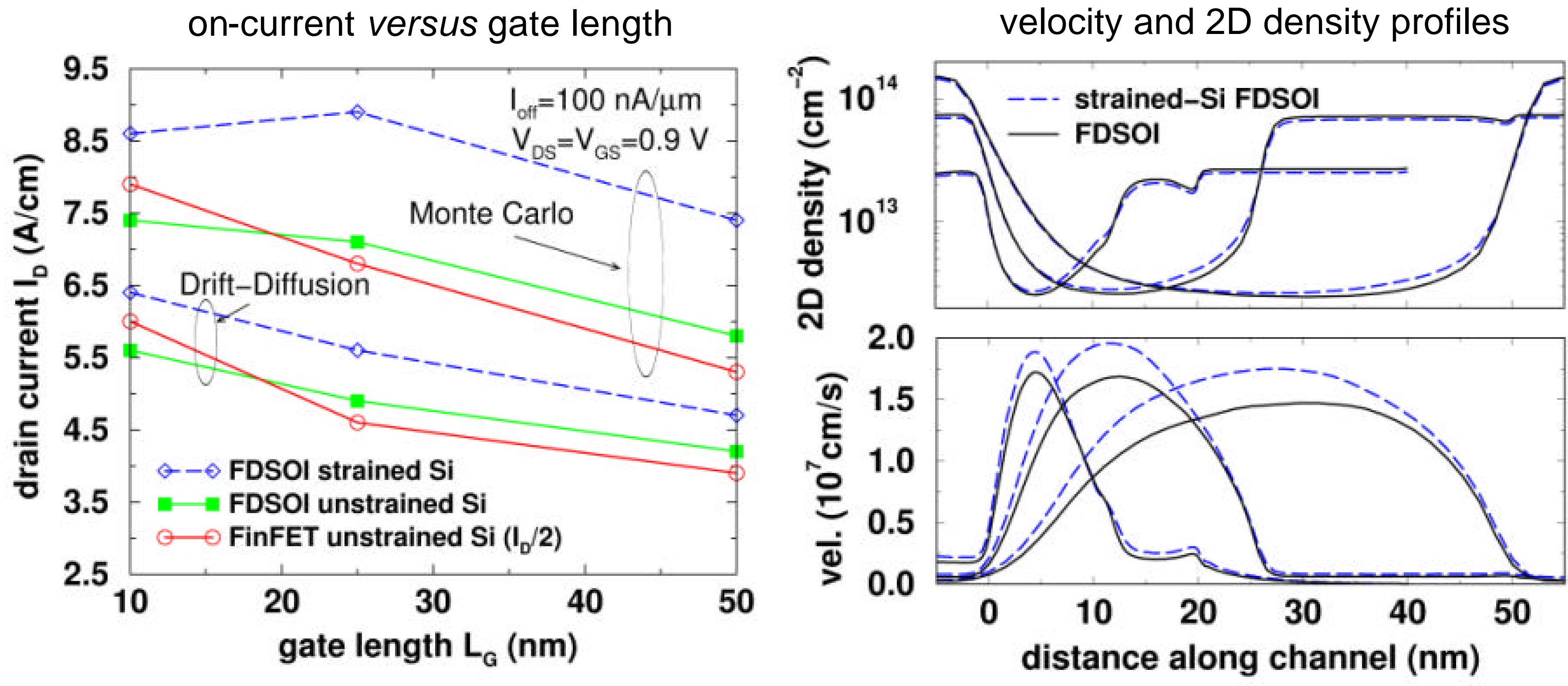
M. V. Fischetti et al., JAP 92(12) 2002, pp. 7320-24

Scalability of FinFETs, unstrained-Si and strained-Si FD SOI MOSFETs



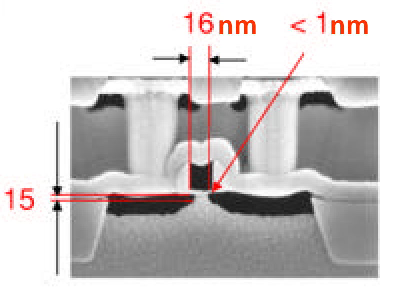
- L_G scaling: 50? 25? 10nm; Si orientation = <110>
- constant off-current I_{off}=100nA/µm @ V_{DS}=0.9V by scaling of t_{Si}: 34.4? 17? 6nm
- corresponding scaling of source/drain, spacer length, doping steepness: 5? 2.5? 1m/dec

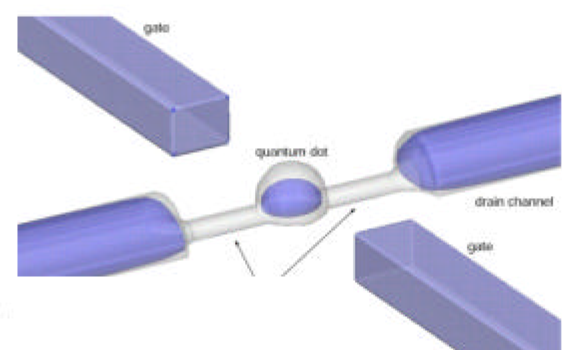
- strain defined by $Si_{0.8}Ge_{0.2}$ buffer
- t_{Si} scaling unstrained: 14.8? 7.4? 2.7nm
- t_{Si} scaling strained: 14.2? 7? 2.54nm
- strained needs thinner SOI to compensate for higher I_{off} (smaller gap)



- **FinFET has the best scalability, but strained-Si FDSOI has the best on-current**
- **strain-enhanced I_{on}'s are due to source-side velocity overshoot**
- **velocity improvement for strained-Si FDSOI upon scaling to L_G=10nm cannot compensate the reduced sheet density ? on-current gets maximum**
- **problems: missing B2B and S2D tunneling (higher I_{off}), missing QM confinement**

Outlook: Future simulation challenges





Semiconductor-based nanodevices

(SEMs and SETs with strong confinement)

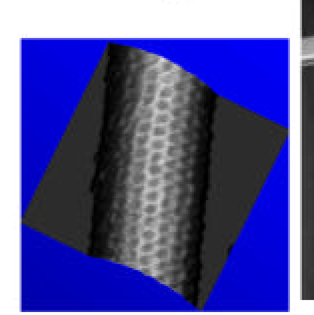
- “extension” of ‘top down’ CMOS, convergence of physics
- tolerances < 1nm, surface states, stray charges, wiring problem, power dissipation

Molecular nanodevices

(e.g. oligo-thiophen, C_{60})

- ‘bottom up’ strategy, no inherent tolerance problem (identical units)
- integration (self-assembly), yield, extremely small currents, sensitivity to contacting

Carbon nanotube devices



- 1D, ballistic transport at 300K up to 250nm? very high ‘mobility’, identical n- and p-type, …
- “switch” based on Schottky barriers, integration, stray charges, sensitivity to chiral angle

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