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Enabling energy efficient tunnel FET-CMOS co-design by compact modeling and simulation

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This project is addressing the power dissipation as the greatest challenge for today's nanoelectronics. Tunnel-FETs are steep slope switches that address critical power issues and are considered in research and industry as the candidate with the highest potential for low power circuit and systems. To achieve its full potential it is required to understand the device physics, optimize its performance and be able to establish the modeling and simulation environment necessary to enable the co-design of steep slope switches with advanced CMOS for novel energy efficient integrated circuits.

ETHZ

The full-band quantum transport solver OMEN [1], allowing to perform atomistic simulations of many different materials as well as any transport direction and gate configuration, has been used to perform the atomistic simulation of the InAs nanowire represented in Fig. 1.

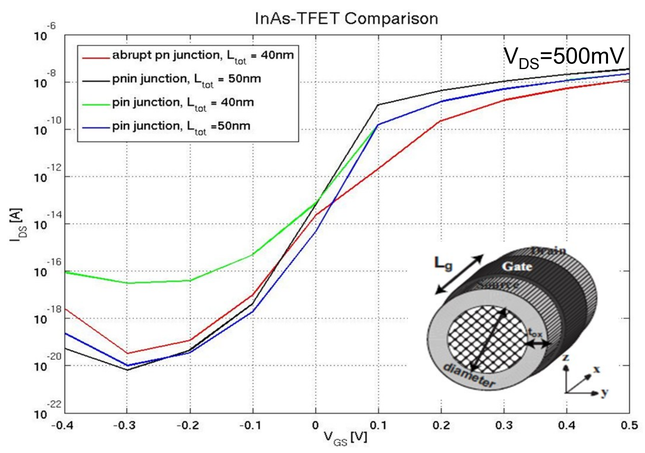

Fig. 1: Impact of different junction configurations on the transfer characteristics of an InAs based GAA nanowire TFET. The transport direction is aligned with the <100> crystal axis, the diameter is 3.35nm and 1nm of gate dielectric (ε_r = 9) have been used.

In Fig. 2, a Kane model [2] has also been compared with ballistic tight-binding NEGF results for bulk-like InAs homodiodes.

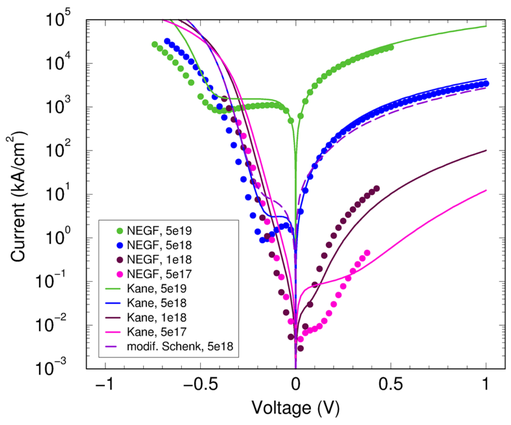

Fig. 2: Comparison between NEGF and TCAD models for ultra-short bulk-like symmetrical doped InAs Esaki diodes.

IBM

Si-InAs heterojunction *p-n* diodes have been fabricated by growing InAs nanowires in oxide mask openings on silicon substrates.

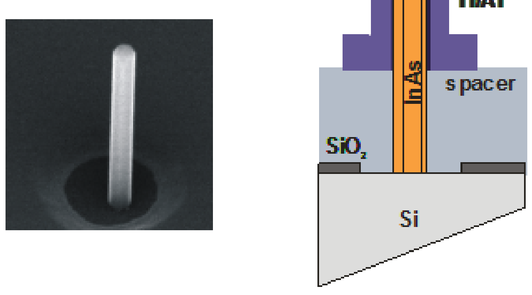

Fig. 3: Left: scanning electron micrograph of a vertical as-grown InAs nanowire on a Si<111> substrate. The nanowire diameters ranges from 110nm to 150nm. Right: schematic cross section of a Si-InAs heterojunction diode.

Fig. 4 investigates the effect of the doping concentration in the p-type Silicon on the diode characteristics.

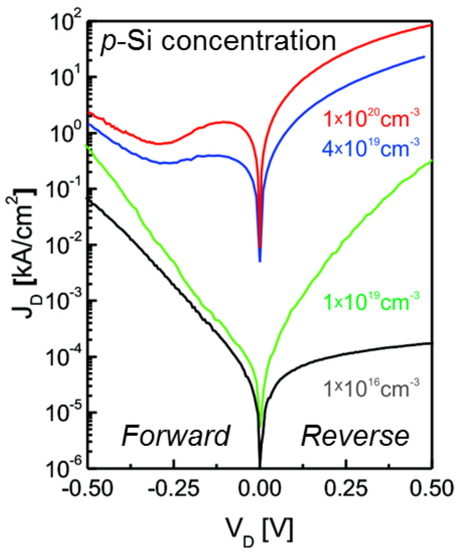

Fig. 4: current density as a function of the applied voltage for different substrate doping levels.

References

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EPFL

In order to include the B2BT in TCAD simulations based on the drift-diffusion theory, different models that describe the B2BT as an additional generation-recombination mechanism have been proposed.

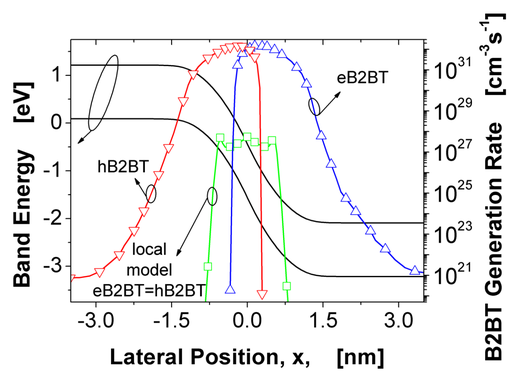

Fig. 5: Numerical simulation of a highly doped p-n junction (N_A=N_D=10^{21}cm^{-3}) showing the relevant differences between a local tunneling model [5] and a non-local one [6]. V_D=-2V.

Fig. 6-left shows a comparison between a TCAD FEM simulation and experimental datas.
On Fig. 6-right the result of the current predicted by an analytical model describing a reverse biased p-n junction are compared with numerical simulation showing a quite good agreement.

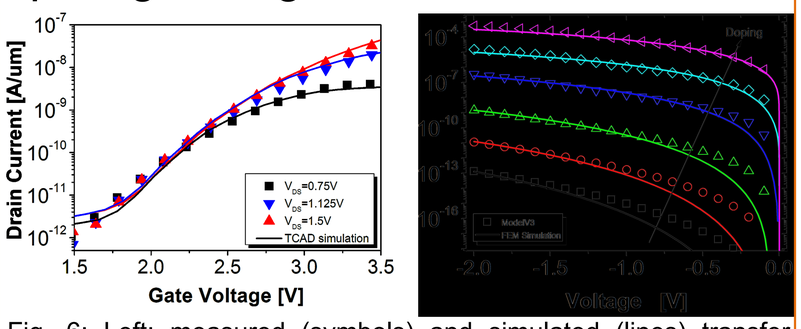

Fig. 6: Left: measured (symbols) and simulated (lines) transfer characteristics of realist TFET devices. Right: comparison between the analytical model (symbols) and the simulated current (lines) of a reverse-biased symmetric p-n junction device with doping levels ranging from 3 □ 10^{18}cm^{-3} to 1□10^{21}cm^{-3}.

CONCLUSIONS A proper modeling of TFET devices requires full quantum approaches which are very demanding from a computational point of view when applied to realist devices. The benchmarking of FEM simulations with advanced quantum transport models and against experimental datas, show that TCAD tool is a mature technique allowing for device optimization and helping the development of analytical and compact model necessary for the success of Tunnel-FET technology.

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