Lateral InAs/Si p-Type Tunnel FETs Integrated on Si—Part 2: Simulation Study of the Impact of Interface Traps

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***Abstract*— This part of the paper presents TCAD simulations of the InAs/Si lateral nanowire (NW) tunnel FET (TFET) with the same geometry as the fabricated device discussed in the first part. In addition to band-to-band tunneling, trap-assisted tunneling (TAT) at the InAs/Si and InAs/oxide interfaces was considered. A very good agreement is found between the simulation results and experimental transfer characteristics of different devices. The simulations confirm that the transfer characteristics in the subthreshold regime of the TFETs are entirely dominated by TAT. Due to the high concentration of generation centers at the InAs/Si interface, the current conduction in the subthreshold regime takes place in two steps: carrier generation by TAT at the InAs/Si interface followed by thermionic emission over the hole barrier. The latter is the limiting process, and hence dominant for the subthreshold swing (SS), preventing a value smaller than 60 mV/decade. In addition, traps at the Si/oxide interface reduce the electrostatic coupling between the gate and the channel, which further degrades the SS. Predictive simulations with varying interface trap densities indicate that a subthermal SS would only be achievable for $D_{it} < 5 \times 10^{11}$ cm^{-2}eV^{-1} at *both* InAs/Si and InAs/oxide interfaces. This confirms a recently found minimum requirement of $D_{it} < 1 \times 10^{12}$ cm^{-2}eV^{-1} for vertical InAs/Si NW TFETs with larger diameters.**

***Index Terms*— InAs/oxide interface, InAs/Si interface, interface traps, tunnel FETs (TFETs).**

I. Introduction

ENERGY scaling of integrated circuits has hit a road block as the operating voltage of the MOSFET-based solid-state switches has attained a minimum possible value. The thermionic emission mechanism, which governs the switching of the MOSFETs, does not allow to achieve an SS below 60 mV/decade at room temperature. For a subthermal SS, it is necessary to utilize a device that does not operate on thermionic emission. The tunnel FETs (TFETs) working on the principle of band-to-band tunneling (BTBT) are considered a potential candidate to replace MOSFETs as solid-state switches [1]. Although simulations have predicted that ideal hetero-TFETs can achieve a subthermal SS, the fabrication of a TFET with sufficient ON-current and subthermal SS over a few decades of drain current remains to be achieved.

Nonidealities in a TFET, such as generation centers at the interface (for brevity called traps in the following), band tails in the semiconductor, and surface roughness, exhibit strong influence on TFET characteristics in the subthreshold regime. Among all the nonidealities, interface traps have the strongest impact [2]. BTBT features a weak temperature dependence arising from the temperature dependence of the bandgap, whereas trap-assisted tunneling (TAT) has a stronger temperature dependence due to the involvement of phonons. The considerable temperature dependence of measured TFET characteristics reported by various groups hints to the major role played by interface traps [3]–[5]. Therefore, analyzing TFET characteristics necessitates the inclusion of the effect of traps in addition to BTBT.

In this paper, we analyze the measured transfer characteristics of lateral InAs/Si heterojunction TFETs presented in part-1. These devices have a best SS value of 67 mV/decade, fairly close to the thermionic limit. By simulation, we will untangle the role played by TAT, BTBT, and thermionic transport in their operation. Based on the analysis, we give an estimate for the D_{it}, which would allow a subthermal SS.

This paper is organized as follows. Section II presents the simulation setup for modeling BTBT and TAT. Section III provides simulation results and a discussion on the contribution of TAT and the mechanisms of operation of the TFET. The conclusions are presented in Section IV.

II. Simulation Setup

A. Device Geometry

TFETs were made from InAs/Si nanowires (NWs) with a cross section of 30 nm × 30 nm, laterally placed on buried oxide. Two of the fabricated devices were selected for the

Manuscript received June 6, 2016; revised July 13, 2016, August 16, 2016, and August 19, 2016; accepted September 16, 2016. Date of publication October 4, 2016; date of current version October 20, 2016. This work was supported by the European Community's Seventh Frame-work Programme under Grant 619509 through Project E2SWITCH.

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Digital Object Identifier 10.1109/TED.2016.2612484

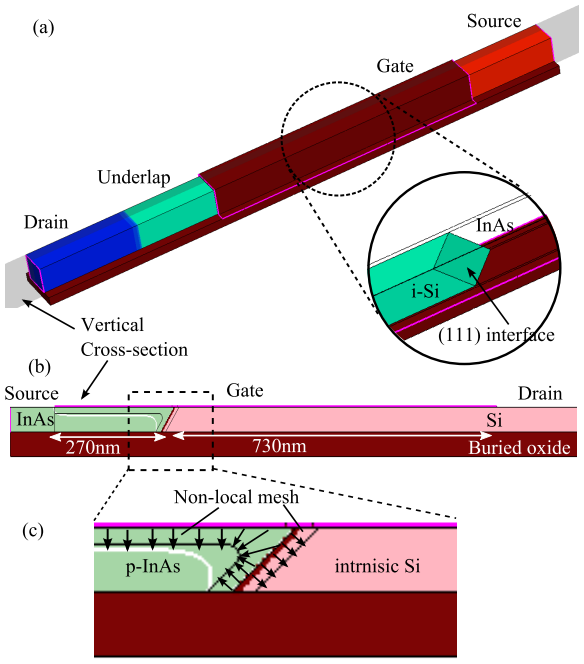


Fig. 1. (a) 3-D simulation domain of the InAs/Si lateral NW TFET along with the plane of vertical cross section. Inset: inclination of the ⟨111⟩ InAs/Si interface to the channel direction, where gate oxide and InAs regions were made transparent. (b) 2-D cross section of the device with various lengths. (c) Nonlocal mesh generated to model TAT at the InAs/oxide and InAs/Si interfaces.

simulation study, namely, FF44 and FF41 (for more details, see part-1 of this paper). An intrinsic underlap region between i-Si channel and p^+-Si drain is present in FF44, while no such underlap exists in FF41. The InAs region is n^+-doped with a concentration of 2×10^{18} cm^{-3}. The section of Si in the channel and the underlap region are intrinsic. The overlap between the InAs source with the gate is 270 nm long while that between Si and the gate is 730 nm long. The simulated underlap region in FF44 has an extension of 100 nm. The gate oxide consists of HfO_2/Al_2O_3 with an effective oxide thickness (EOT) of 1.75 nm. A vertical cross section of the device at the midpoint along the width of the NW [Fig. 1(a)] was simulated using the commercial simulator S-Device [9]. Since the channel orientation is along the ⟨100⟩-direction while the InAs/Si interface is a (111)-plane, the InAs/Si interface in the cross section is slanted, making an angle of 45^0 with the buried oxide. It must be noted that the device does neither possess a symmetry axis nor a plane of symmetry. A vertical cross section was selected for 2-D simulations to lower the computational burden, but some 3-D simulations were also done for validation purposes.

As observed in the TEM images in part-1, the thicknesses of InAs source and Si channel differ by about 5 nm, creating a step at the InAs/Si interface. Simulations with and without this step show that its impact on the transfer curves is negligible in the subthreshold region. The inclusion of the step slightly changes the ON-current, but the mechanism of operation remains unchanged. Therefore, a step at the InAs/Si interface will be ignored in the following.

TABLE I
VALUES OF VARIOUS BAND STRUCTURE PARAMETERS REQUIRED FOR THE KANE MODEL

Parameter	Unit	InAs	Silicon
		Direct gap	Indirect gap
E_g	eV	0.36	1.11
ΔE_C	eV	0.88	
ΔE_V	eV	0.13	
$m_C\langle 100\rangle$	m_0	0.023	0.19
$m_{LH}\langle 100\rangle$	m_0	0.026	0.147
Degeneracy (g)	1	2	2

B. Miscellaneous Physical Models

The dynamic nonlocal path BTBT model in S-Device [9] was used for the simulation of tunneling. It is based on Kane's two-band theory of BTBT [10], [11] and involves integration over the imaginary dispersion along all possible tunnel paths. This model requires the direct conduction band (CB) and light hole (LH) effective masses, the direct bandgap, and the degeneracy factor to simulate BTBT between the Γ−valley and the VB. Table I lists the values of various band structure quantities used in the simulation [7]. The temperature dependence of the bandgap was modeled following Varshni [6] with default parameters in S-Device. The temperature dependence of the effective masses was ignored. Tunneling from the Si LH band to the InAs CB is the primary BTBT process in this device. The degeneracy factor ($g = 2 \times g_C \times g_V$) for this process is 2.[1] Therefore, the degeneracy factor for BTBT in Si was set to 2, although the factor is 12 for intramaterial tunneling in Si. Owing to the large effective mass of heavy holes (HHs), tunneling between the Γ-valley of the CB and the HH band was ignored. The VB offset between InAs and Si was chosen to be 130 meV referring to the experimental data in [8]. Due to the small bandgap of InAs, Shockley–Read–Hall generation is strong and was modeled with constant lifetimes of 1×10^{-9} s. These values provided the best fit to the temperature dependence of reverse IV-curves of unintentionally doped InAs/Si hetero-NW diodes [12]. The gate work function was set to 5.05 eV and the source-drain bias was 500 mV in all simulations presented in this paper. As explained in part-1, the Schottky barrier at the source contact is expected to introduce a contact resistance visible at high gate bias. In TFETs, the impact of the contact resistance is usually very small due to the relatively low current densities. Therefore, the barrier at the source contact is expected to have only minimal impact on the device characteristics. It is, therefore, ignored in the simulations.

C. Modeling Trap-Assisted Tunneling

TAT takes place through excitation of electrons from the valence band to the trap state and subsequent emission of the

[1] In the calculation of the degeneracy factor it is assumed that tunneling is a spin-conserving process. Therefore, $g_C, g_V = 1$ for direct tunneling between CB and LH band as an electron can only tunnel between states having the same spin. Because there are two degenerate spin states in each band, an additional factor 2 enters the equation making $g = 2$.

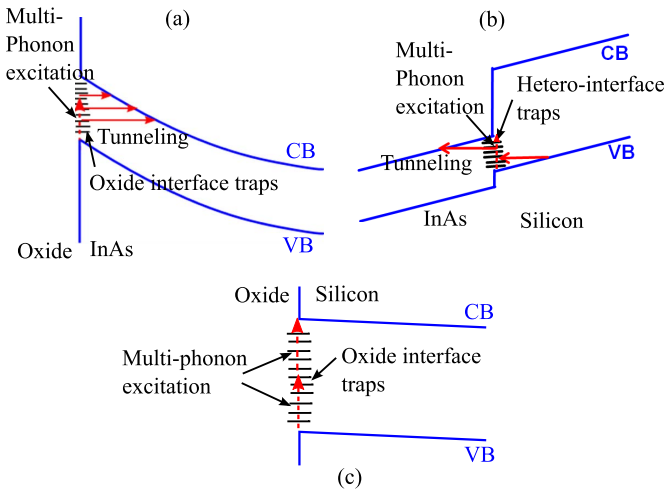


Fig. 2. Schematic showing TAT at (a) oxide/InAs interface, (b) InAs/Si interface, and (c) oxide/Si interface.

trapped electrons to the CB or vice versa. The occupancy of a trap state is determined by the principle of detailed balance taking into account all trapping and detrapping processes. The total trap occupancy at any interface determines the charge density at the respective interface, which changes the electrostatics of the device self-consistently. In the given TFET, the following TAT processes are dominant.

1) InAs/Oxide Interface: In this TAT process, an electron is captured by a trap state from the VB of InAs by a multiphonon excitation process. The trapped electron is emitted into the CB through either multiphonon excitation or phonon-assisted or direct tunneling [Fig. 2(a)]. The multiphonon excitation of electrons was modeled by the phenomenological V-model, which assumes temperature-independent capture cross sections and the thermal velocity to calculate the carrier capture-emission rate. Phonon-assisted and direct tunnel processes were modeled by a nonlocal model, which calculates the tunnel rate in WKB approximation with numerical integration over the imaginary dispersion [13]. The model was activated on the nonlocal mesh that was constructed adjacent to the InAs/oxide interface.

2) InAs/Si Interface: In this process, an electron from the Si VB can be trapped through both a multiphonon excitation and a (direct or phonon-assisted) tunneling process [Fig. 2(b)]. Similarly, a captured electron can be emitted to the InAs CB through either of these two processes. Similar to the case of the InAs/oxide interface, multiphonon excitation of electrons was modeled by the phenomenological V-model, whereas phonon-assisted and direct tunnel processes were modeled by the nonlocal model. The nonlocal model was activated on the nonlocal mesh that runs on either side of the InAs/Si interface and that was constructed normal to the interface.

3) Si/Oxide Interface: Depending on the fabrication process, traps may be also present at the Si/oxide interface. Since Si is intrinsic in the channel, a triangular-like potential well does not form. With increasing gate bias, the Si channel enters the accumulation mode, in which holes accumulate in the entire region without significant band bending. In the absence of band bending, TAT does not occur. Instead, an electron is captured through multiphonon excitation from the VB and subsequently emitted to the CB through another multiphonon process [Fig. 2(c)]. This kind of generation was modeled using the phenomenological V-model. Traps at the Si/oxide interface were not included in the simulation of FF44 devices as their impact was negligible. However, they had to be included in the simulation of FF41 devices.

TABLE II
VALUES OF TAT PARAMETERS REQUIRED FOR LOCAL AND NONLOCAL TAT MODELS

Parameter	Unit	InAs/Si	InAs/oxide
Non-local TAT model			
Huang-Rhys factor (S)	-	3	3
Phonon energy ($\hbar\omega$)	eV	0.06	0.06
Trap Volume	$Å^3$	50	10
Local V-section model			
Cross-section	$Å^2$	10	10
Thermal velocity	cm/sec	2.042×10^7	7.57×10^7

The V-model for multiphonon excitation has two parameters: capture cross section and thermal velocity, while the nonlocal model for direct and phonon-assisted tunneling contains three parameters, namely, trap interaction volume, Huang–Rhys factor, and phonon energy. The values of these parameters for both interfaces are provided in Table II. Both the models calculate capture and emission rates for each discrete trap level in the bandgap. The rates are proportional to the trap density. The nonlocal model requires effective electron and hole masses to perform integration over the imaginary dispersion relations. Effective electron and hole masses in bulk InAs and Si (given in Table I) have been used for the nonlocal TAT model.

The energetic trap distribution at the InAs/oxide interface was assumed to be uniform throughout the InAs bandgap. The trap density at the InAs/oxide interface was set to its measured value of 1×10^{13} $\text{cm}^{-2}\text{eV}^{-1}$ taken from [14]. At the InAs/Si interface, the energetic distribution of traps was assumed to have Gaussian shape with a peak concentration of 6×10^{13} $\text{cm}^{-2}\text{eV}^{-1}$, a full-width-half-minimum (FWHM) of 0.11 eV, and the peak position at the VB edge of InAs (see Section III for a more detailed discussion). For the simulation of FF41 TFETs, the trap density at the Si/oxide interface was assumed to be uniform throughout the bandgap of Si. Its value was set to 4×10^{12} $\text{cm}^{-2}\text{eV}^{-1}$ after fitting the experimental data.

III. RESULTS AND DISCUSSION

A. Temperature Dependence

The FF44 TFET [see Fig. 1(b)] was simulated by including the traps at the InAs/Si and InAs/oxide interfaces and using the model parameters outlined in Section II. A comparison of simulated and measured transfer characteristics is shown in Fig. 3. The used model parameters are mostly experimental data; only Huang–Rhys factor, trap interaction volume, and trap density at the InAs/Si interface, which are related to

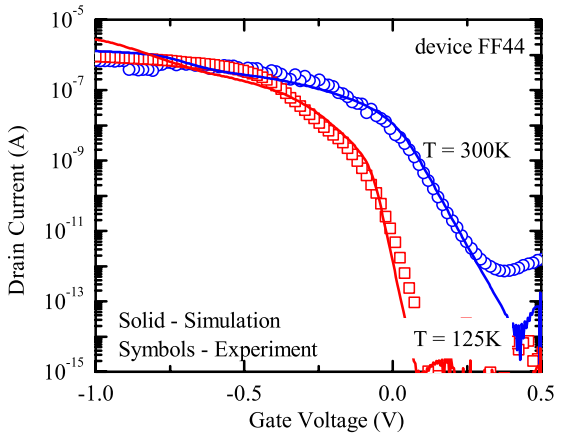


Fig. 3. Comparison of experimental and simulated transfer characteristics of FF44 TFETs for two different temperatures.

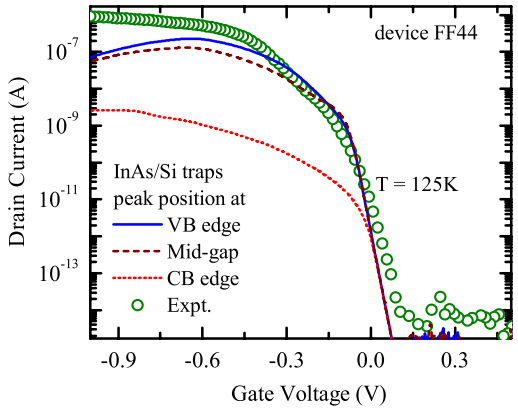


Fig. 4. Variation of the peak position of the Gaussian D_{it} in the bandgap of InAs at the InAs/Si interface. Only TAT at the InAs/Si interface was enabled in the simulation.

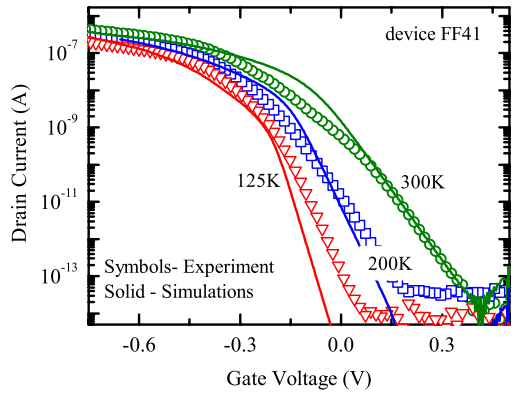


Fig. 5. Measured and simulated transfer characteristics of the FF41 TFETs for three different temperatures.

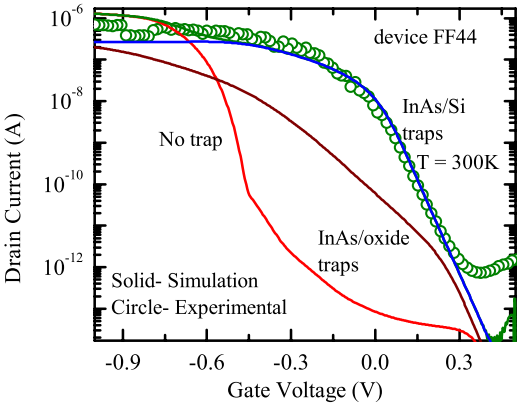


Fig. 6. Individual contributions of BTBT and the two TAT processes at 300 K in the simulated transfer characteristics of FF44 TFETs. TAT is dominant in the subthreshold region.

the TAT model, have been fitted to obtain a good match to the experimental data. It is observed that the variation of the Huang–Rhys factor has only a small effect on the transfer characteristics. The trap interaction volume merely acts as a scaling factor in the expression for the capture rate. A small change in the trap interaction volume will not cause a significant shift in the transfer characteristics on log scale. Therefore, they are little affected by the uncertainty associated with these two parameters.

The energetic trap distribution at the InAs/Si interface affects the electrostatics of the device as well as the capture and emission rates. At 125 K, the contribution from oxide traps to the transfer characteristics is negligible. Therefore, the low-temperature characteristics can be used to study the distribution of traps at the InAs/Si interface. A Gaussian shape was assumed for D_{it}, and the position of the peak was varied throughout the InAs bandgap, keeping the FWHM fixed to 0.11 eV. Fig. 4 shows the transfer characteristics of the TFET at 125 K for three different peak positions in the bandgap of InAs along with the experimental data. Best agreement is obtained for a peak position close to the VB edge of InAs. The output characteristics of the FF44 TFETs are presented in Fig. 5(b) of part-1. Good agreement between experimental and simulated output characteristics further validates the above simulation setup.

The FF41 TFETs were also simulated using the same simulation setup. Fig. 5 shows the comparison of simulated transfer characteristics with experimental data at different temperatures. Unlike in the analysis of the FF44 TFETs, traps at the Si/oxide interface had to be included for a good fit. Because of the large bandgap of Si, multiphonon excitation of electrons through traps at the Si/oxide interface is a less important process. Instead, the charging of these interface traps impacts the transfer characteristics by degrading the coupling between the gate electrode and the Si channel as explained below.

B. Individual Contributions of Various TAT Processes

At 300 K, the drain current originates from three sources: BTBT, TAT at the InAs/oxide interface, and TAT at the InAs/Si interface. The contribution of the individual mechanisms is shown in Fig. 6 for the case of device FF44. Note that the remaining components had to be disabled, which neglects the effect of the self-consistent coupling of all sources. TAT at both interfaces begins at a lower gate bias than BTBT as the effective tunnel gap for TAT is much smaller than that for BTBT. The drain current component due to TAT at

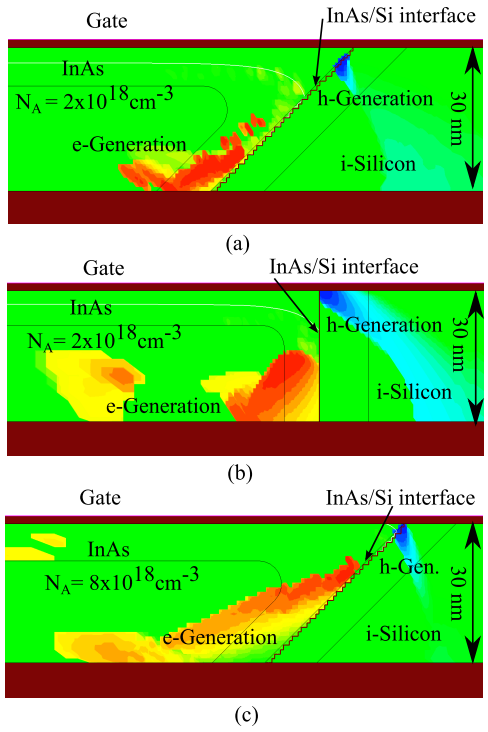


Fig. 7. Color-mapped diagrams of electron and hole generation rates at (a) inclined InAs/Si interface, (b) vertical InAs/Si interface with moderate source doping, and (c) inclined InAs/Si interface with high source doping. In all the cases, the gate voltage was $V_{GS} = 0.2$ V.

the InAs/oxide interface increases much more gradually and has a higher SS than the one originating from traps at the InAs/Si interface. The reason is the weak bias dependence of the multiphonon excitation step at the InAs/oxide interface. On the other hand, the drain current component from TAT at the InAs/Si interface yields an SS close to 60 mV/decade at 300 K. This astonishing coincidence will be explained in Section III-C.

The onset voltage of the TFET is fully dominated by TAT. The contribution of BTBT is negligible at the onset. However, the ON-current is determined by BTBT, as it becomes the dominant mechanism at high gate bias. The overestimation of the simulated ON-current at very high gate bias (see Fig. 3) is due to the neglect of quantization effects [15]. Furthermore, the effect of the slant in the InAs/Si interface along the z-axis is neglected in 2-D simulations, which also results in an overestimation of the drain current at high gate bias.

C. Impact of Inclined InAs/Si Interface on BTBT

The simulated transfer characteristics in the absence of traps are unusual as they exhibit a very weak slope at the onset. As seen in Fig. 6, the drain current gradually increases at a lower bias (-0.3 V $< V_{GS} <$ 0.3 V), which can be attributed to the slanted InAs/Si interface. As demonstrated in Fig. 7(a), the tunnel path connecting the electron and hole generation centers is long for a TFET with a slanted InAs/Si interface. Also the gate control is weaker as the electron generation center is far away from the gate and shielded by the carriers in the inversion layer. Both factors result in a gradual increase of the drain current. Note that the same behavior is also observed in

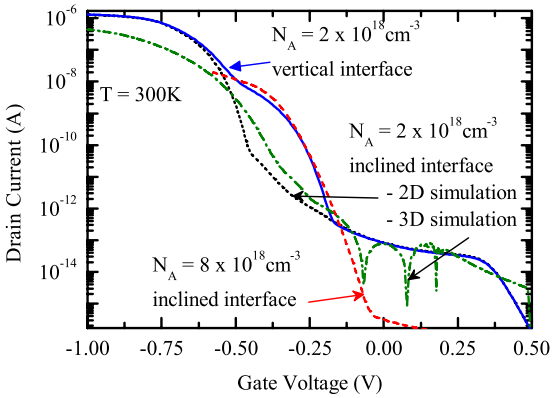


Fig. 8. Simulated transfer characteristics of an ideal lateral InAs/Si NW TFET without traps for different device geometries and source doping levels. A vertical InAs/Si interface or high source doping can result in a sharp onset of the drain current.

the transfer characteristics obtained by 3-D simulations with the exact device geometry (see Fig. 7), which suggests that it is not an artifact of simulating a 2-D cross section. A vertical InAs/Si interface would shift the center of electron generation closer to the gate and would reduce the tunnel length, as shown in Fig. 7(b). This greatly improves the transfer characteristics, as shown in Fig. 8. For the given TFET with the slanted InAs/Si interface, only the increase of the InAs source doping can improve the BTBT current slope, as demonstrated for a value of 8×10^{18} cm^{-3}. This is a result of the reduced tunnel length [see Fig. 7(c)]. However, in the real TFETs, the drain current component due to BTBT is completely dominated by the TAT current. Therefore, the above alterations will improve the subthreshold characteristics only after suppression of TAT.

D. Mechanism of Operation

The SS extracted from the measured characteristics of the TFET is 70 and 35 mV/decade at 300 and 125 K, respectively. Contrary to the weak temperature dependence of an ideal TFET, the SS is roughly proportional to the temperature here, which is a characteristic of thermionic emission. Fig. 9 explains the reason for this anomaly observed in the experiments and the simulations. The band diagram along the channel of the TFET [Fig. 9(a)] for different gate bias values clearly reveals a large thermionic barrier. This causes a two-step current conduction process: TAT at the InAs/Si interface and subsequent transport of holes to the drain by thermionic emission. The barrier is lowered with increasing negative gate bias. In the subthreshold regime, the thermionic barrier is high, and thermionic emission of holes becomes the rate-determining step. Therefore, the slope of the drain current is typical for a thermal SS. At a higher gate bias, when the barrier is sufficiently low, TAT at the InAs/Si interface becomes the bottleneck and the drain current becomes determined by TAT. The two regimes in the transfer characteristics are clearly distinguishable at 125 K, as shown in Fig. 9(b). In short, the TAT leakage current is blocked by the thermionic barrier, which gradually releases the blockade with the increasing negative gate bias. This results in an SS dominated by the thermionic emission mechanism. In this way, the presence of a high trap density at the InAs/Si interface causes the TFET

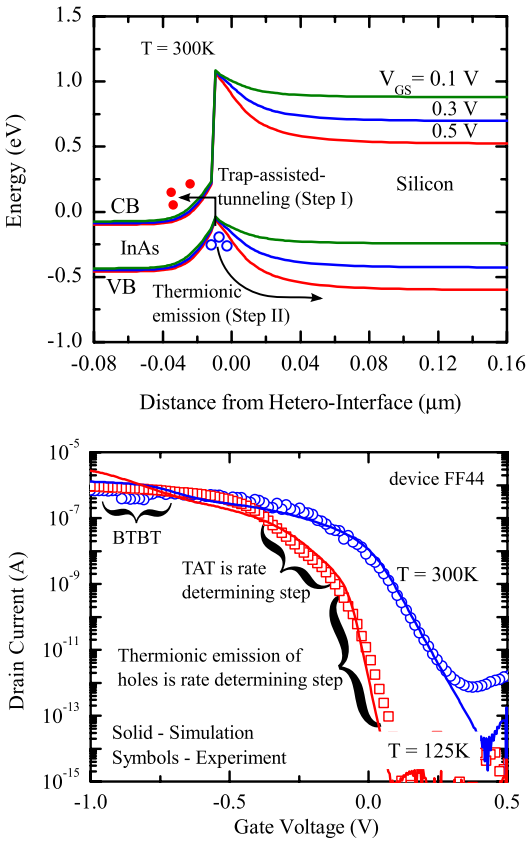


Fig. 9. (a) Band diagram along the channel for three different gate bias values near the onset of the TFET. In the presence of traps at the InAs/Si interface, transport of carriers happens via two subsequent steps, viz., TAT and thermionic emission. Note that the VB offset at the InAs/Si interface is 130 meV although it is not visible in the band edge diagram. This is due to the discretization at the interface, which linearizes the otherwise abrupt band offset, and due to the high electric field, which gives rise to a sharp gradient at the interface making it difficult to distinguish the band offset. (b) Two separate intervals in the transfer characteristics with dominant mechanisms in respective intervals.

to operate like an MOSFET with the intrinsic Si region as a gated channel.

E. Effect of Traps at the Si/Oxide Interface

In the analysis of FF44 TFETs, traps at the Si/oxide interface could be ignored. However, such traps seem to have a strong impact on FF41 TFETs, possibly due to a higher concentration as result of process variations. The presence of defects at the heterojunction is likely a somewhat stochastic effect, which could cause a variation in trap density from one device to another. The effect of Si/oxide traps is highlighted in Fig. 10, which compares the transfer characteristics of FF41 TFETs with and without Si/oxide interface traps. It can be explained as follows. When Si/oxide traps are included, the slope of the transfer characteristics changes in the region where it is dominated by thermionic emission. Traps at the oxide/Si interface introduce an additional capacitance in parallel with the depletion layer capacitance, which degrades the electrostatic coupling between the gate and the intrinsic Si channel [16]. The reduced gate coupling increases the SS from its ideal value to 81mV/decade for the above devices at 300 K.

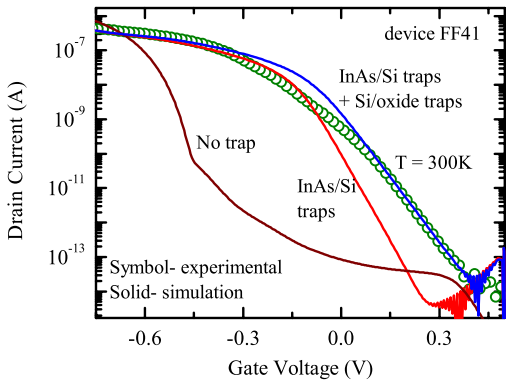
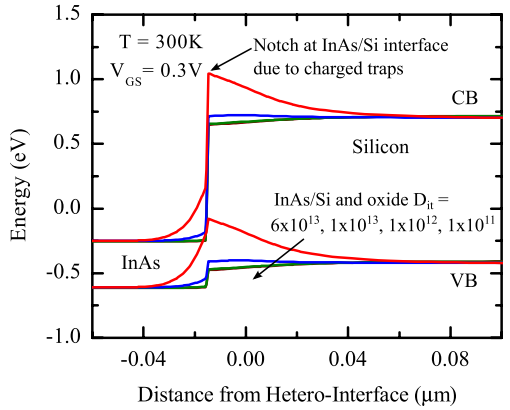


Fig. 10. Effect of Si/oxide traps on the transfer characteristics of FF41 TFETs. Si/oxide traps reduce the electrostatic coupling between gate and channel. This degrades the SS similar to what is observed in a MOSFET.



(a)

Fig. 11. Band diagram along the channel of the device for different interface trap densities (V_{DS} = 0.5 V).

This effect is similar to what is observed in MOSFETs in the presence of oxide interface traps. The generation rate of carriers by multiphonon excitation is weak at this interface due to large bandgap of Si. Thus, the degradation of the SS due to Si/oxide traps can be entirely attributed to the reduced gate coupling.

It must be noted that a gate work function of 4.9 eV was used in the simulation of FF41 devices as compared to 5.05 eV for the FF44 devices. This change could result from trapped oxide charges.

F. Prediction for D_{it} Limits

Having achieved good agreement between the experimental and simulated TFET characteristics, the above simulation setup can be utilized to study the impact of a given D_{it} on the SS. Simulations were carried out for different trap concentrations at the InAs/oxide and InAs/Si interfaces. A source doping of 8×10^{18} cm^{-3} was used in these simulations, as it is optimal for the given device geometry. The band diagram along the channel of the device (Fig. 11) shows that a very high trap density may result in the formation of a notch at the heterointerface, creating a thermionic barrier for hole transport. At a somewhat lower trap concentration, the thermionic barrier vanishes and the

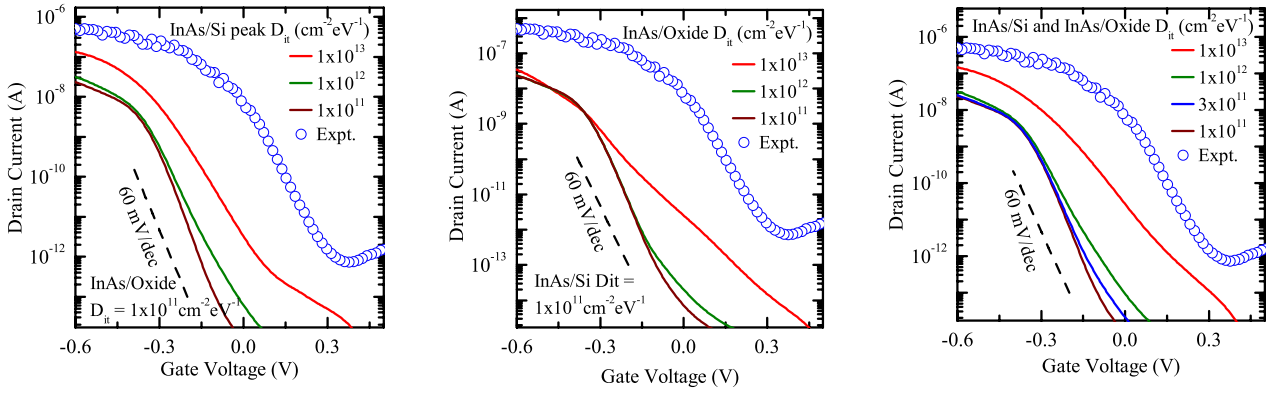


Fig. 12. Predictive simulations to study variation of interface trap density at (a) InAs/Si interface, (b) InAs/oxide interface, and (c) both InAs/Si and InAs/oxide interfaces.

transfer characteristics are solely determined by TAT. The resulting transfer characteristics qualitatively change when the trap density is reduced from 6×10^{13} $\text{cm}^{-2}\text{eV}^{-1}$ to 1×10^{12} $\text{cm}^{-2}\text{eV}^{-1}$, as shown in Fig. 12. It turns out that the device characteristics will degrade even if either of the two interfaces has a trap concentration above 1×10^{12} $\text{cm}^{-2}\text{eV}^{-1}$. Such a value was recently found as a minimum requirement for vertical InAs/Si NW TFETs with larger diameters [17]. As a more conservative estimate, the interface trap concentration at both the InAs/Si and InAs/oxide interfaces needs to be close to 5×10^{11} $\text{cm}^{-2}\text{eV}^{-1}$ to enable an SS < 60 mV/decade.

IV. Conclusion

InAs/Si lateral NW gate-overlapped-source TFETs were simulated taking into account not only BTBT but also TAT processes at the InAs/Si and InAs/oxide interfaces. It was confirmed that the TAT current begins at a lower gate bias than BTBT. Therefore, the interface traps determine the TFET characteristics in the subthreshold regime. In TFETs with a high trap concentration at the InAs/Si interface, current conduction takes place in two steps. electron–hole pairs are generated at this interface by a TAT process, which is followed by thermionic emission of holes to the drain. In the subthreshold regime, due to the presence of a high thermionic barrier, thermionic emission of holes is the rate-determining step. At higher gate bias, when the thermionic barrier is sufficiently lowered, TAT becomes the rate-determining step. Simulations of FF41 TFETs suggest that in addition to the above mechanisms, traps at the Si/oxide interface further degrade the SS of the devices by reducing the coupling between the gate and the Si channel. Predictive simulations with different D_{it}-values have shown that $D_{\text{it}} = 5 \times 10^{11}$ $\text{cm}^{-2}\text{eV}^{-1}$ is the maximum allowable value that still would result in a subthermal SS.

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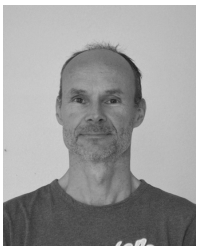

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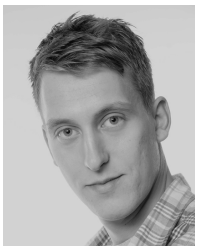

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