A Comparison of Advanced Transport Models for the Computation of the Drain Current in Nanoscale nMOSFETs

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Abstract:

In this paper we compare advanced modeling approaches for the determination of the drain current in nanoscale MOSFETs. Transport models range from Drift-Diffusion to direct solutions of the Boltzmann Transport equation with the Monte-Carlo method.

Template devices representative of 22nm Double-Gate and 32nm Single-Gate Fully-Depleted Silicon-On-Insulator transistors were used as a common benchmark to highlight the differences between the quantitative predictions of different approaches. Using the standard scattering and mobility models for unstrained silicon channels and pure SiO_2 dielectrics, the predictions of the different approaches for the 32nm template are quite similar. Simulations of the 22nm device instead, are much less consistent, particularly those achieved with MC simulators. Comparison with experimental data for a 32nm device shows that the modeling approach used to explain the mobility reduction induced by the high-κ dielectric is critical. In the absence of a clear understanding of the impact of high-κ stack on transport, different models, all providing agreement with the experimental low-field mobility, predict quite different drain currents in saturation and in the sub-threshold region.

1 Introduction

Many modeling approaches for the determination of the drain current I_{DS} in MOSFETs are currently used and developed. One of the main reasons driving these modeling efforts is the industry need to understand performance improvements due to quasi-ballistic transport and other technology boosters such as strain, high-κ dielectrics and Ultra-Thin-Body Silicon-On-Insulator (SOI) architectures [1]. The possible modeling approaches can be grouped in a few *families* which range from modifications of the conventional Drift-Diffusion (DD) model used in commercial TCAD tools to advanced Monte-Carlo [2] (MC) and Non-Equilibrium-Green's-Function (NEGF) simulators [3] able to handle the strongly off-equilibrium transport taking place in decananometric devices. Even inside a given *family* of simulation approaches, many options are possible e.g. handle quantization in the inversion layer or other physical effects. For example in the MC family some models based on the free-electron gas [4, 5, 6] neglect quantization, while others adopt quantum corrections [7, 8, 9]. Models based on a Multi-Subband description of the carrier gas [10, 11, 12] and approaches based on the solution of the Wigner Equation [13, 14] instead, explicitly incorporate quantum mechanical effects. Similar distinctions apply also to Drift-Diffusion simulators.

A transparent and thorough assessment of these models is not trivial. Validation by direct comparison with experimental data is often unable to rule out possible model inaccuracies, since many parameters of the experimental devices, such as doping profiles and series resistances, which play a critical role in determining I_{DS}, are not precisely known and are often used as adjusting parameters.

Comparison between simulations of the same devices performed with different models represents a simple and sound methodology to identify and quantify the impact of the assumptions taken by the different models. Examples of this methodology are [15, 16, 17, 18], works that, in

our opinion, have increased the awareness and the confidence of the electron device community in the capabilities of device modeling.

In this paper we have followed an approach similar to the one in [15, 16, 17, 18]. We have first defined template (idealized) devices: a 32nm Fully-Depleted-SOI (FDSOI) and a 22nm Double-Gate (DG) device, both optimized for low-stand-by-power applications. Then we have simulated them with the available modeling approaches, all previously calibrated on the universal mobility curves [19]. Results in terms of low-field mobility, drain current and internal quantities (concentration and velocity) have been compared. This provides us an estimate of the degree of convergence between the different transport models in aggressively scaled devices. We have then applied the models to the simulation of a real device (a 32nm FDSOI similar to one of the template devices), paying special attention to the modeling of the mobility reduction induced by the use of high-κ dielectrics. In particular, the scattering and mobility models have been calibrated on the experimental low-field mobility, then the simulated drain current has been compared to the experimental data without any further adjustment.

The paper proceeds as follows. The template devices are described in Section 2. An overview of the simulation approaches is provided in Section 3. The results of the comparison between models carried out on the template devices are reported in Section 4. Comparison between simulation and experimental data for a 32nm device is presented in Section 5. Conclusions are finally drawn in Section 6.

2 Simulated Devices

The 32nm FDSOI template is sketched in Fig.1. The channel is lowly doped (10^{15}cm^{-3}). The substrate is p-type (N=10^{18}cm^{-3}). The metal work-function is 4.6eV. The gate stack consists of 2.3nm of HfO_2 on top of 0.8nm of SiO_2 (EOT=1.2nm). The spacer is made of Si_3N_4 and comes in direct contact to the silicon. Doping profiles for the S/D regions have been obtained from

process simulations of a realistic 32nm process. As we will see in Section 5, experimental data for a device similar to this template are available and will be compared with the predictions of the various simulation models. At this stage, before arriving to Section5, we will denote with *32nm FDSOI device* the idealized template, not the real device.

The 22nm DG device is an idealized Double-Gate MOSFET with a gate length of 22nm, a gate stack consisting of 2.4nm of HfO_2 on top of 0.7nm of SiO_2 (EOT=1.1nm). The silicon film thickness is 10nm and the metal work-function is 4.8eV. The doping profiles are similar to the ones of the 32nm template, with all the diffusion lengths scaled by 22/32.

Both templates are n-type and feature unstrained Si channels.

3 Simulation Approaches

In the following, the key features of each model (identified with the acronym of the main developer) are presented. For a sake of a more transparent comparison we group the models in two families: the MC family, which collects models based on the direct solution of the Boltzmann-Transport-Equation (BTE) using the Monte Carlo method [2], and the DD family, which gathers drift-diffusion-like models where only the first momenta of the BTE are calculated.

3.1 MC family

UD-MSMC: Multi-subband ensemble Monte Carlo described in [20]. It provides the coupled solution of the effective-mass Schrödinger equation in each section of the device, of the system of coupled BTEs for each subband in the inversion layer and of the 2D Poisson equation. In this way quantization effects such as charge repulsion from the channel/dielectric interface, subband repopulation, dependence of the scattering rate on the size- and bias-induced quantization [21] are naturally taken into account. An analytical non-parabolic model is used for the energy dispersion of the subbands. A first order approach to include quantum effects in the transport

direction has been implemented as described in [22]. Scattering mechanisms included in the solution of the BTE are bulk phonons and surface roughness (SR), with the model described in [23]. The models for the scattering mechanisms related to high-κ dielectrics (remote-phonons and remote-charge) and used in Sec.5 are described in [24]. Ionized impurity (II) scattering in the S/D extensions is not active in these simulations, but series resistances extracted from DD simulations (R_S=R_D=90$\Omega \mu m$ for the 22nm template and 60$\Omega \mu m$ for the 32nm one) have been introduced as lumped elements. Vertical S/D contacts are placed just at the end of the spacers (x=26nm in Fig.1).

BO-MC: Full-band ensemble Monte-Carlo (free carrier gas) [25] with quantum corrections (effective potential). Scattering mechanisms include phonons, SR, II as well as carrier-plasmon in the S/D [26]. The model for SR is based on the extension to the free carrier gas of the model for the quasi-2D carrier gas, as described in [25]. II scattering in the S/D is calibrated to reproduce bulk mobility data for doping up to 10^{21} cm^{-3}.

ETH-MC: Full-band ensemble Monte Carlo (free carrier gas) with phonon, II and SR scattering [27]. The scattering physics is the same as in [28]. Quantum correction are not taken into account. SR is included using partially diffusive scattering at the SiO_2 interface with a Fuchs factor of 20%.

Numonyx-MC: Full-Band Ensemble Monte-Carlo [29] (free carrier gas) featuring quantization effects through a quantum mechanical correction of the potential that is computed by solving self-consistently the Schrödinger equation in each section of the device. The silicon anisotropic full-band structure is computed with the Empirical Pseudopotential Method [30]. Scattering mechanisms are assumed to be isotropic and include: elastic acoustic phonon scattering, inelastic optical phonon scattering, II scattering (according to the isotropic model of [28]), impact ionization. SR scattering is treated as in [31] i.e. by including both surface roughness and sur-

face phonon scattering mechanisms as a function of the average electric field weighted by the carrier concentration. Phonon scattering for electrons and holes has been extensively calibrated to reproduce a large variety of experiments including strain dependent mobility [29, 32, 33].

IEF-MC: Ensemble Monte Carlo described in [34]. Quantum corrections are not taken into account here and carriers are treated as a three-dimensional (free) gas in the simulator. We consider an analytical conduction band structure of silicon consisting of six ellipsoidal non parabolic Δ valleys located along the [100] directions at 85% of the Brillouin zone edge. The energy-dependent scattering rates are calculated prior to the simulation and stored in a look-up table used throughout the simulation. All relevant scattering mechanisms are included, i.e. electron-phonon, II and SR scattering, according to the models described in [35]. Throughout this work in this simulator and in the other MC simulators, we assume bulk phonon energies and the same coupling constants as in bulk Si without including possible effects on phonon dispersion related to ultra-thin layers.

UGLA-MC: 3D Monte Carlo simulator [36]. An efficient methodology is used for the fully self-consistent inclusion of 3D density gradient (DG) quantum corrections [37]. Efficient analytic ellipsoidal, non-parabolic band models are employed and all major phonon mechanisms required to calibrate to bulk mobility in Silicon are included. Within device simulation, carriers are treated as a free carrier gas and II scattering is included as in bulk via the Brooks-Herring formalism with static screening based upon the local carrier concentration and corrected for degeneracy. Ridley's third body exclusion is also incorporated in order that the scattering rate in regions of low carrier density is low enough to allow efficient simulation. SR scattering is included via Ando's model, using a rejection technique based upon the local perpendicular field, and has been calibrated to experimental universal mobility results.

3.2 DD family

BO-QDD: 1D drift-diffusion solver for SOI-MOSFETs combined with the solution of the coupled Schrödinger-Poisson equations on the device cross-sections normal to the transport direction [38]. The physical model thus accounts for the quantization due to both the structural confinement and the application of the transverse effective field by realistically computing the device electrostatics. The harmonization of the drift-diffusion model with the Schrödinger equation is pursued by means of Bohm's theory of quantum potential. The model requires the solution of as many drift-diffusion equations as the number of populated subbands. A physically-based unified mobility model has been incorporated in the QDD solver, which is an analytical function of the effective field and doping concentration. The model provides the effective mobility of the 2DEG in a SOI MOSFET channel by averaging the single-valley mobilities weighted with their respective valley populations. Elliptic parabolic bands for the six conduction valleys are assumed. The lowest subband energies of each valley derived from the Schröinger-Poisson solver are used to calculate the relative valley population by assuming Boltzmann statistics. For the single-valley mobilities, the model accounts for phonon scattering, Coulomb scattering and SR scattering, combined via Matthiessen's rule. More details about the mobility models are given in [39, 40]. Velocity saturation at high longitudinal fields is accounted for by means of the Caughey-Thomas formula [41] with $v_{sat} = 1.07 \times 10^7 cm/s$.

UGLA-aDD: 3D *atomistic* drift diffusion simulator [42]. It employs density gradient quantum corrections [43]. In this work, calibration has matched standard Dessis [44] simulations.

PI-MSDD: Multi-subband DD, i.e. self-consistent solution of the 2D Poisson and Schrödinger equations (in the direction perpendicular to the Si/SiO2 interface), coupled with the solution of the continuity equation along subbands in the DD approximation [45, 46]. The low field mobility of [47] has been implemented, while the approach described in [48] has been adopted

for high electric fields.

3.3 Other transport approaches

UGLA-NEGF: Modified version [49] of the fully 2D NEGF simulator initially developed by NASA [50]. In this work scattering is not included, so that carriers move ballistically from source to drain.

WUT: Electron mobility model based on the relaxation time approximation, employing the Matthiessen's rule for different scattering mechanisms. It uses a 1D Poisson-Schrödinger solver which can handle both open and closed boundary conditions for the wave functions, and also different co-existing potential wells (or channels) may be considered independently. Electron mobility in multi-layered structures may be investigated, including bulk devices, SG and DG SOI devices, devices with strained-Si/SiGe channels and high-κ gate stacks. The phonon limited mobility is calculated within the isotropic approximation. The SR scattering model is based on the Ando's approach, modified to account for thickness fluctuations of the structure component layers [51, 52]. Contribution of roughness of each interface (front and back in the case of SOI) can be modeled independently. An exponential spectrum of roughness is employed. The Coulomb scattering limited mobility is obtained by determining screened scattering potentials from Coulomb centers and determining the corresponding relaxation times, following the approach presented in [53]. Influence of charges located in the channel, in the dielectric layers and at the corresponding interfaces may be considered.

3.4 Model calibration

The models described above differ in terms of band-structure, scattering models, treatment of non-local transport, etc. For the sake of a fair comparison, all simulators have been first calibrated to reproduce the universal curves in bulk Si devices (see Fig.2). More details about

about this step of the procedure can be found in the references provided in the previous sections.

At the time of the comparison, not all models contained all the ingredients to simulate advanced devices as the template transistors defined in Sec.2. In particular, some handle strained channels but not high-κ stacks. Furthermore, scattering models for options such as high-κ dielectrics are not well assessed yet, since there is still a debate about the relative contribution of remote-phonons [54] and remote-coulomb scattering [55], and a large spread exists between the prediction of the different models for remote-phonon scattering [24]. For these reasons, although the template devices described in Sec.2 include high-κ stacks, and although 32nm and 22nm devices are likely to include strained channels, when simulating the template devices we consider unstrained Si and neglect the scattering mechanisms induced by the presence of the high-κ dielectric. This latter aspect will be addressed in Sec.5 when comparing the various simulation approaches against experimental data for nanoscale MOSFETs featuring high-κ dielectric.

4 Results

In this section we report the results obtained by simulating the template devices of Sec.2 with the models described in Sec.3. In all the following figures we have used a consistent set of symbols, so that each model is always identified by the same symbol and type of line. All models of the MC family are identified by solid lines, whereas models of the DD family are identified by dashed lines.

4.1 Low-Field Mobility

We report in Figs.3, 4 the low-field mobility as computed in long channel devices with the same *vertical* structure as the 32nm FDSOI and 22nm DG templates. The mutual agreement between the different models is quite good at large inversion charges N_{inv}, in particular in the

32nm FDSOI template, whereas discrepancies appear at low N_{inv}, especially in the 22nm DG device. This is mainly due to the different treatment of phonon scattering in inversion layers in the various models.

Note that experimental effective mobility curves are different for poly gates and metal gates [55]. However, in this comparison we do not consider effects related to the gate material such as remote coulomb scattering, plasmons in poly-silicon.

4.2 Drain current in the 32nm template

Figs.5, 6 report I/V curves of the 32nm FDSOI template at low and high drain-source voltages, respectively.

Considering the models of the DD family, the figures show a more than satisfactory mutual agreement, that has been observed also below threshold (not shown).

Considering now MC models, which take into account more accurately the quasi-ballistic nature of carrier transport in short MOSFETs, the mutual agreement is quite satisfactory, much better of what has been found in [18], mainly because in the 32nm FDSOI device considered in this work the role of II scattering in the S/D regions is significantly reduced with respect to the devices in [18]. It is also interesting to note that different treatments of quantization (MSMC vs. quantum corrections vs. no quantization) and of different descriptions of the band structure (full-band vs. simple non-parabolic analytical bands) only have a marginal impact on the simulated current of this device.

As expected, the current provided by the MC models is larger than the one given by the DD ones at high V_{DS}, where non-equilibrium effects become significant. At low V_{DS}, instead, the two approaches give essentially the same current, as it is expected since the device works close to equilibrium. In some cases (ETH-MC vs. UGLA-aDD) current from DD is larger than from

MC, consistently with the failure of DD models also near equilibrium reported in [56].

4.3 Drain current in the 22nm DG template

Comparisons between the MC, DD and NEGF results for the 22nm DG template are reported in Figs.7, 8 for low and high V_{DS}, respectively.

Concerning the DD models, the overall agreement is essentially as good as for the 32nm device.

Concerning the MC models, at low V_{DS} the agreement between I_{DS} predictions is quite poor, but it improves for V_{DS}=1V. Possible explanations can be traced back to the different modeling of SR and phonon scattering in thin film Double-Gate SOI structures, since we have seen that also the differences in low-field mobility in this device are significant (see Fig.4) and the device works at lower effective field compared to the 32nm FDSOI template..

Since in the 22nm DG device the impact of II in the S/D regions is large (the series resistances extracted from DD simulations are $90 + 90\Omega\mu m$), we have performed MC simulations without II scattering to isolate the effect of the various scattering mechanisms on the spread between the simulation results. As it can be seen in Fig.9, without II the spread between the MC results is smaller than in Figs.7, 8, but still significant, especially at low V_{DS}, meaning that the different treatment of II scattering [18] implemented in the models is only one of the reasons for the spread between the MC results.

4.4 Summary of the comparison in terms of I/V curves

A direct mutual comparison between the families of models (DD, MC and NEGF) is summarized in Table.1. We see that:

a) DD and MC models provide quite similar I_{DS} at low V_{DS}, as it is expected since in this case the transport regime is close to equilibrium conditions;

b) ionized impurity scattering in the S/D is important, especially at low V_{DS}, where the voltage drop on the S/D regions is a significant fraction of the applied V_{DS};

c) purely ballistic transport models (as the NEGF solver used here) significantly overestimate the I_{DS} of these nanoscale devices, since they neglect scattering in the channel as well as in the S/D regions.

4.5 Internal quantities

To further investigate the origin of the discrepancies between the different modeling approaches, we have compared internal quantities (inversion charge and average velocity profiles) as obtained with the various simulators. Results are reported in Figs.10, 11 for the 22nm DG device and in Figs.12, 13 for the 32nm FDSOI.

The correlation between the spread of the drain currents and the spread in terms of average velocity is not so clear. The difference in the average velocity predicted by many models over a large fraction of the channel is often even larger than that in the corresponding drain currents, in particular for the 32nm FDSOI device (compare Fig.12 and Fig.6). In fact it is the velocity near the injection point (the so-called *virtual source*) that essentially controls the current drive of the device [57, 26]. In this respect, we see that the velocity in the DD models is limited to the saturation velocity (approximately $10^7 cm/s$), whereas the MC models feature peak velocities that can be more than two times larger, but the differences in terms of I_{DS} are significantly smaller (see Table 1). On the other hand these differences in terms of velocity have a large impact in the determination of the cut-off frequency [58] of the devices.

The differences in terms of inversion charge that can be observed in Figs.11, 13 in the central portion of the channel and close to the drain junction can be interpreted as differences in terms of velocity. In fact, also in the case of N_{INV}, it is the value at the virtual source that really

controls the current.

We have thus collected the inversion charge and average velocity at the virtual source for some of the modeling approaches, see Table 2. However also this comparison does not help too much in understanding the origin of the different model predictions. First of all, being all the approaches self-consistent, they provide different potential profiles, and thus different positions of the virtual source. Since in all cases the virtual source is in the region where the carrier concentration varies very rapidly over space (as it can be seen by mapping the x_{VS} data in Tab.2 in Figs.11, 13), small differences in x_{VS} translate in large differences in inversion charge (and thus in velocity) much larger than the differences in terms of drain current. This is consistent with what has been found in [59].

We have also verified that the product between the inversion charge and the electron velocity (which multiplied by the electron charge gives the current density per unit width) is essentially constant along the channel. Small fluctuations can be observed in some of the MC models, but they are much smaller than the differences in terms of drain current observed e.g. in Figs. 7, 8.

5 Comparison with experimental data

Devices similar to the template 32nm FDSOI described in Sec.2 have been fabricated by ST Crolles. An extensive characterization activity has been carried out, including determination of the low-field mobility in long channel devices, of the I/V curves in devices with gate length down to 30nm and of the source and drain series resistances. TEM images have been used for an accurate determination of the thickness of the different layers (SOI film, interfacial SiO_2 layer and high-κ material). The main differences between the template 32nm FDSOI described in Sec.2 and the fabricated devices are listed below: 1) the thickness of the interfacial layer is 1.3nm;

2) the high-κ material is $HfZrO_2$; we have assumed a dielectric constant of $15\epsilon_0$ in the simula-

tions;

3) the thickness of the high-κ layer is 1.9nm;

4) the doping below the BOX is $2 \times 10^{15} cm^{-3}$;

5) series resistances have been estimated as R_S=R_D=100$\Omega\mu m$ [60];

6) the device is strained: stress in the channel is transferred by a tensile cap liner around 500MPa (Contact etch stop layer); process simulations have shown that the stress level is strongly layout dependent, but that in large width devices (as the ones considered in the following), strain can be considered as uniaxial; the valley splitting induced by a strain level of 500MPa (approximately 10meV) and the corresponding variation of the transport mass ($0.18m_0$ instead of $0.19m_0$) are so small that have a negligible effect on the drain current. MSMC simulation with and without accounting for that show a drain current difference of about 5% for high as well as low V_{DS}.

Since the fabrication process is similar to the one on which we based the process simulations used to determine the S/D doping profiles of the template 32nm FDSOI, we have assumed that the fabricated devices have the very same S/D doping profile of the template 32nm FDSOI device, and we have used the latter in the simulations reported in the following. Since uncertainties in the orders of a few nanometers are possible, we have set L_G=32nm in the simulations, and compared the results with the experimental data for L_G=30nm and 35nm.

Comparison between experiments and simulations using the standard calibration parameters (reproducing Takagi's curves see Sec.3.4) are reported in Fig.14. The threshold voltage and the sub-threshold behavior are quite nicely reproduced without any adjustment of the device parameters, meaning that the knowledge of the doping profiles, gate length and gate stack is quite accurate. However above threshold, at low as well as at large V_{DS}, the simulated currents are significantly larger than the experiments.

The main origin of this discrepancy is that the measured low-field mobility is much lower than the universal curves, so that the standard calibration overestimates the mobility. In fact, we can see in Fig.15 that the simulations using the standard calibration described in Sec.3.4 (denoted by *std.param.*) provide a much larger mobility than the measured one. In order to account for this reduced mobility, some of the models have been re-calibrated following different strategies. Results are denoted as *adj.param.* in Fig.15. In the UD-MSMC we have attributed the mobility reduction to the presence of charge at the ITL/high-κ interface. A concentration of $2 \times 10^{14} cm^{-2}$ is required in order to reproduce the experimental data. The WUT's model reproduces the experimental data by placing a concentration of charge of $8.8 \times 10^{12} cm^{-2}$ at the Si/ITL interface. In ETH-MC, the Fuchs factor for surface roughness is modified from 20% to 65%. In Numonyx-MC the local scattering by ionized impurities is artificially increased in the channel to mimic the effect of charge in the gate stack. On the other hand, BO-QDD includes a mobility model with remote-phonons and remote-coulomb-scattering. Experimental data are reproduced by assuming a charge concentration of $1.9 \times 10^{13} cm^{-2}$ at the ITL/high-κ interface.

Clearly the difference in the models and in the the model parameters indicate that no consensus has been reached yet about the explanation of the mobility in advanced devices with high-κ stacks. This further motivates our choice (in the previous sections) of comparing the predictions of the transport models on idealized devices, limiting our scattering models to much more mature and established models of phonons, SR and II.

The new calibration helps improving the agreement between simulated and experimental I_{DS} curves, see Fig.16, especially above threshold at low V_{DS}, where the regime of transport is essentially the same as in the long channel device used to extract the low-field mobility of Fig.15. In the case of high V_{DS}, the spread between the different models and between models and experiments is larger, but still satisfactory. On the other hand, since all the simulators,

except the ETH-MC one, model the mobility reduction with respect to the universal curve as an enhanced coulomb scattering, the effect below threshold (where the effect of carrier screening is weak) is strong, and the agreement between experiments and simulations is worst in Fig.16 than in Fig.14. Furthermore, it should be mentioned that the charges introduced as a source of remote coulomb scattering were not treated in a self-consistent way, i.e. they were not included in the computation of device electrostatics. In fact this charge can be in the form of dipoles of have different sign in different position along the interface. Taking these charges into account in the electrostatics would cause a significant threshold voltage shift.

In summary, we observe that while the overall agreement between experimental data and simulations in Fig.16 is quite satisfactory, many open issues remain in the understanding and modeling of carrier transport in the presence of high-κ dielectrics.

6 Conclusions

The extensive comparison presented in this work has interested four DD simulators, six MC simulators, one NEGF solver and a model for the computation of the low-field mobility. The model predictions tend to converge for the longer channel devices (especially when considering the DD models), whereas the predictions of the scaling trends of on-current improvement are quantitatively quite different among the models. Comparison with ballistic NEGF results, points out that even with a limited number of scattering mechanisms accounted for (II, phonons, SR) scattering still plays a remarkable role in decenanometric devices. The impact of scattering on I_{DS} becomes even larger when specific mechanisms needed to reproduce the low-field mobility of advanced devices (e.g. remote charges in the high-κ) are included in the models.

Direct comparison with experiments is difficult because of many assumptions and uncertainties in the determination of many device parameters. Nevertheless most models compare quite well with the data. Unfortunately this result is achieved with quite different values of

physical quantities such as the charge in the high-κ, a situation that emphasizes the need for a better understanding of these materials.

Finally we emphasize that simulations of more mature technologies (e.g. 32nm compared to 22nm one) yields more similar predictions from the different simulators. Residual discrepancies may be impossible to eliminate because of the intrinsically different simplifications adopted by the models. Nevertheless these comparisons allow us to quantitatively assess the impact of model assumptions on the results, hence to increase the degree of confidence we expect from transport models.

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Figure captions

Figure 1. Structure of the 32nm FDSOI template transistor used in this work. Only one half of the symmetric structure is reported. All dimensions are in nm.

Figure 2. Simulated low-field mobility in bulk devices (infinite gate length) in the absence of II scattering, showing the calibration of the transport parameters.

Figure 3. Simulated low-field mobility of the 32nm FDSOI template. Being the device undoped, an inversion charge of $10^{13}cm^{-2}$ corresponds to an effective field of 760kV/cm.

Figure 4. Simulated low-field mobility of the 22nm DG template. The inversion charge includes both channels (front and back interface). This means that an inversion charge of $10^{13}cm^{-2}$ corresponds to an effective field of 380kV/cm.

Figure 5. Trans-characteristics of the 32nm FDSOI template for V_{DS}=0.1V.

Figure 6. Trans-characteristics of the 32nm FDSOI template for V_{DS}=1V.

Figure 7. Trans-characteristics of the 22nm DG template for V_{DS}=0.1V.

Figure 8. Trans-characteristics of the 22nm DG template for V_{DS}=1V.

Figure 9. Trans-characteristic of the 22nm DG template for V_{DS}=0.1V (plot a) and 1V (plot b). Results from MC simulations without ionized impurity scattering.

Table 1. Comparison between DD, MC and NEGF I_{DS} values (mA/μm) for V_{GS}=1V. The data are averages of the results reported in the previous figures.

Figure 10. Velocity profiles along the channel in the 22nm DG template biased at V_{GS}=V_{DS}=1V.

Figure 11. Inversion charge profiles along the channel in the 22nm DG template biased at V_{GS}=V_{DS}=1V.

Figure 12. Velocity profiles along the channel in the 32nm FDSOI template biased at V_{GS}=V_{DS}=1V.

Figure 13. Inversion charge profiles along the channel in the 32nm FDSOI template biased at V_{GS}=V_{DS}=1V.

Table 2. Position of the virtual source (x_{VS}, where $x = 0$ is the middle of the channel), average velocity (v_{VS}) and inversion charge N_{VS} at the virtual source. V_{GS}=V_{DS}=1V

Figure 14. Comparison between measured I/V data for a 32nm FDSOI device and the predictions of some of the simulation models of this work.

Figure 15. Comparison between experimental low-field mobility [60] (measured in a $10\mu m \times 10\mu m$ device) and simulations using the calibration of Section 3.4 (denoted as *std.param.*) or featuring an ad-hoc calibration (denoted as *adj.param.*). The ETH-MC model has not been

calibrated on the mobility data, but on the I/V curves of a 220nm device at low drain bias.

Figure 16. Comparison between measured I/V data for a 32nm FDSOI device and the predictions of some of the simulation models of this work, calibrated in order to reproduce the measured low-field mobility (*adj.param.* in Fig.15). (a): log-scale, (b): linear scale.

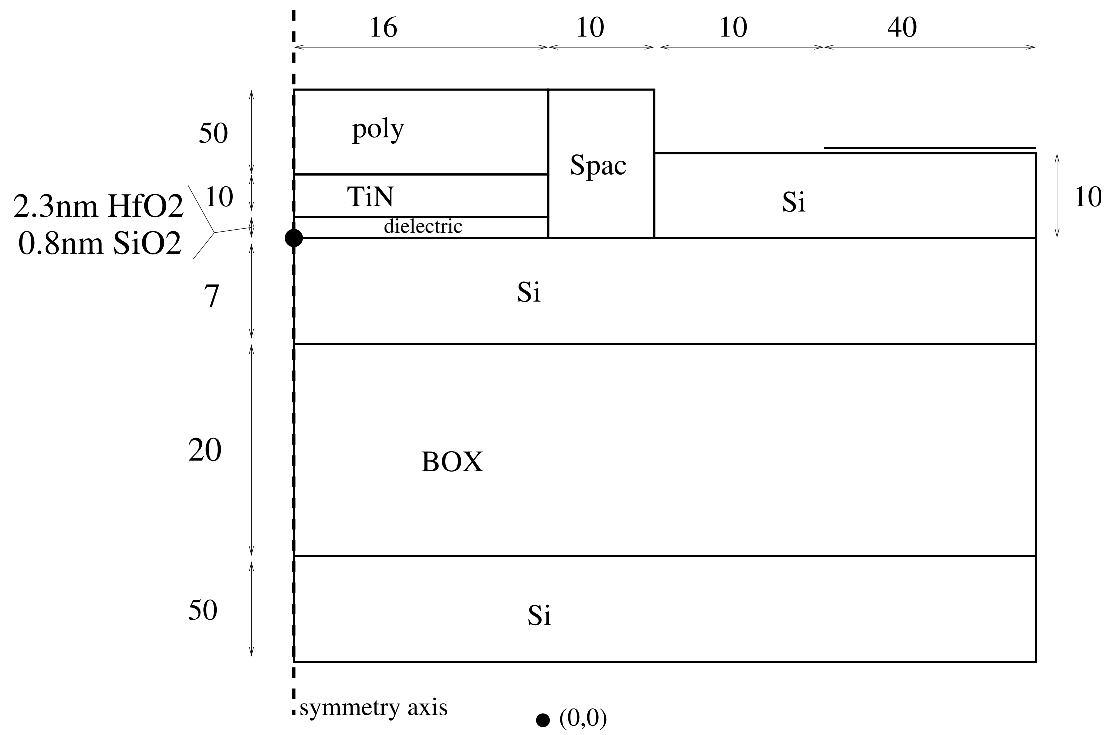


Figure 1
A Comparison of Advanced Transport Models for the Computation of the Drain Current in Nanoscale nMOSFETs

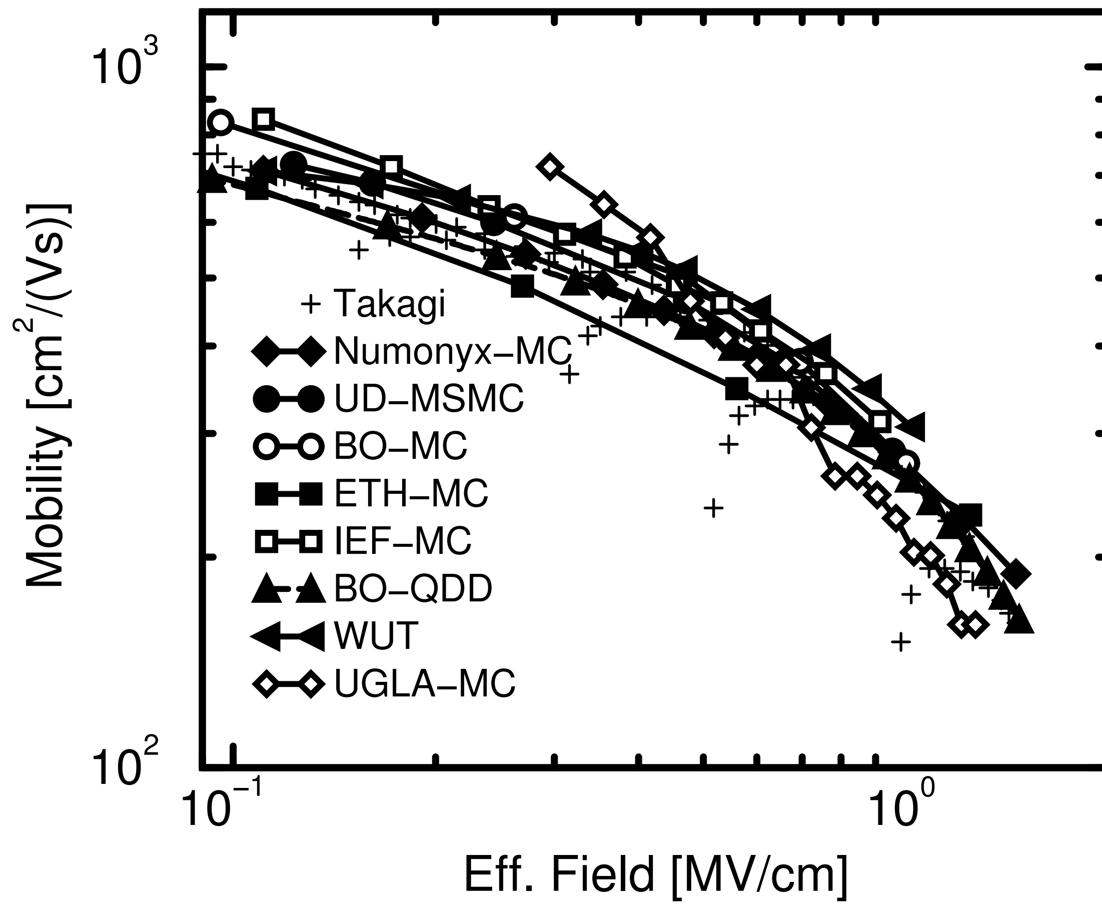


Figure 2

A Comparison of Advanced Transport Models for the Computation of the Drain Current in Nanoscale nMOSFETs

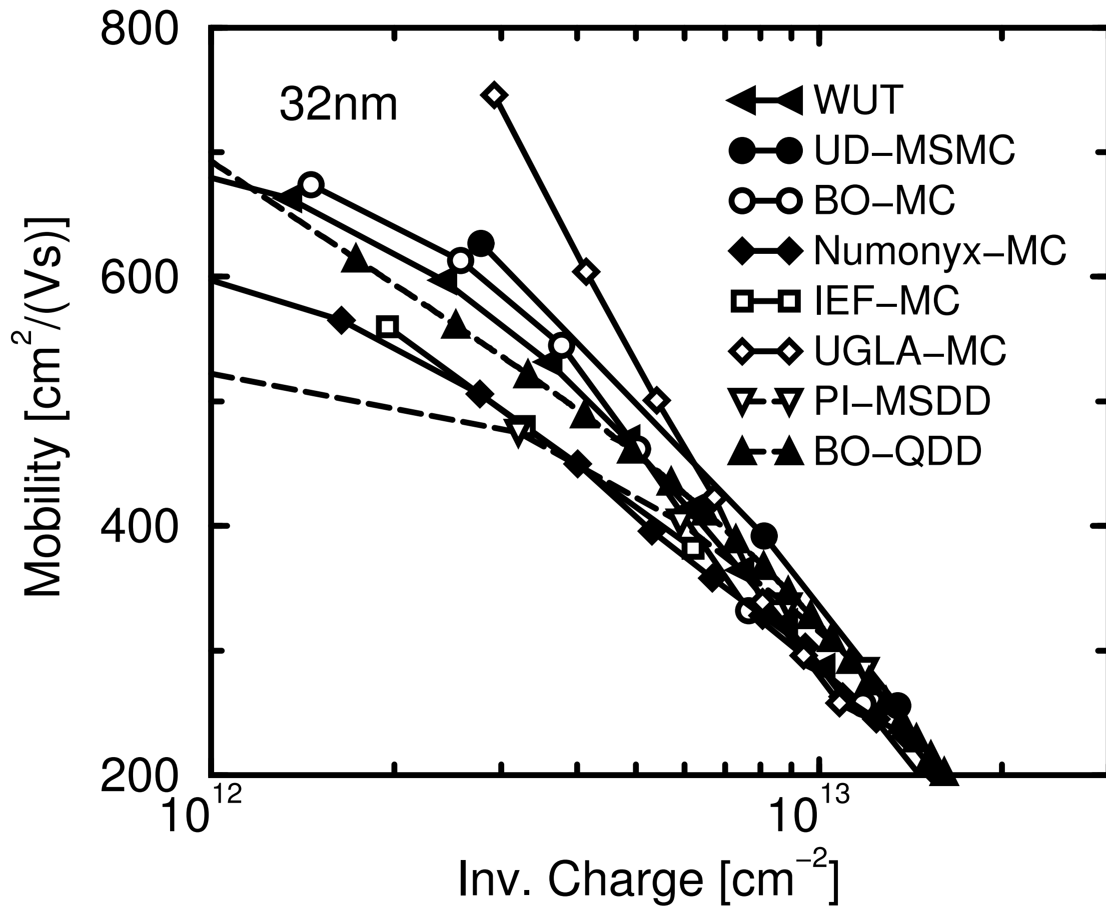


Figure 3

A Comparison of Advanced Transport Models for the Computation of the Drain Current in Nanoscale nMOSFETs

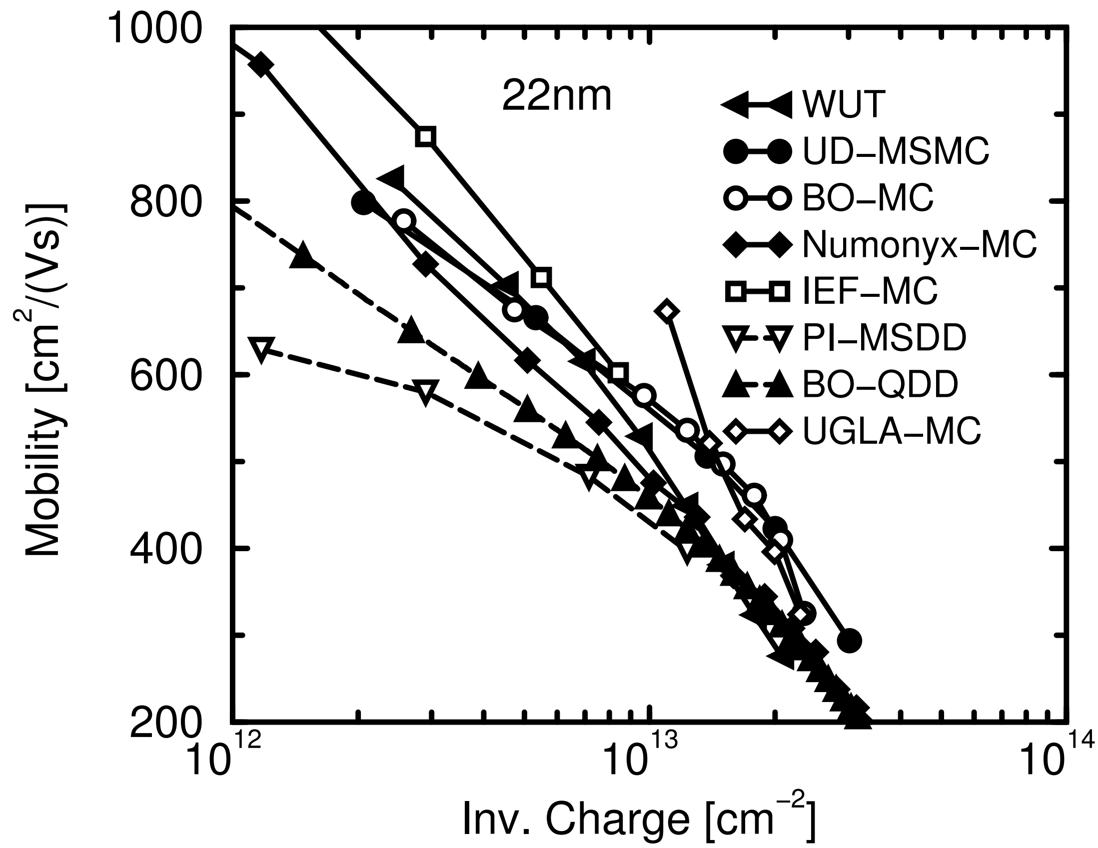


Figure 4

A Comparison of Advanced Transport Models for the Computation of the Drain Current in Nanoscale nMOSFETs

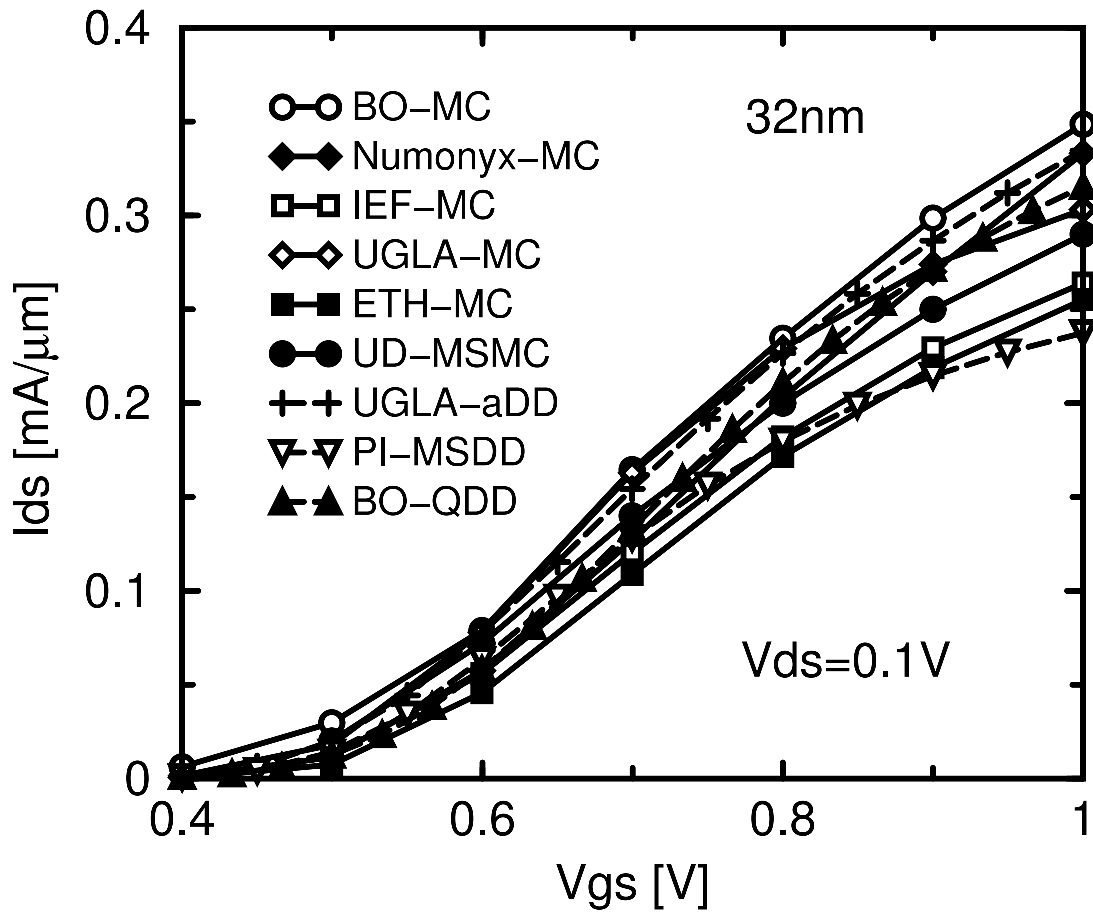


Figure 5

A Comparison of Advanced Transport Models for the Computation of the Drain Current in Nanoscale nMOSFETs

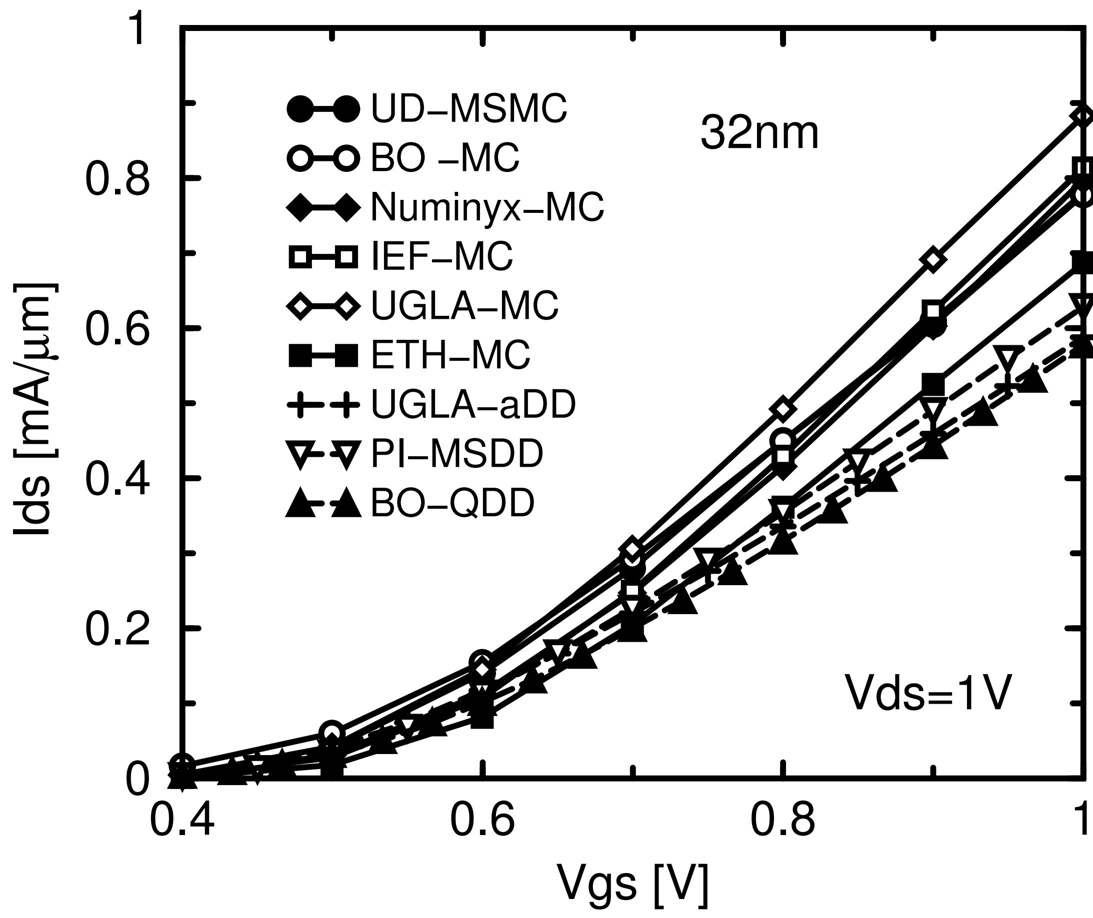


Figure 6

A Comparison of Advanced Transport Models for the Computation of the Drain Current in Nanoscale nMOSFETs

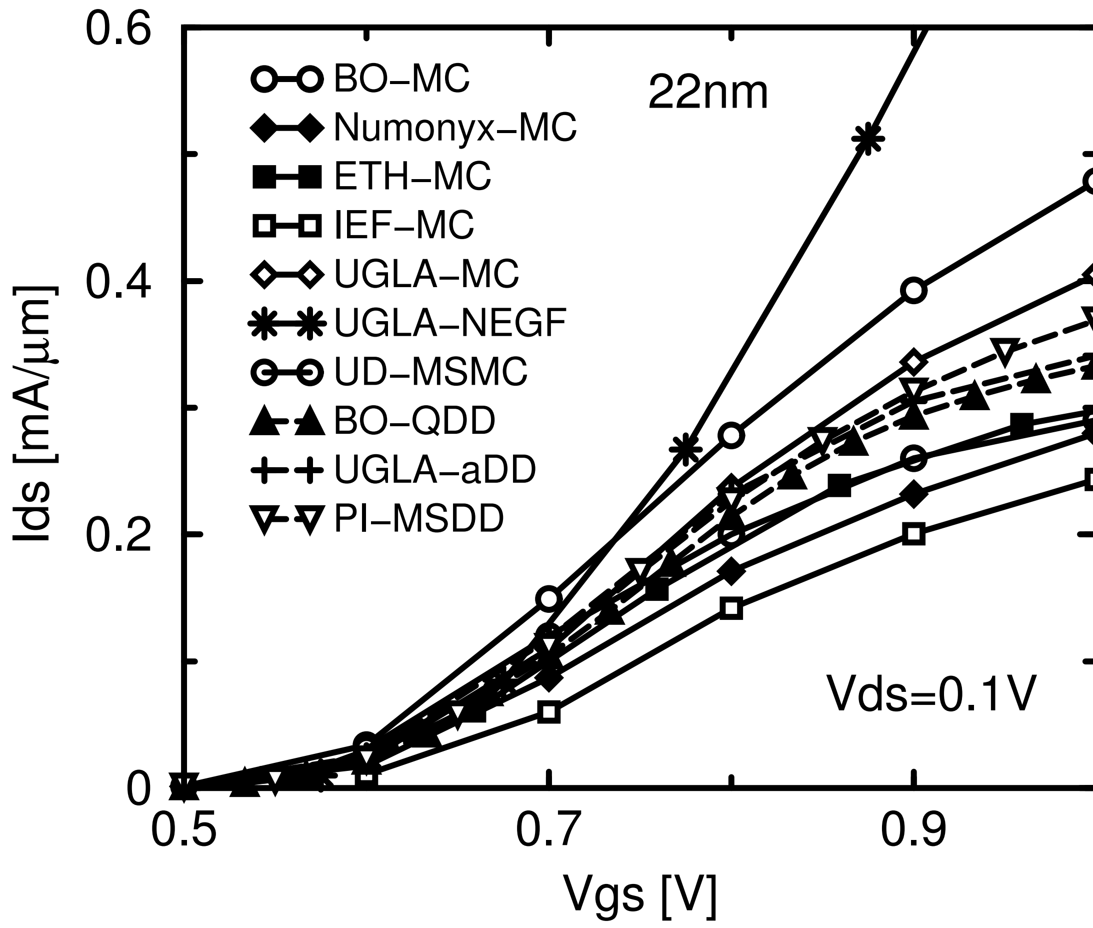


Figure 7
A Comparison of Advanced Transport Models for the Computation of the Drain Current in Nanoscale nMOSFETs

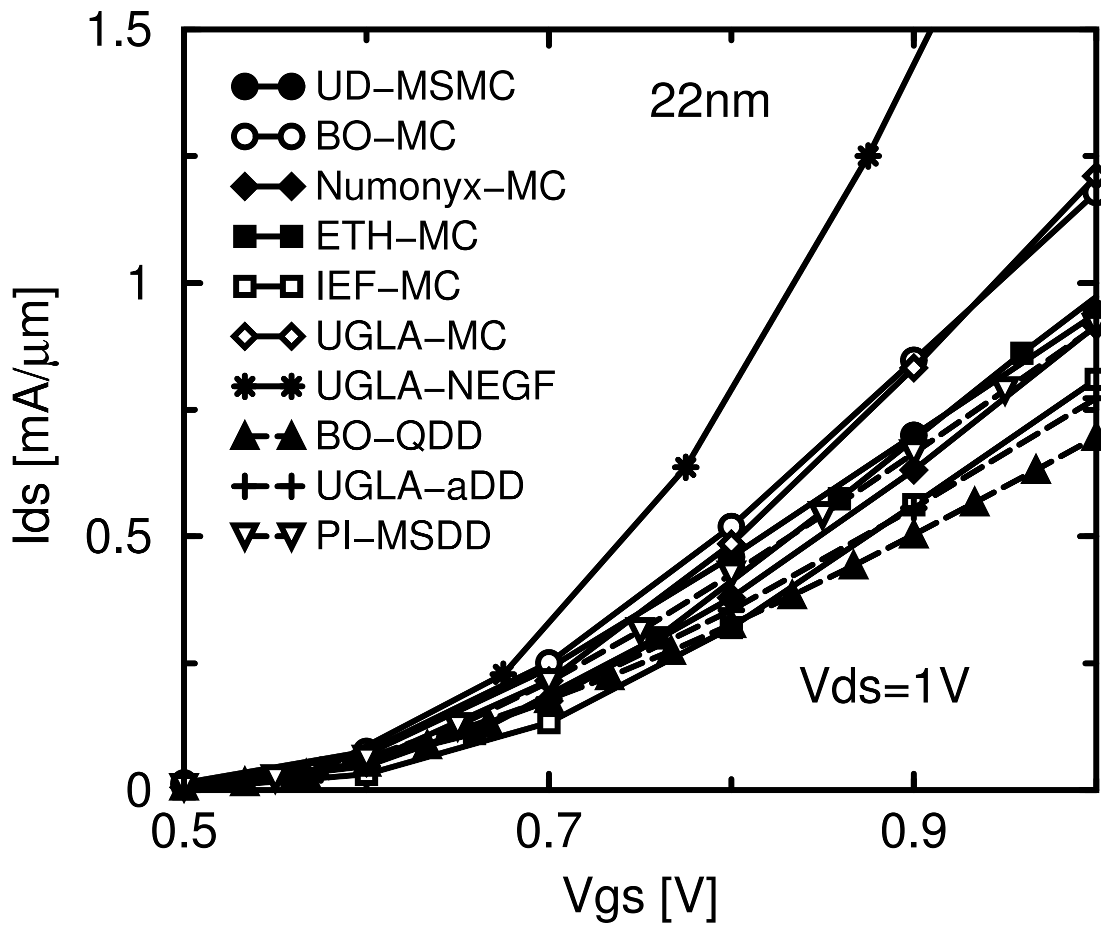
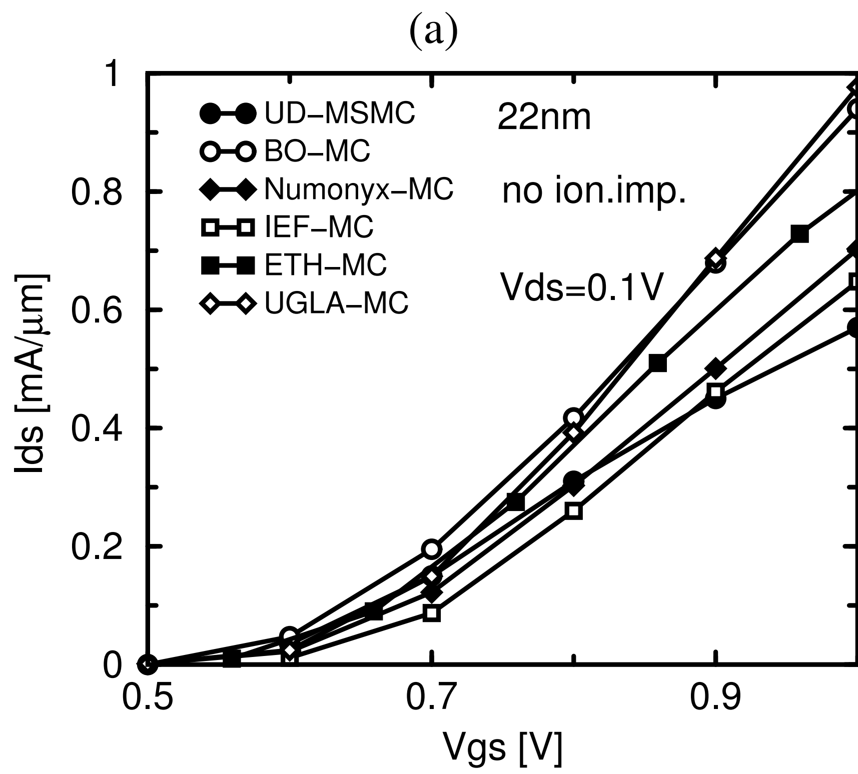


Figure 8

A Comparison of Advanced Transport Models for the Computation of the Drain Current in Nanoscale nMOSFETs



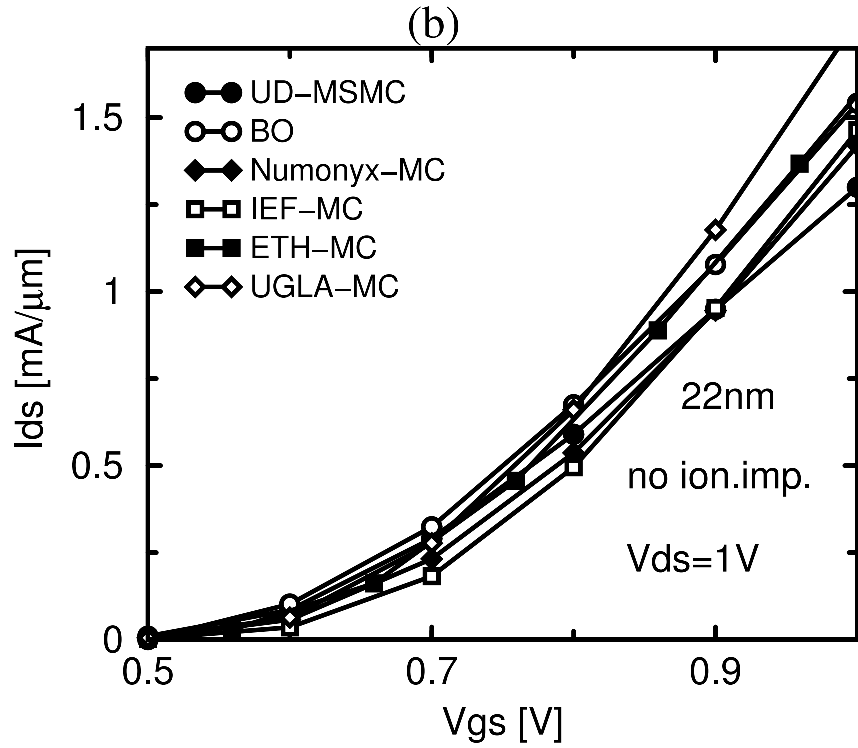


Figure 9

A Comparison of Advanced Transport Models for the Computation of the Drain Current in

Dev.	V_{DS}	DD	MC (II)	MC (no-II)	NEGF
22nm	0.1	0.3	0.3	0.6	0.85
22nm	1.0	0.7	1.0	1.3	2.3
32nm	0.1	0.3	0.3	0.45	n.a.
32nm	1.0	0.55	0.8	0.9	n.a.

Table 1

A Comparison of Advanced Transport Models for the Computation of the Drain Current in Nanoscale nMOSFETs

	x_{VS} nm	v_{VS} $10^7 cm/s$	N_{VS} $10^{13} cm^{-2}$	x_{VS} nm	v_{VS} $10^7 cm/s$	N_{VS} $10^{13} cm^{-2}$
device	32nm	32nm	32nm	22nm	22nm	22nm
UD-MSMC	-15.5	0.70	0.66	-9.9	0.82	0.75
ETH-MC	-16.8	0.41	1.06	-11.2	0.47	1.24
BO-MC	-16.8	0.50	1.0	-10.3	0.75	1.0
BO-QDD	-14.7	0.47	0.76	-8.5	0.7	0.6

Table 2

A Comparison of Advanced Transport Models for the Computation of the Drain Current in Nanoscale nMOSFETs

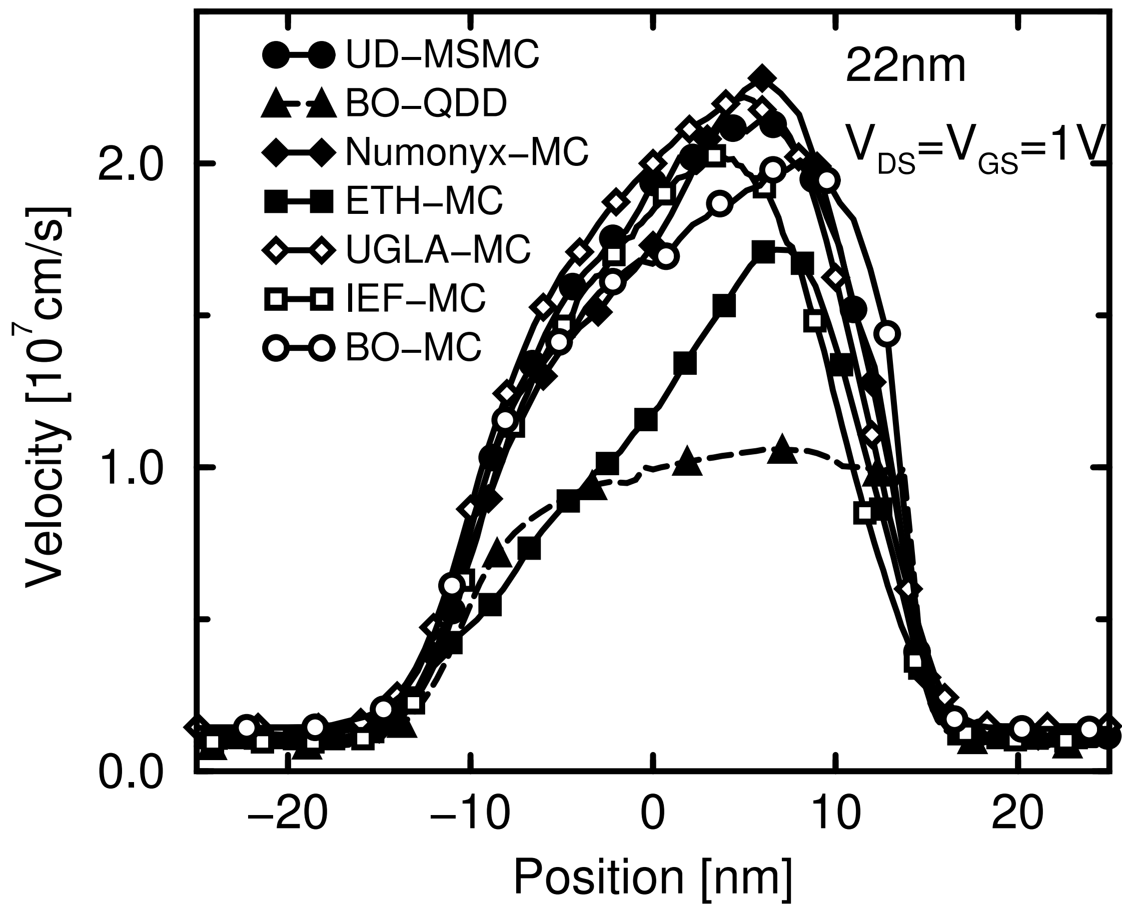


Figure 10

A Comparison of Advanced Transport Models for the Computation of the Drain Current in Nanoscale nMOSFETs

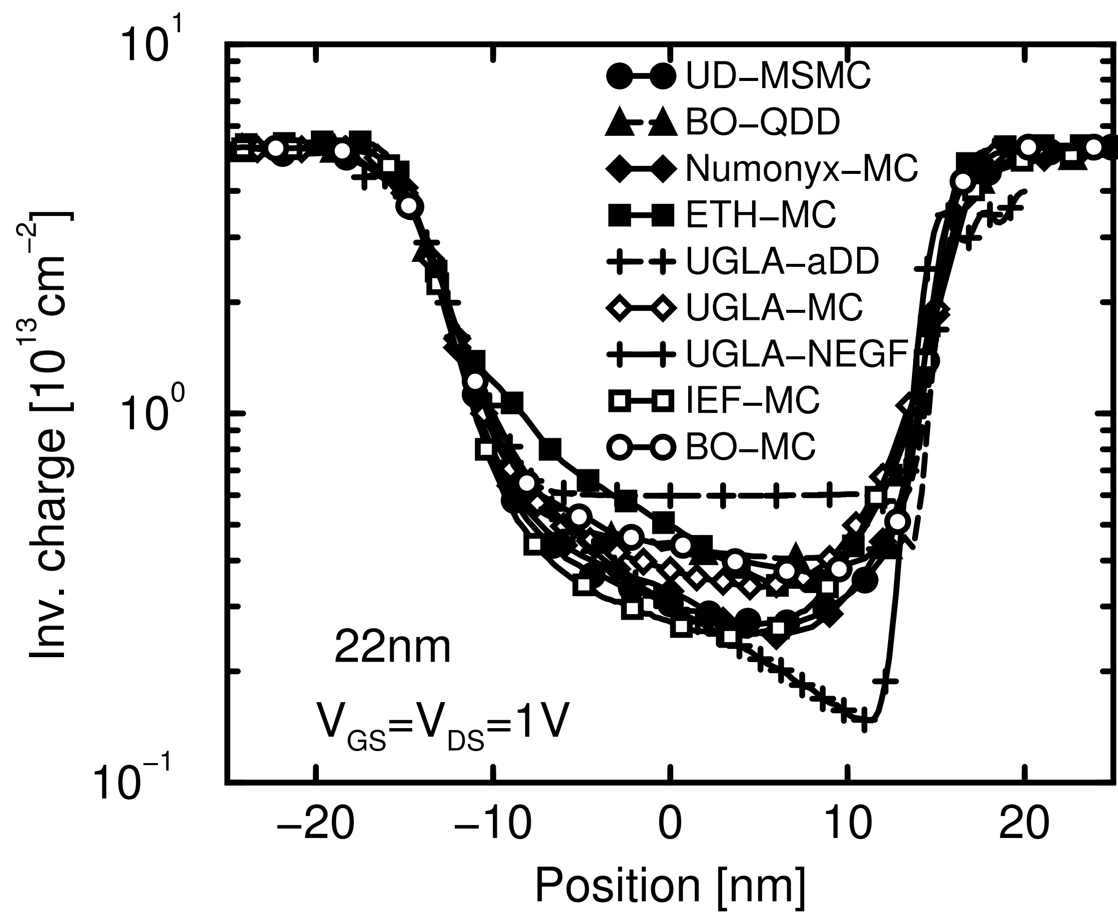


Figure 11

A Comparison of Advanced Transport Models for the Computation of the Drain Current in Nanoscale nMOSFETs

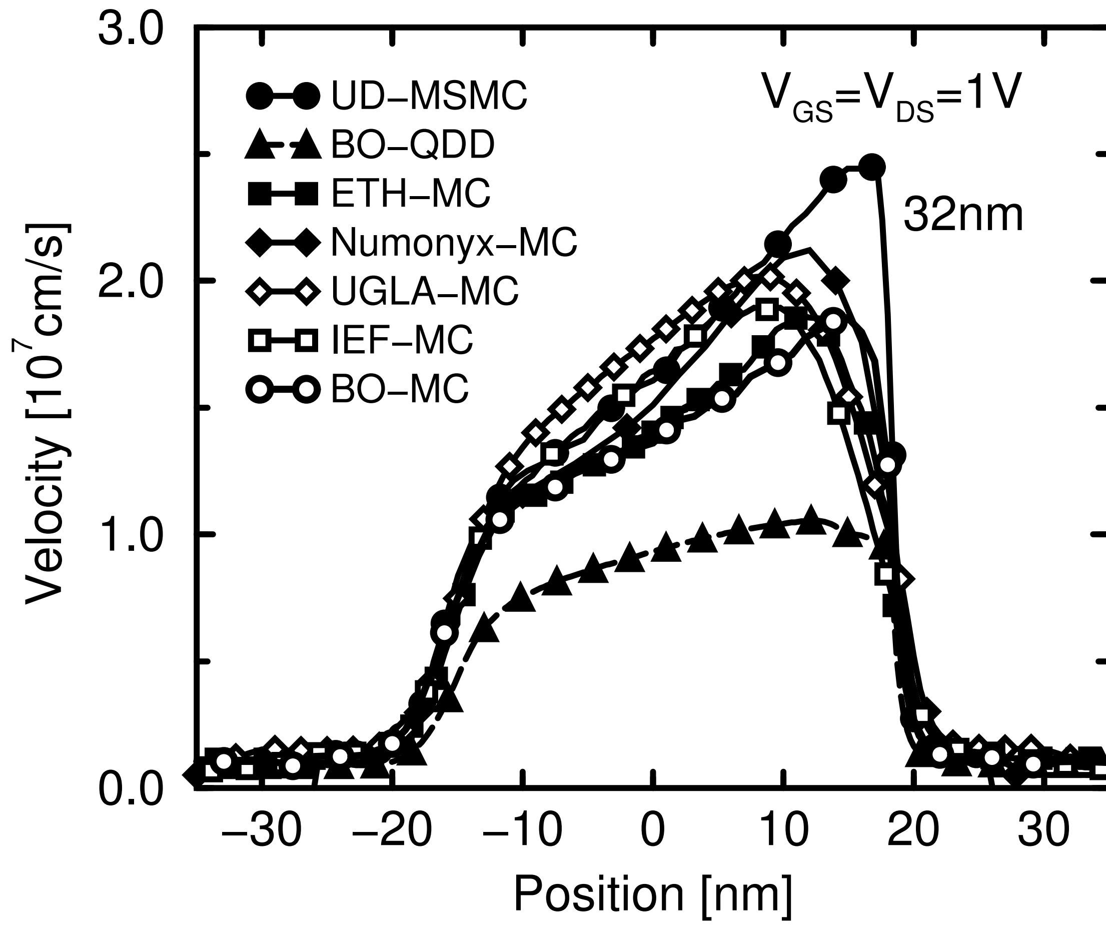


Figure 12

A Comparison of Advanced Transport Models for the Computation of the Drain Current in Nanoscale nMOSFETs

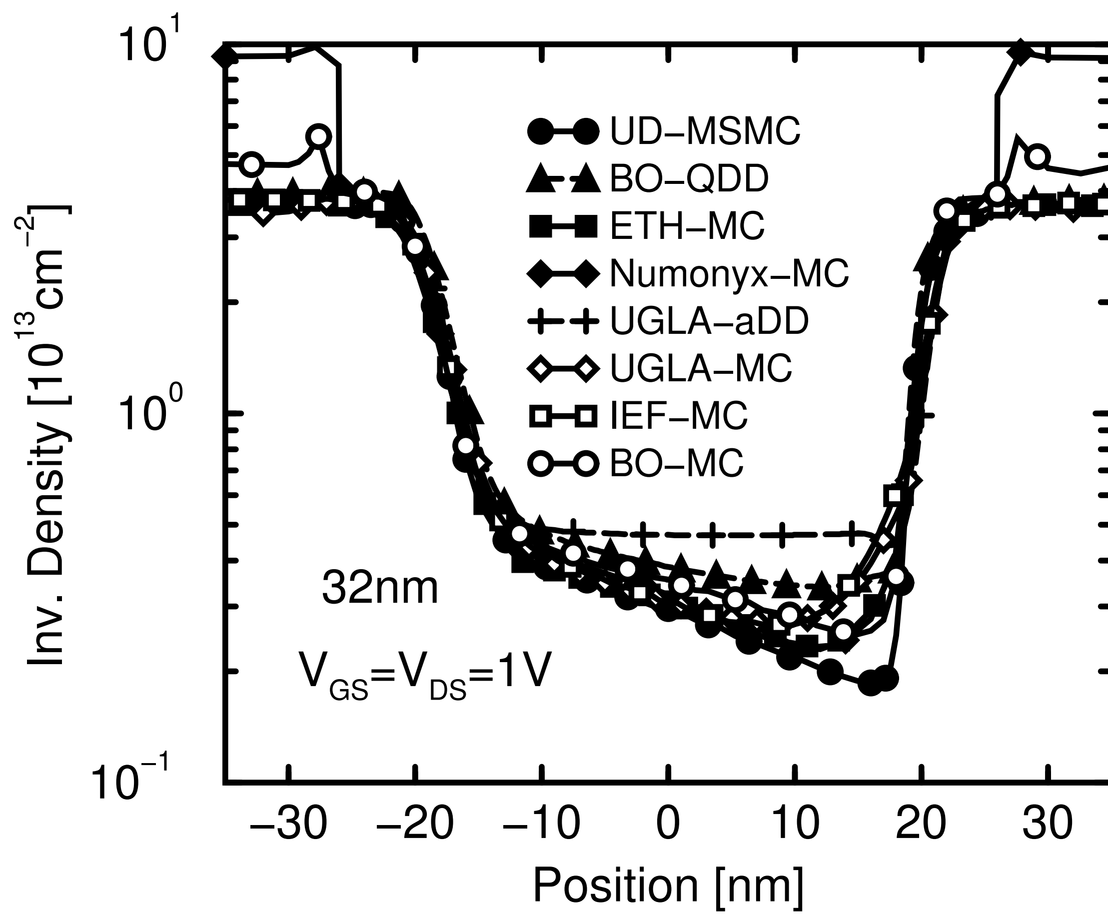


Figure 13

A Comparison of Advanced Transport Models for the Computation of the Drain Current in Nanoscale nMOSFETs

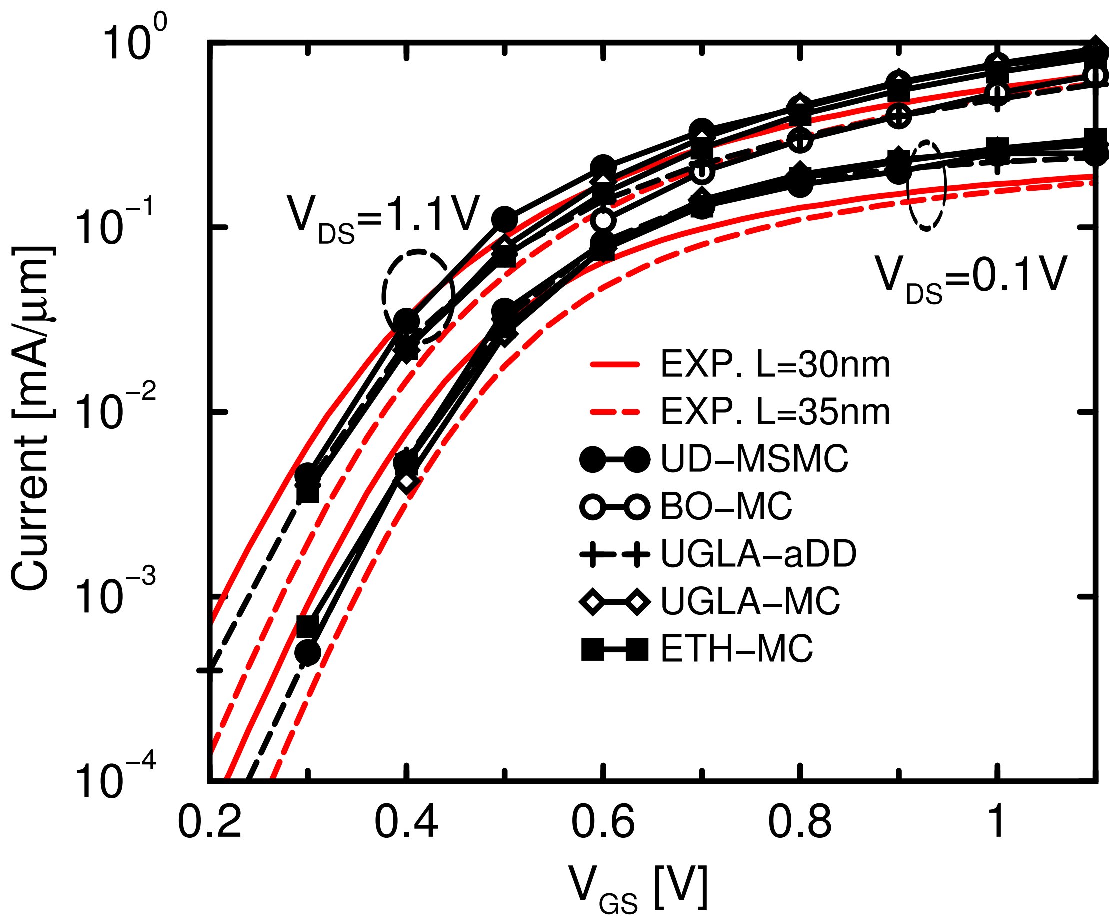


Figure 14

A Comparison of Advanced Transport Models for the Computation of the Drain Current in Nanoscale nMOSFETs

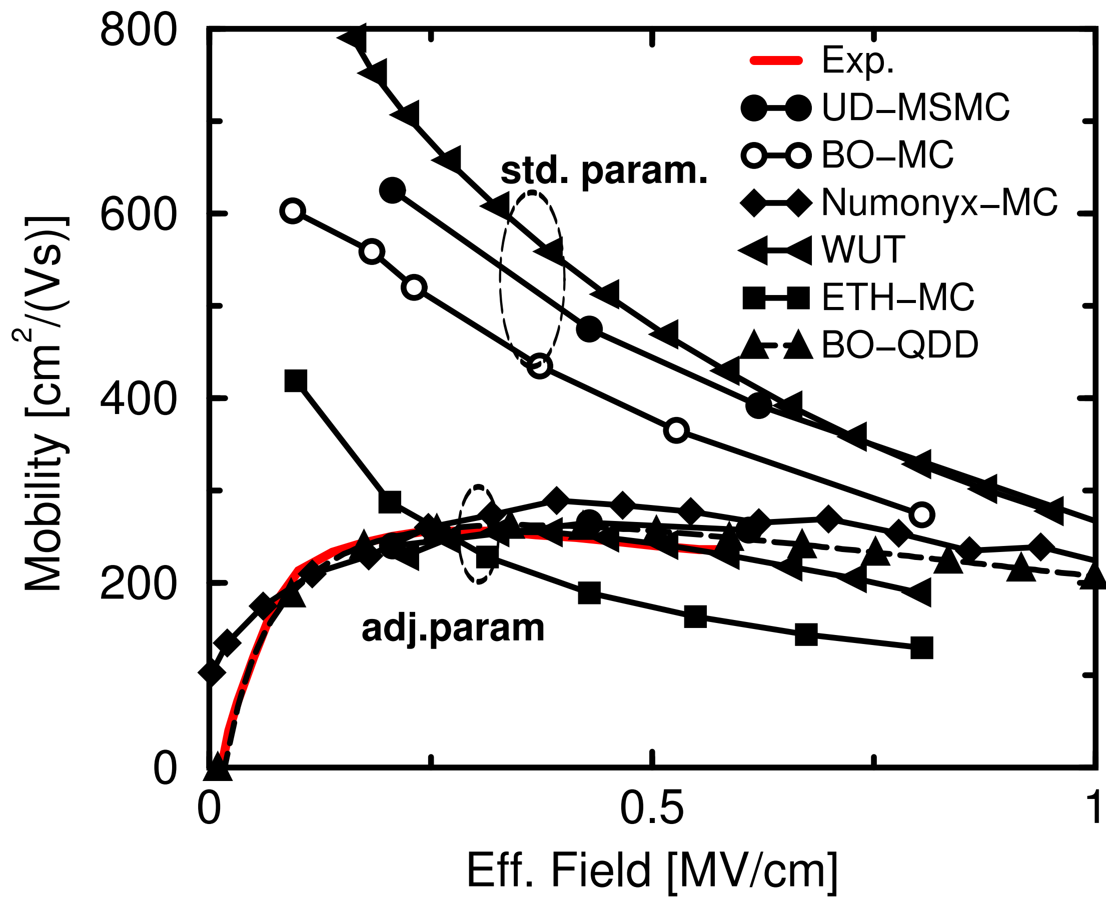
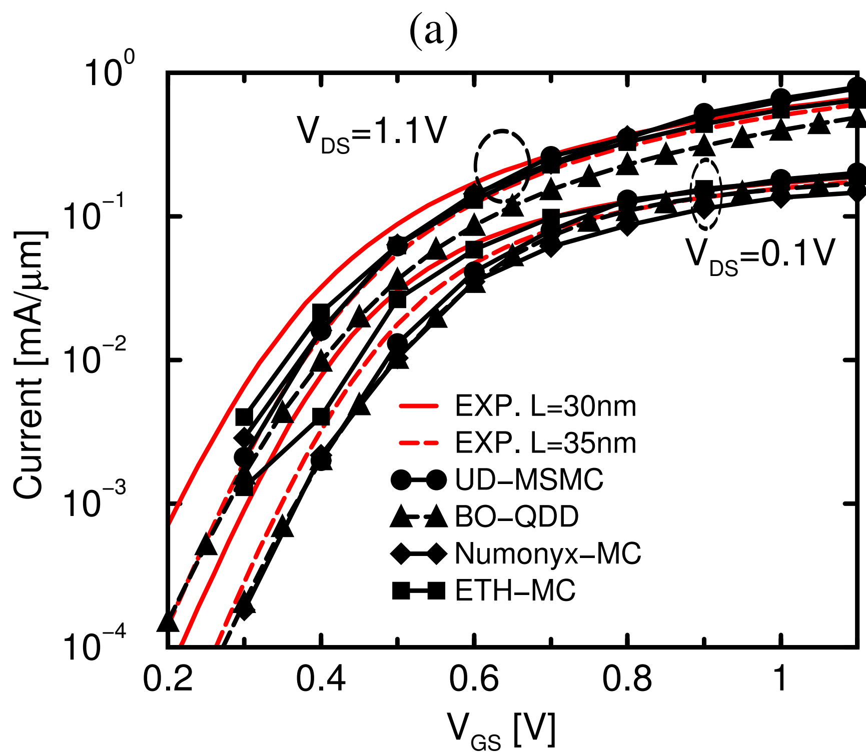


Figure 15

A Comparison of Advanced Transport Models for the Computation of the Drain Current in Nanoscale nMOSFETs



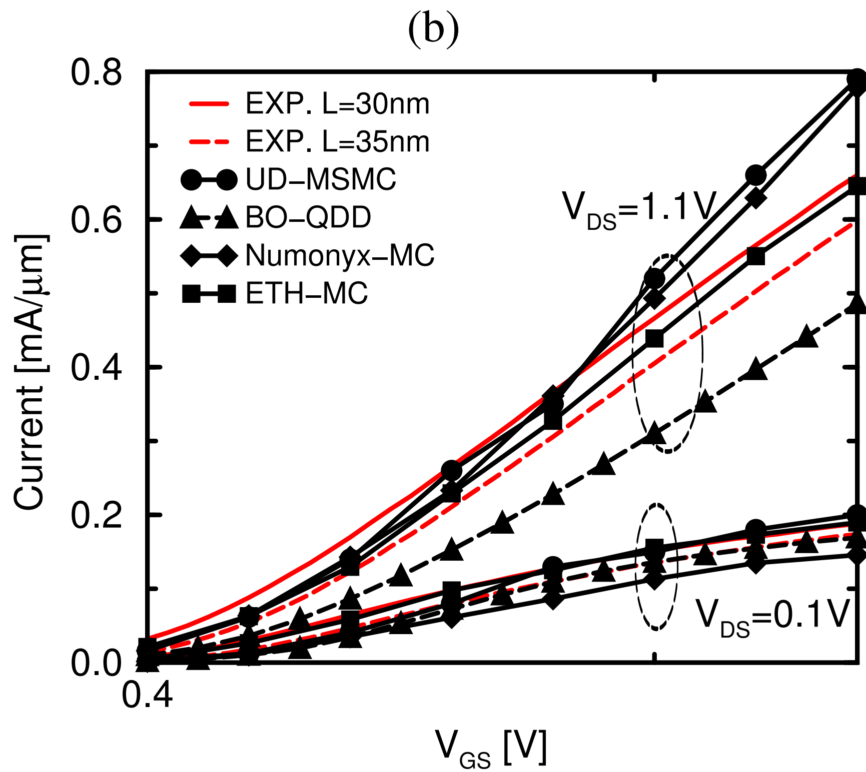


Figure 16

A Comparison of Advanced Transport Models for the Computation of the Drain Current in