Impact of Non-idealities on the Performance of InAs/(In)GaAsSb/GaSb Tunnel FETs

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ABSTRACT. Measured InGaAsSb/InAs nanowire TFETs showing both, sub-60mV/dec slope and high ON-current, are simulated using calibrated TCAD. The focus is laid on the impact of non-idealities, such as hetero-interface traps, oxide-interface traps, and bulk traps on device characteristics. Simulated temperature-dependent transfer curves are in good agreement with the measured data which validates the simulation set-up. It is found that trap-assisted tunneling involving bulk traps adjacent to the hetero-junction is primarily responsible for the degradation of the swing. Due to the small diameter of the nanowire, trap-assisted tunneling is inhibited at the InAs/oxide interface. Still, oxide interface traps reduce the electrostatic coupling between gate and channel, which further increases the swing. The TCAD analysis correctly predicts the negative transconductance observed at high gate bias. If the same simulation set-up is used to study the effect of gate alignment, a significant improvement of both ON-current and swing is found.
KEYWORDS. III-V semiconductors, Tunnel FETs, trap-assisted tunneling, negative transconductance.

1. Introduction

The Tunnel Field Effect Transistor (TFET) is considered as a solid-state electronic switch alternative to the MOSFET to achieve further scaling of the supply voltage [1,2]. TFETs which operate on the principle of field modulation of band-to-band tunneling (BTBT) can, in principle, deliver a subthreshold swing (SS) less than 60 mV/dec as predicted by full-band quantum transport simulations [3]. The ON-current is strongly affected by the band gap and the effective masses of the semiconductor. Due to the small effective masses and the direct band gap, III-V materials are well suited for TFET application. The introduction of a hetero-junction can further improve the ON-current by reducing the effective tunnel gap. Thus, III-V hetero-junction TFETs can deliver both high ON-current and low SS. Experimental data of InAs/InGaAsSb nanowire TFETs presented in [4,5] confirm these theoretical considerations.

The SS of a TFET is degraded by various non-idealities such as hetero-interface or oxide interface traps, bulk traps, band tails, and others, which are inevitably present in the hetero-junction devices. Among them, traps have the strongest effect on the SS as e.g. observed in the TCAD analysis of InAs/Si hetero-junction TFETs [6-8]. In this work, the experimental data of InAs/InGaAsSb hetero-junction TFETs [5] are analyzed using TCAD to understand whether the above-mentioned non-idealities degrade the SS of all-III-V TFETs, which non-idealities have the strongest impact, and what is the best performance predicted for the given TFETs.

TCAD modeling of TFETs commonly involves the fitting of various parameters of the BTBT model to measured I_D-V_{GS} curves. Due to the possibility that multiple parameter sets can yield the same good fit, TCAD results based on fitted parameters cannot always be generalized, and the predictability remains limited. Therefore, we tried to minimize the number of fitting parameters in order to make the present TCAD study more reliable. The nonlocal BTBT model depends on band gap, band alignments, and effective masses. All these parameters are set to their experimental values taking into account the position dependence of material composition, uniaxial stress, and crystal structure. This information is extracted

from transmission electron microscopy (TEM) and other physical characterizations. Also, we have used measured interface trap densities wherever available.

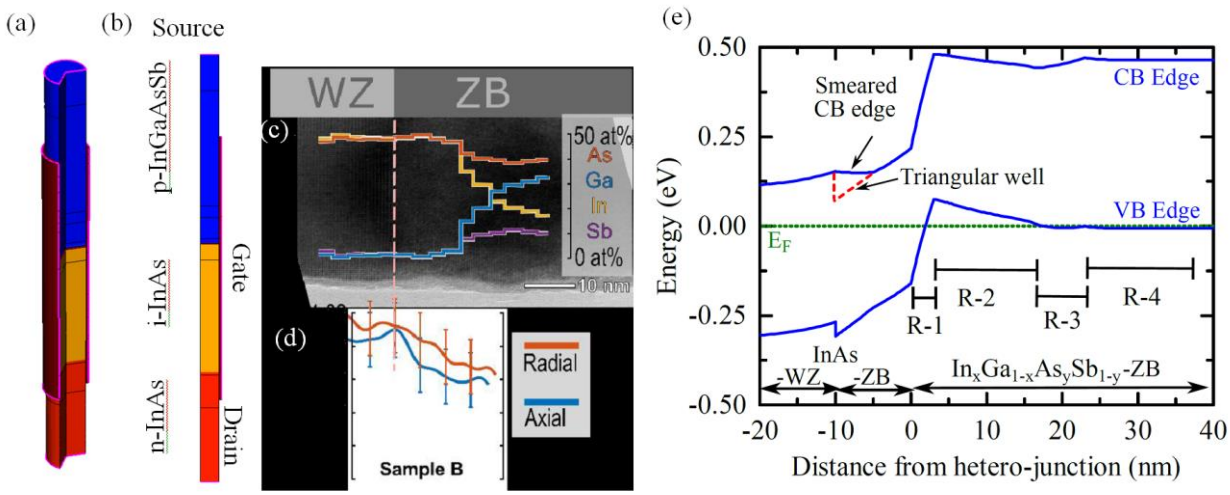

Figure 1. *(a) Schematic of the simulated nanowire TFET, (b) radial cross section, (c) TEM image of the hetero-interface and material composition, (d) strain profiles, (e) band edge diagram along the axis of the nanowire at V_{DS} = V_{GS} = 0 V. A triangular-like quantum well is present at the InAs-ZB/InAs-WZ interface. Its effect on the band structure is mimicked by gradually changing the band gap of the material.*

This paper is organized as follows. Section II describes how the material-composition-dependent band structure parameters are used and various non-idealities are modeled to capture the physics in the device as exactly as possible. The simulation results, including the temperature dependence of the transfer characteristics are presented in Section III. This section also outlines the deconvoluted effects of various non-idealities as well as the physical origin of the measured negative transconductance. The section ends with a brief discussion on possible changes of the device geometry for an improved performance. Conclusions of the TCAD analysis are given in Section IV.

2. Simulation Set-up

The vertical nanowire TFET consists of an intrinsically doped InAs channel, p+ doped InGaAsSb source and n+ doped InAs drain. The radial cross section of the nanowire is shown in Fig. 1(b). Using cylindrical coordinates enables to simulate a radially symmetric 3-dimensional device in 2D. This is done initially to speed-up the simulations, but true 3D simulations will be performed later to assess the impact of single traps and their location. The gate oxide is an Al_2O_3/HfO_2 bilayer with an effective oxide thickness (EOT) of 1.4 nm. The InAs/InGaAsSb/GaSb nanowire with a diameter of 40 nm was grown on the substrate using Metal Oxide Vapor Phase Epitaxy from Au seed particles which were patterned on a Si (111) substrate by electron beam lithography. The InAs/InGaAsSb segment was later trimmed to a diameter of 20 nm before introducing high-k dielectric. A detailed description of the device fabrication can be found in Ref. [5]. TEM analysis was performed on the nanowire to obtain information on the variation of material composition as well as its crystal structure along the nanowire axis [5]. The analysis reveals that the channel consists of a wurtzite (WZ) segment of InAs followed by a 10 nm zincblende (ZB) segment which is followed by the quaternary alloy InGaAsSb. The InGaAsSb segment, which forms the source, is *in-situ* doped with $N_A = 1\times10^{19}\,cm^{-3}$. The InAs segment in the drain is *in-situ* doped with $N_D = 1\times10^{19}\,cm^{-3}$. The gate overlaps with the 60 nm long InGaAsSb segment making it a gate-overlapped-source (GOS) TFET. The TEM image of the hetero-interface is shown in Fig. 1(c) along with the plot of

the composition of InGaAsSb. The variation of the uni-axial strain along the nanowire axis can be inferred from Fig. 1(d).

2.1. *Band structure modeling*

Adjacent to the hetero-interface, the composition of InGaAsSb changes rapidly along the axis which results in a variation of the band gap as well as the electron and hole effective masses. Since BTBT is strongly affected by the band gap and the effective masses, it is necessary to consider the variation of the material composition in the simulation. The InGaAsSb segment of the nanowire is divided into four regions, R-1, …, R-4. In region R-1, the alloy composition varies from InAs (to the left) to $In_{0.7}Ga_{0.3}As_{0.84}Sb_{0.16}$ (to the right), denoted as $In_{1\rightarrow0.7}Ga_{0\rightarrow0.3}As_{1\rightarrow0.84}Sb_{0\rightarrow0.16}$. Region R-2 consists of $In_{0.7\rightarrow0.44}Ga_{0.3\rightarrow0.56}As_{0.84\rightarrow0.72}Sb_{0.16\rightarrow0.28}$. Region R-3 is composed of $In_{0.44\rightarrow0.32}Ga_{0.56\rightarrow0.68}As_{0.72}Sb_{0.28}$ while R-4 consists of $In_{0.32}Ga_{0.68}As_{0.72}Sb_{0.28}$. In each segment, the band gap and the effective masses were set to the experimental values taken from Ref. [9]. To obtain the values for intermediate compositions, an interpolation formula suggested by Adachi [10] was used. The material composition was assumed to vary linearly within each region. This doesn't necessarily imply a linear variation of band gap and effective masses, since bowing of these quantities for intermediate compositions was taken into account in the calculations. The energetic position of the conduction band (CB) edge is set to the electron affinity of the semiconductor/alloy taken from Ref. [19]. Thus, the band alignment at all the semiconductor interfaces follows Anderson's rule. The abrupt change in the crystal structure of InAs from WZ to ZB during the growth is taken into account by using the band structure parameters of the respective allotropes. In addition to the composition variation, uniaxial compressive strain is present at the hetero-interface. The position-dependent uniaxial stress along the axis was extracted from the high-resolution TEM images [5] and plotted in Fig. 1(d). The effect of strain on band gap and band alignments has been modeled with the model-solid theoretical approach by Van de Walle [11]. The temperature dependence of the band gap was modeled using Varshni's law [22]. The parameters α and β of Varshney's model were taken from literature [9] and interpolated using Adachi's interpolation formula for quaternary alloys. In this way, any explicit fitting of band structure quantities and band offsets has been avoided. The band diagram at zero bias extracted along the nanowire axis of the TFET is plotted in Fig. 1(e). Band-structure quantities used at the beginning/end of each of the above segments are listed in Table I.

InGaAsSb Composition	Strain	E_g (including strain effect)	m_C	m_V
InAs(WZ)	0%	0.42	0.042	0.084
InAs(ZB)	-2%	0.376	0.026	0.026
$In_{0.7}Ga_{0.3}As_{0.84}Sb_{0.16}$	-1%	0.405	0.036	0.038
$In_{0.44}Ga_{0.56}As_{0.72}Sb_{0.28}$	0%	0.432	0.043	0.048
$In_{0.32}Ga_{0.68}As_{0.72}Sb_{0.28}$	0%	0.47	0.048	0.077

Table 1. *Composition-dependent band structure parameters at the end of each segment in the nanowire.*

In addition to the above variations, quantum confinement may also alter the device characteristics. The inability to account for quantum-confinement effects is a drawback of semi-classical simulations. An abrupt change in the crystal structure from InAs-WZ to ZB results in a band offset at the interface which gives rise to a triangular-like potential well. Our calculations suggest that the quantization of the CB states in the well results in the formation of only one bound state close to the top of the finite barrier. This effectively smears out the otherwise steep well at the interface. Simulations confirmed that, ignoring this

effect causes a strong discrepancy between simulated and measured *IV*-characteristics. Therefore, quantization has been modeled by introducing a pseudo-grading of the CB edge at the interface thus making it continuous. The small effects related to quantum confinement normal to the transport direction were ignored in the simulations.

2.2. *Trap distribution and modeling of trap-assisted tunneling*

The analysis of the TEM images reveals that the composition of InGaAsSb changes sharply in region R-1 which may induce defect states in this region. The degradation of the TFET performance due to trap-assisted tunneling (TAT) at the hetero-interface was simulated using the nonlocal TAT model of Ref. [12]. In the TCAD implementation of this model, the tunnel rate between trap and band states is computed using the WKB approximation and integrating over the imaginary dispersion. Both the direct and phonon-assisted nonlocal TAT models were activated on a non-local mesh constructed at the hetero-interface. Since the exact location of the traps in the segment R-1 is unknown, a constant density of bulk traps (D_{bt}) in this region was initially assumed. Choosing $D_{bt} = 1.6 \times 10^{18}\,\mathrm{cm}^{-3}$ gives, on spatial integration, approximately *one* trap in region R-1. The variation of the defect energy level in the band gap leads to best agreement with the experimental *IV*-data when it resides 0.1 eV above the valence band (VB) edge. A simulation parameter called *trap interaction volume*, which reflects the coupling strength of the tunneling process and acts as a scaling factor of the nonlocal TAT generation rate, was set to $50\,\text{Å}^3$ to match the simulated current level to the experimental one. This parameter is related to the volume of the localized wave function.

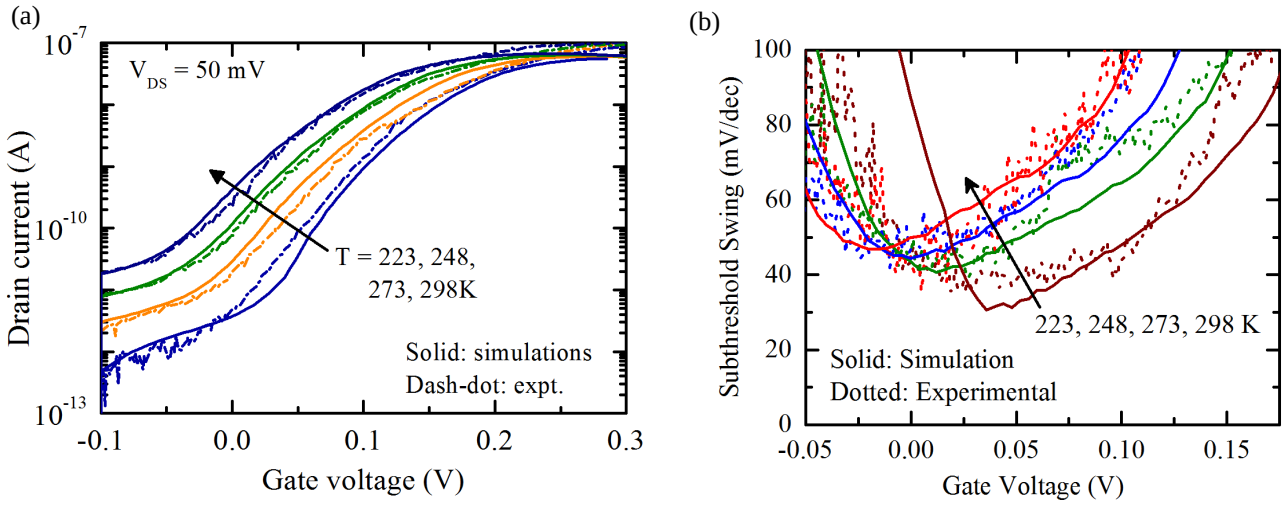

Figure 2. *(a) Comparison of simulated temperature-dependent transfer characteristics of the TFET with the experimental data. (b) Comparison of SS calculated from the simulated and the experimental transfer characteristics. A reduction of the minimum swing with decreasing temperature is visible.*

In addition to traps near the hetero-junction, traps at the InAs/oxide interface may degrade the TFET performance. Donor-like traps were introduced at this interface. Their energetic distribution was extracted from CV measurements of InAs nanowires [13] and adapted here. Traps may also exist in the band gap at the InGaAsSb/oxide interface. Since the Fermi level in InGaAsSb is located below the VB edge, these interface traps are empty and hence electrostatically inactive.

The gate work function (WF) was obtained by horizontally shifting the simulated I_D-V_{GS} plots for the best match with the experimental data. The WF was found to vary linearly from 4.86 eV to 4.92 eV as the temperature decreases from 298 K to 223 K. This variation could be due to the freezing of charges at

certain oxide traps causing a shift of the WF. A similar WF shift with temperature in InAs nanowire MOSFETs had been observed earlier [24].

The nanowire TFET was simulated with the commercial TCAD simulator Sentaurus-Device [14] using the above-described simulation set-up.

3. Simulation Results and Discussion

3.1. *Temperature dependence*

A comparison of simulated and measured temperature-dependent transfer characteristics of the TFET is shown in Fig. 2(a). The good agreement confirms the validity of the simulation set-up. Note that only the density of traps in region R-1 was fitted to the *IV*-curves. The remaining simulation parameters were taken from published experimental data. The good agreement also validates the above approach to obtain band gap, band alignment and effective masses by interpolating their experimental values to the extracted position-dependent material compositions.

The simulated ON-current is about 30% smaller than the measured one. This difference could be due to an inevitable error introduced in determining the composition of InGaAsSb from the TEM image. Small changes in the process parameters/material composition could lead to significant variations in the on-current as observed from statistical analysis of a number of TFET samples presented in [23].

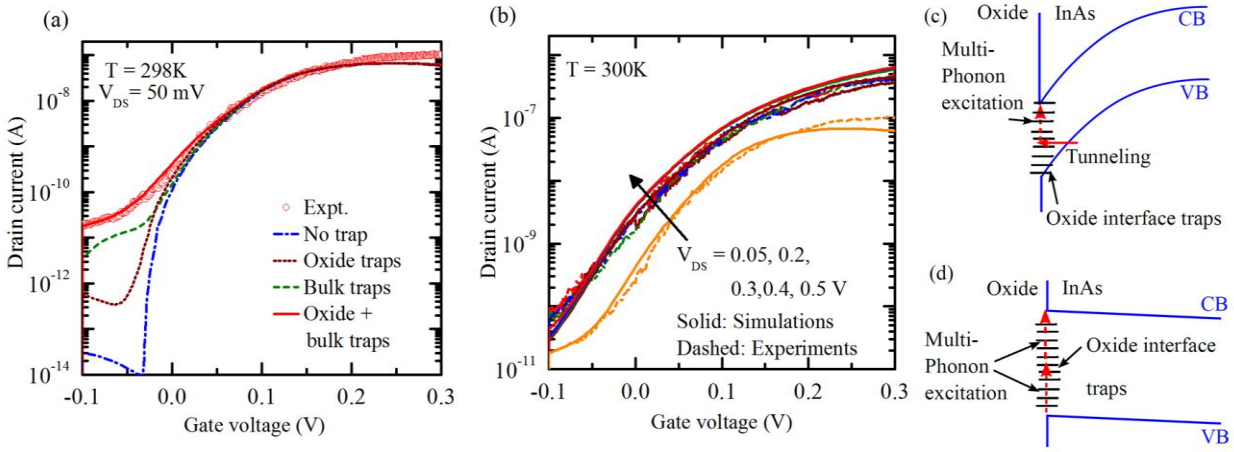

Figure 3. *(a) Transfer characteristics of the TFET taking into account oxide and bulk traps separately. (b) Threshold voltage shift as observed in experiment with increasing V_{DS} is reproduced in the simulation. (c) Schematic diagram of trap-assisted tunneling and (d) multi-phonon excitation processes at the oxide/InAs interface.*

The temperature-dependent SS was obtained from the transfer characteristics and plotted in Fig. 2(b). Within an interval of about 100 mV, the SS lies below the thermal limit of 60 mV/dec. The minimum point slope exhibits a weak temperature dependence only. It stems from the temperature dependence of the band gap in the rate of direct BTBT in III-V materials. This can be inferred from the WKB probability $\exp(-\frac{\sqrt{2m_{red}E_g^3}}{3q\hbar F})$. Assuming that the local electric field is proportional to the gate voltage, the slope of I_D as a function of V_{GS} $(=\frac{d(\log I_D)}{dV_{GS}})$ is proportional to $E_g^{3/2}$. Hence, at a given V_{GS}, the swing is expected to decrease with the slight widening of the gap caused by the decreasing temperature.

3.2. *Effect of traps*

InAs/oxide traps and bulk traps adjacent to the hetero-interface affect the performance of the TFET by strikingly different mechanisms. One can study them separately by activating each trap type individually. The transfer characteristics simulated by instantiating each of the two trap types are plotted in Fig. 3(a). Tunneling at bulk traps takes place near the hetero-interface in two steps. An electron tunnels from the VB to the trap creating a hole in the VB and then undergoes another tunneling process to the CB. In the present device, this hetero-junction TAT results in a severe degradation of the SS. It also gives rise to a large leakage current which could render the TFET less attractive for low-power applications. Suppressing bulk traps near the hetero-junction will significantly improve the TFET characteristics.

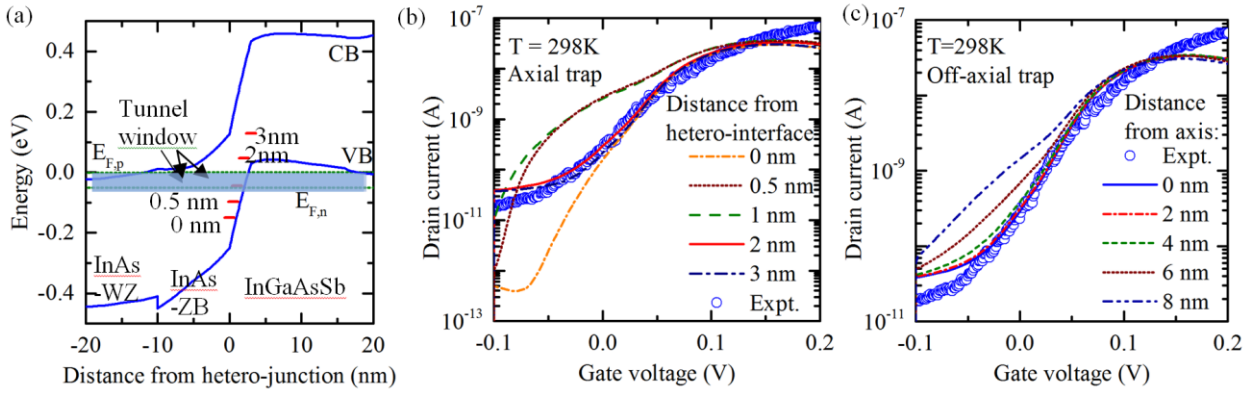

Figure 4. *(a) Energetic and spatial location of the single trap leading to the I_D-V_{GS} characteristics by 3D simulations of the nanowire TFET shown in Fig. 1(a). (b) Variation of the location of single trap along the axis of the nanowire in segment R-1. (c) Variation of the location of the trap along the radius, at an axial distance of 2 nm.*

At the oxide/semiconductor interface, the TAT mechanism is different. When a triangular-like well is formed at the oxide interface, an electron can tunnel from the VB of the semiconductor to the interface trap creating a hole in the VB. This is followed by a multi-phonon transition of the electron to the CB as shown in Fig. 3(c). Thus, band bending at the oxide interface is necessary for the TAT process to take place. In the absence of sharp band bending, TAT at the oxide/semiconductor interface is inhibited. Then, both the capture of an electron from the VB and its emission to the CB take place by multi-phonon excitation (see Fig. 3(d)) which is a much weaker generation process. In the present TFET, the InAs channel is intrinsically n-doped. As the gate bias is ramped up, the narrow InAs segment enters the accumulation region. Therefore, the necessary band bending does not take place and the triangular well is not formed at the oxide/InAs interface which inhibits tunneling. Still, oxide interface traps result in surface SRH generation of electron-hole pairs by multi-phonon excitation, which give rise to a weak leakage current (~1 pA as seen in Fig. 3(a)). Oxide/InAs traps change the electrostatics of the TFET and cause a slight degradation of the SS as observed in Fig. 3(a). This is due to electrostatic screening of the InAs channel by the oxide interface traps which reduces the coupling between gate and channel [15]. A variation of the threshold voltage with V_{DS} is observed experimentally. This variation is reproduced in the simulations as shown in Fig. 3(b). The threshold voltage is shifted by nearly 60 mV when V_{DS} is increased from 50 mV to 200 mV. For $V_{DS} > 200$ mV, the threshold voltage shift is negligible in the experimental as well as simulated transfer characteristics. This is a result of the moving Fermi level with V_{DS} in the channel region which changes the occupancy of the oxide/InAs interface traps and alters the interface charge density. A rising V_{DS} increases the positive charge density of the oxide/InAs interface which acts as a positive gate charge and shifts the onset of tunneling to a lower gate bias. In this way, the threshold

voltage is changed. This V_T shift as function of V_{DS} vanishes as soon as the oxide/InAs interface traps are deactivated in the simulation, confirming that the effect has no other reason.

In the above analysis, a spatially uniform distribution of bulk traps in the segment R-1 had been assumed. In reality, the trap charge is expected to be strongly localized at the defect location. To understand how the strong spatial localization of the trap charge changes the picture, a single trap with energy level 100 meV above the VB edge was introduced in the segment R-1. The location of the trap was varied along the axis of the nanowire and also within a circular disk 2 nm away from the hetero-interface. The corresponding transfer characteristics are shown in Figs. 4(b) and 4(c). Since the trap energy is kept constant at 100 meV above the VB edge, moving the trap away from the hetero-interface results in a shift of the energy level relative to Fermi energy (see Fig. 4(a)). This has the consequence that the trap energy level approaches the "tunnel window" (the energy interval at the hetero-junction in which the BTBT rate is maximum) when the trap is 1 nm away from the hetero-interface. Shifting the trap further to a location 2 nm away from the interface moves the trap energy level out of the tunnel window. Therefore, the TAT current is high when the trap is located 1 nm away from the interface, but reduces when the trap approaches a distance of 2 nm from the interface, as can be observed in Fig. 4(b). In a similar way, as the trap is displaced from the axis along the radius, the trap level moves deeper into the tunnel window which results in an increasing TAT. Ref. [24] reports a statistical analysis of a number of nanowire TFETs fabricated using the same process flow. The variation of the swing observed in the fabricated TFETs is in the same range as the simulated data. Our analysis suggests that the variation of the swing is possibly due to the statistical variation of the location of a single trap in segment R-1. Note, that the above analysis does not rule out the presence of defects in other segments. It merely states that the defects in segment R-1 are the most dominant ones due to their location at the tunnel junction.

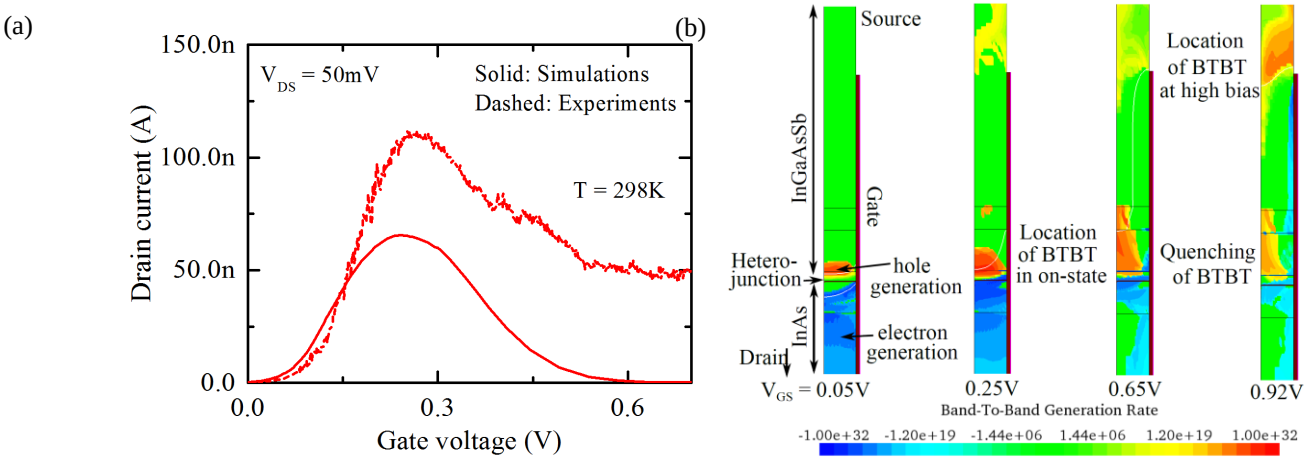

Figure 5. *(a) Measured and simulated transfer characteristics over an extended gate voltage range. (b) Color-mapped diagram of the BTBT rate in the radial cross section of the nanowire TFET at different V_{GS} values (V_{DS} = 50mV). Quenching of BTBT generation at the hetero-junction causes negative transconductance.*

3.4. *Origin of negative transconductance at high gate voltages*

The measured transfer characteristics of the TFET at V_{DS} = 50 mV show a peculiar reduction in the drain current with increasing gate bias above $V_{GS} \approx 0.3$ V as shown in Fig. 5(a). The simulated transfer characteristics (also shown in Fig. 5(a)) correctly reproduce this "negative transconductance region" although the simulated peak current is about 30% lower than the measured one. The origin of this negative transconductance is explained as follows. At low gate bias, electrons accumulate in the i-InAs channel while the p+ doped InGaAsSb source is under weak inversion. As a consequence, BTBT starts at the

InAs/InGaAsSb hetero-interface. With increasing gate bias, BTBT at the hetero-interface becomes stronger and reaches its maximum at $V_{GS} \approx 0.25$ V. Beyond this voltage, volume inversion begins in the entire source overlapped by the gate. This leads to a gradual quenching of the BTBT generation at the hetero-interface till $V_{GS} \approx 1$V. This causes the current to reduce gradually giving rise to the negative transconductance region. The stages of building up the BTBT generation rate at the hetero-junction and its subsequent quenching are discernible in Fig. 5(b) and confirm the above hypothesis. The possibility of obtaining a negative transconductance regime in narrow nanowire TFETs was suggested in Refs. [18, 19]. The transfer characteristics of the present TFET give an evidence of this phenomenon.

3.5. *Possible improvement in the device geometry*

In a previous study of InAs/Si TFETs [20], gate alignment was found to improve the SS of the TFET even in the presence of high trap concentrations at the hetero-interface. In the present TFET, bulk traps adjacent to the hetero-junction degrade the SS. To assess whether gate alignment can mitigate their detrimental effect, the device was simulated with a gate-aligned InAs/InGaAsSb hetero-junction. Transfer characteristics with and without gate alignment are presented in Fig. 6(a). The SS as well as the ON-current improve as soon as the gate is aligned with the p-i junction (which is also the hetero-interface). When the gate is aligned with the pn-junction, the electric field at the pn-junction is superimposed on the strong field at the source edge of the gate. This amplification of the field improves the swing as well as the ON-current. Note that both the distributions of bulk traps and oxide/InAs traps were kept the same as before.

Although the gate alignment improves the TFET characteristics, a small misalignment is found to degrade SS and ON-current significantly. The transfer characteristics simulated with the device geometry having a 5 nm overlap on the InGaAsSb source and the one having an underlap region of 5 nm between the source and the gate are shown in Fig. 6(b). As soon as an overlap of 5 nm is introduced, the improvement over the present TFET geometry is reversed. On the other hand, an underlap of 5 nm results in a less severe degradation of SS and ON-current.

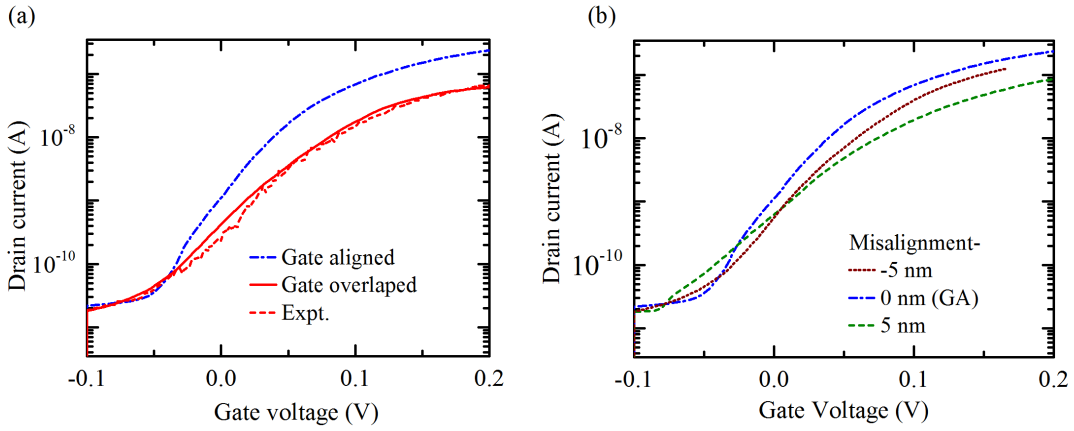

Figure 6. *(a) Transfer characteristics of the nanowire TFET with the gate aligned to the InAs/InGaAsSb hetero-junction and with the gate overlapped on the source (present device geometry). (b) Impact of an overlap of 5 nm and an underlap of 5 nm on the transfer characteristics compared to the gate-aligned TFET.*

In a previous study on InAs/Si TFETs [20] it turned out that gate alignment advances the onset of BTBT with the result that it coincides with that of hetero-interface TAT thus eliminating the leakage floor caused by the latter. This is not observed here. The reason is the nearly broken-gap band alignment at the

InAs/InGaAsSb hetero-interface as opposed to a staggered-gap band alignment at the InAs/Si interface. If the 3 nm long R-1 segment is ignored, the InAs-ZB/InGaAsSb interface exhibits a broken gap. As a consequence, both TAT and BTBT take place at the hetero-interface, at the same gate bias, even in the presence of gate overlap. Hence, BTBT cannot be advanced any further by the band alignment.

4. Conclusion

Measured InAs/InGaAsSb nanowire TFETs with high ON-current and sub-thermal SS were studied by calibrated TCAD to understand how different non-idealities such as bulk traps, and interface traps, affect their performance. The position-dependent composition of the quaternary alloy $In_xGa_{1-x}As_ySb_{1-y}$ extracted from TEM and other physical characterizations was used to determine the values of band gap, band alignment, and effective masses, thus avoiding a fit of these parameters. A good match between simulated and measured *IV*-characteristics at different temperatures could be obtained which validates the approach. The analysis showed that bulk traps present adjacent to the hetero-junction are primarily responsible for the degradation of the SS. Assuming interface traps at the hetero-interface instead of bulk traps can yield a similar agreement, but it is impossible to reproduce the measured leakage current. A further improvement in both ON-current and SS may be achieved by aligning the gate with the InAs/InGaAsSb hetero-junction. However, a misalignment of only 5 nm will completely reverse this advance.

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