Three-dimensional Modeling of Gate Leakage in Si Nanowire Transistors

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Abstract

The gate currents of Si nanowire transistors are investigated using a three-dimensional, real-space, and self-consistent Schrödinger-Poisson solver. The influence of the gate material (metal or poly-Si) and the choice of the dielectric (SiO_2 or high-κ stacks) are studied in details. Then, the performances of nanometer-scaled triple-gate structures are analyzed with respect to ON- and OFF-currents, subthreshold swing, and threshold voltage.

Introduction

The progress achieved in the fabrication of Si nanowire (NW) transistors make these devices an interesting alternative to planar metal-oxide-semiconductor field-effect transistors (MOSFETs) [1]. Due to their better electrostatic control [2], their performances approaching the ballistic limit [3], and their reproducible electronic properties [4], NW field-effect transistors (FETs) could play a significant role in the future of nanoelectronics.

The computer aided design is an important step in the realization of novel devices. A transport simulator dedicated to nanowire FETs requires the inclusion of quantization effects and must be self-consistently coupled to the three-dimensional (3D) calculation of the device electrostatic potential. For that purpose, the mode-space approximation [5-7], which consists in separating the transport direction of the nanotransistors from the others, is often applied. However, this approach does not allow to take gate leakage currents into account due to the imposed boundary conditions [7].

As the equivalent oxide thickness (EOT) of the dielectric layers surrounding the nanowire FETs are approaching the atomic scale, the leakage caused by the direct tunneling of electrons from the gate to the nanowire can no more be neglected. In effect, it increases the OFF-current of the nanodevices and deteriorates the I_{ON}/I_{OFF} ratio. Therefore, we developed a self-consistent three-dimensional Schrödinger-Poisson solver to correctly model the gate leakage currents through single oxide layers or high-κ gate stacks.

Approach

The triple-gate nanowire transistor depicted in Fig. 1 is chosen to illustrate the behavior of gate leakage currents. The 3D Schrödinger equation is solved in the whole device, including the triple-gate region, in the effective mass approximation. Full-band calculations would require a proper description of the oxide layers and of the gate materials, which is out of the scope of this work. A scattering boundary ansatz [8] is used to describe the injection from the source, the drain, and the gate contacts, all treated in a similar manner. Contrary to the recursive Non-equilibrium Green's functions approach [9] all the injection contributions coming from the different gate contacts are included in the solution of the Schrödinger equation.

The nanowire current and charge densities are then calculated with the resulting wave functions. Note that this approach preserves the nanostructure of the gate and, therefore, fully accounts for the state confinement in the contacts. It does not consider the gate contacts as the 3D superposition of one-dimensional tunnel problems [10], but as unified regions. Furthermore, it allows current crowding at the beginning and the end of the gate contacts. This effect cannot be captured by one-dimensional tunnel lines [11].

Three gate-dielectric configurations are examined in this paper. They are shown in Fig. 2 to Fig. 4. They all have an EOT of 1 nm.

(i) SiO_2 oxide layers (t_{SiO_2}=1 nm, relative dielectric constant ϵ_r=3.9, and isotropic effective mass m^*=$0.5m_0$) with n-doped poly-Si gate contacts (affinity $\chi_{poly-Si} = 4.05eV$, doping concentration N_D=10^{20} cm^{-3}, same effective mass as Si).

(ii) SiO_2 oxide layers (same parameters as above) with TiN metal gate contacts characterized by their Fermi level E_{Fm}, their work function ϕ_m=4.35 eV, their electron effective mass (m^*=m_0), and their conduction

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band edge E_{CB}. A virtual conduction band edge E_{CB} situated 2 eV below E_{Fm} is assumed so that all the significant gate states can be injected into the device.

(iii) A SiO_2-HfO_2 stack with TiN contacts. An isotropic effective mass m^*=$0.2m_0$, a relative dielectric constant ϵ_r=25, and a conduction band offset ΔE_{CB}=1.5 eV (relative to Si) are used for HfO_2. The EOT is divided into 0.5 nm of SiO_2 and 3.25 nm of HfO_2.

The poly-Si layers are included in the 3D Schrödinger-Poisson solver as can be seen in Fig. 5. The four thick black layers labeled "OBC" represent regions where open boundary conditions are defined. Hence, states can propagate from the gates into the device, as indicated in the plot. Only one atomic layer of the TiN contacts is sufficient to inject electrons into the device.

Results

The ballistic $I_d - V_{gs}$ characteristics of the Si nanowire transistor presented in Fig. 1 are simulated for V_{ds}=V_{dd}=0.6 V and V_{ds}=0.05 V. Figure 6 shows the results for the poly-Si - SiO_2 gate configuration, Fig. 7 for the TiN - SiO_2 case, and Fig. 8 for the TiN - SiO_2/HfO_2 stack. The performances of the different transistors are summarized in Fig. 9. The threshold voltage V_{th}, the ON-current I_{ON} (defined as I_d at V_{ds}=0.6 V and V_{gs}=V_{th}+0.3), the subthreshold swing SS, the drain-induced barrier lowering $DIBL$, and the maximal gate current density $J_{g,lim}$ are analyzed.

The nanowire FET with n+ poly-Si gate contacts and SiO_2 oxide layers offers the smallest ON-current (1.44 mA/μm) and exhibits a V_{th} too low to be used for logic application (-0.26 V). The replacement of poly-Si by TiN shifts V_{th} to a more appropriate value (0.3 V) [12] and increases I_{ON} to 1.76 mA/μm. The use of a stacked dielectric instead of SiO_2 does not affect V_{th} (0.29 V) or I_{ON} (1.8 mA/μm). The OFF-current and the subthreshold swing are strongly influenced by the choice of the gate material. With SiO_2 oxide layers I_{OFF} is reduced by more than one order of magnitude (from 1.12 to 0.1 μA/μm) if poly-Si is replaced by TiN [12]. The same trend is observed for SS, decreasing from 92.5 mV/dec to 78 mV/dec. The best results (I_{OFF}=2.5 nA/μm, SS=69 mV/dec) are obtained for the high-κ gate stack. Like the SS, the $DIBL$ is large (>60 mV/V) for the three transistor structures reflecting their high sensitivity to short channel effects.

Finally, the gate current density is investigated. The shaded regions in Fig. 10 indicate gate regions where electrons can tunnel into the device, one on the drain side, another on the source side. Figure 11 describes the influence of the gate current on the total nanowire current. In the source the current flowing towards the gate (positive) overcompensates the current coming from the drain (negative) for V_{gs} <0 V. In the drain there are two negative current components flowing in the same direction, one to the gate contact, the other to the source. As expected, the lowest $J_{g,lim}$ (1.4 mA/cm^2) occurs with the TiN - SiO_2/HfO_2 gate, which definitively positions it as the best configuration.

Conclusion

In this paper we presented the simulation of Si nanowire transistors with different gate-dielectric materials. The recourse to a real-space three-dimensional Schrödinger-Poisson solver allowed the inclusion of gate leakage currents and a detailed performance analysis of selected devices was achieved.

Acknowledgment

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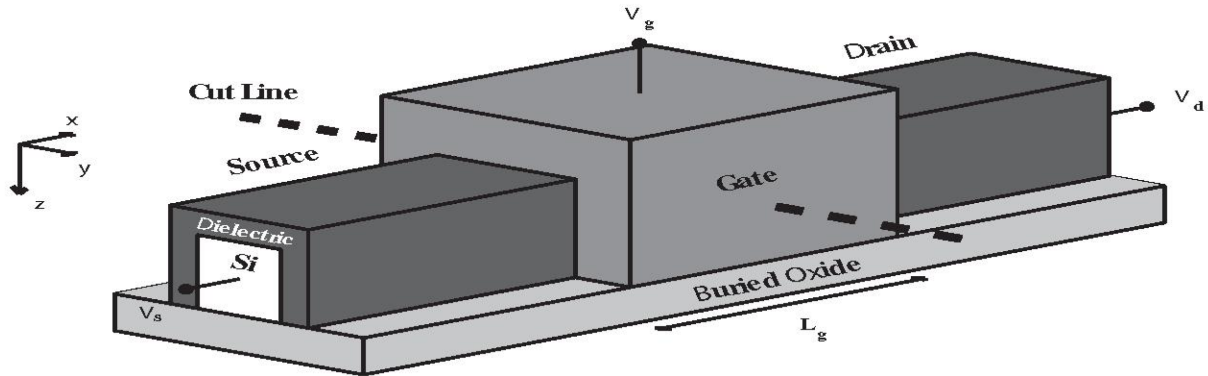

Fig. 1. Schematic view of a triple-gate Si nanowire transistor deposed on a buried oxide and surrounded by three dielectric layers of equivalent oxide thickness EOT=1 nm. The different dielectric and gate material configurations are shown in Fig. 2 to Fig. 4 along the dashed cut line drawn above. The source, the drain, and the gate measure L_s=10 nm, L_d=10 nm, and L_g=10 nm, respectively. States can be injected into the device from all these ports. The x-axis is the transport direction, y and z are directions of confinement. The cross section of the nanowire (white area labeled "Si") is a 3 nm × 3 nm square. A potential V_g is applied to the gate, V_s to the source, and V_d to the drain. The n-doped source and drain regions have a doping concentration N_D=10^{20} cm^{-3}.

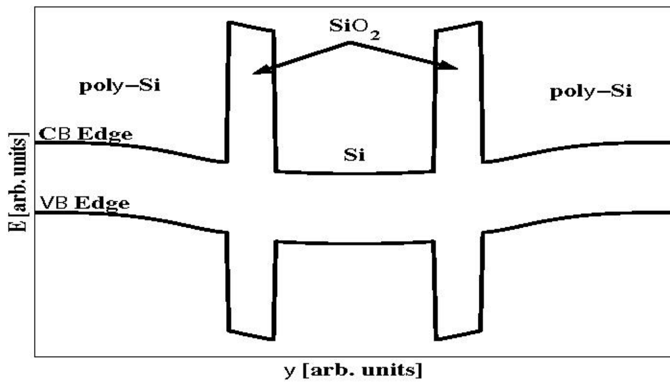

Fig. 2. Schematic band diagram of the n+ poly-Si - SiO_2 gate configuration taken in the middle of the transistor channel along the cut line in Fig. 1.

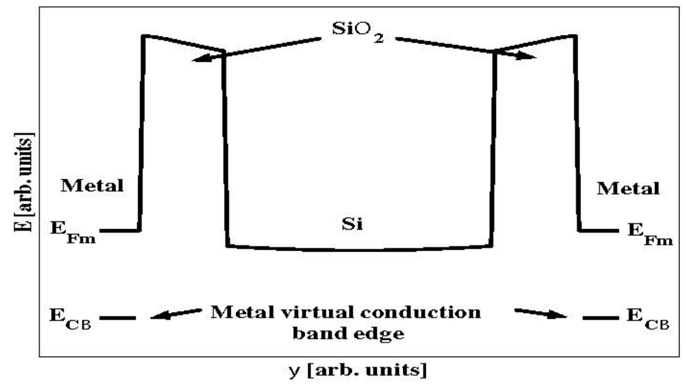

Fig. 3. Schematic band diagram of the metal (TiN) - SiO_2 gate configuration taken in the middle of the transistor channel along the cut line in Fig. 1.

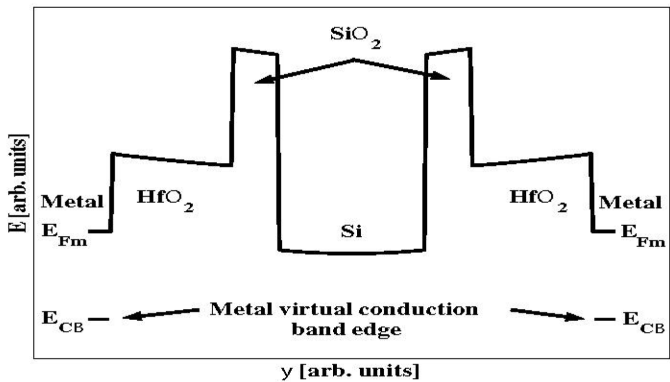

Fig. 4. Schematic band diagram of the metal (TiN) - SiO_2/HfO_2 stacked gate configuration taken in the middle of the transistor channel along the cut line in Fig. 1.

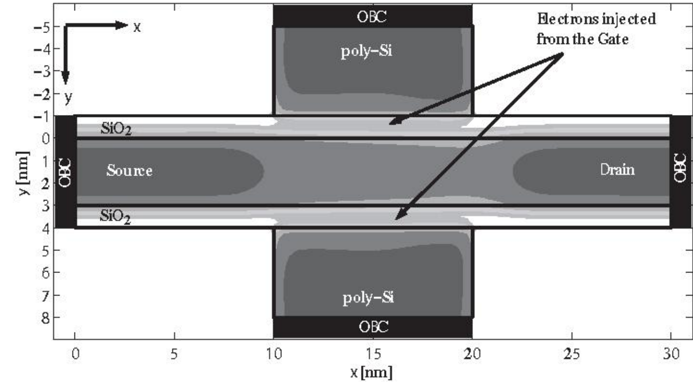

Fig. 5. Logarithmic contour plot of the electron density $n(x,y)$ at the mid-NW height for the poly-Si gate with 1 nm-thick SiO_2 layers (V_{ds}=0.6 V, V_{gs}=0.2 V, band diagram at x=15 nm in Fig. 2).

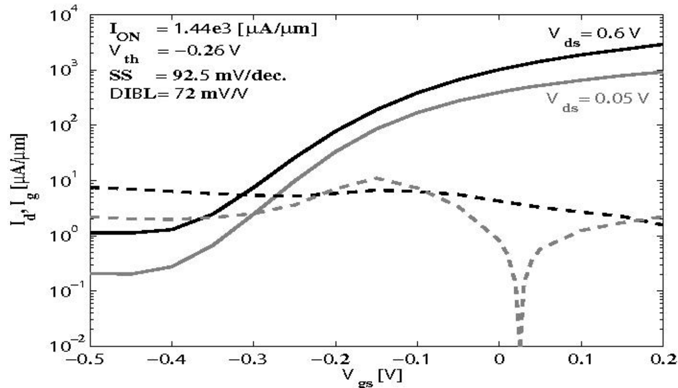

Fig. 6. $I_d - V_{gs}$ characteristics of the nanowire in Fig. 1 with poly-Si gates and 1 nm-thick SiO_2 layers as in Fig. 2. The solid lines stand for the drain current I_d (unit [μA/μm]), the dashed lines for the gate current I_g (unit [μA/μm]). The currents are calculated for V_{ds}=0.05 V (gray lines) and for V_{ds}=V_{dd}=0.6 V (black lines).

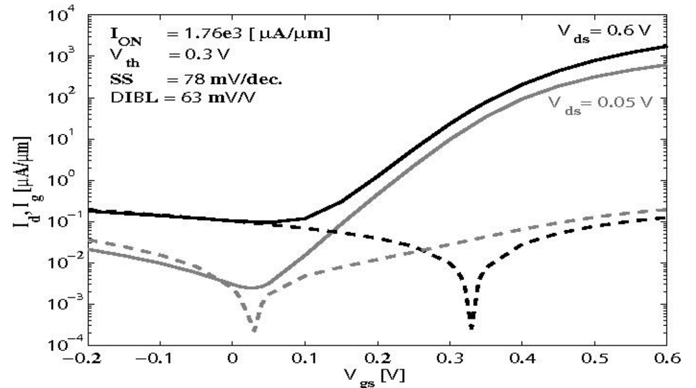

Fig. 7. $I_d - V_{gs}$ characteristics of the nanowire in Fig. 1 with TiN gates and 1 nm-thick SiO_2 layers as in Fig. 3. The solid lines represent drain currents I_d (unit [μA/μm]), the dashed lines gate currents I_g (unit [μA/μm]). The currents at V_{ds}=0.05 V (gray lines) and V_{ds}=V_{dd}=0.6 V (black lines) are given.

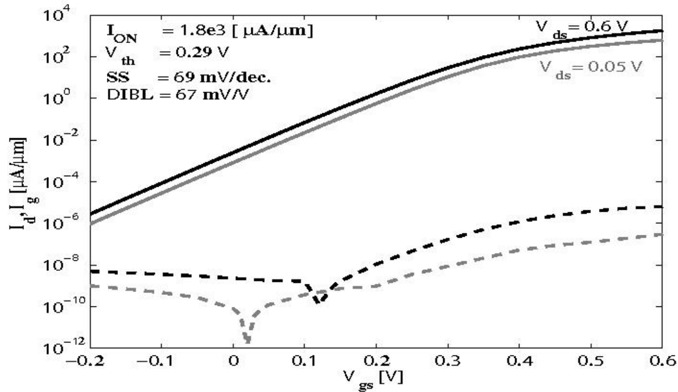

Fig. 8. $I_d - V_{gs}$ characteristics of the nanowire in Fig. 1 with TiN gates, 0.5 nm-thick SiO_2 layers, and 3.25 nm-thick HfO_2 layers as in Fig. 4. The same conventions as in Fig. 7 are used.

	Structure 1	Structure 2	Structure 3
Gate material	poly-Si	TiN	TiN
Gate dielectric	SiO_2	SiO_2	SiO_2-HfO_2
EOT [nm]	1	1	1
Type	n	n	n
V_{dd} [V]	0.6	0.6	0.6
I_{ON} [μA/μm]	1.44e3	1.76e3	1.8e3
V_{th} [V]	-0.26	0.3	0.29
SS [mV/dec.]	92.5	78	69
$DIBL$ [mV/V]	72	63	67
$J_{g,lim}$ [A/cm^2]	1.7e3	900	1.4e-3
I_{ON}/I_{OFF}	1.28e3	1.76e4	7.2e5

Fig. 9. Performance parameters for the three Si triple-gate nanowire transistor structures presented in Fig. 2 to Fig. 4. The currents are normalized with half of the nanowire perimeter (6 nm).

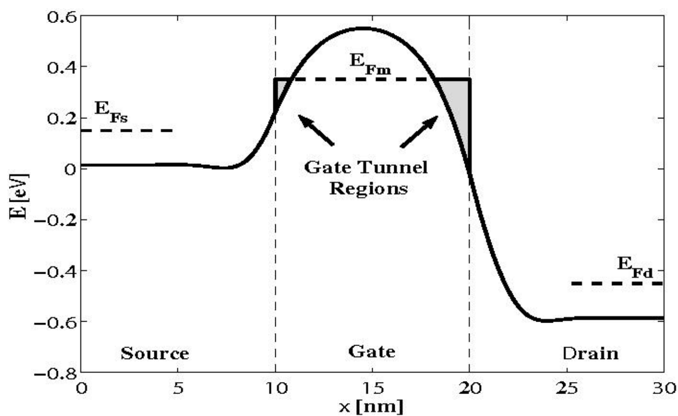

Fig. 10. Self-consistent electrostatic potential of the nanowire with the TiN-SiO_2 gate configuration (Fig. 3). The plot is realized along the transport x-axis on a line situated in the middle of the Si nanowire. The positions of the source (E_{Fs}), the drain (E_{Fd}), and the metal (E_{Fm}) Fermi levels are also shown.

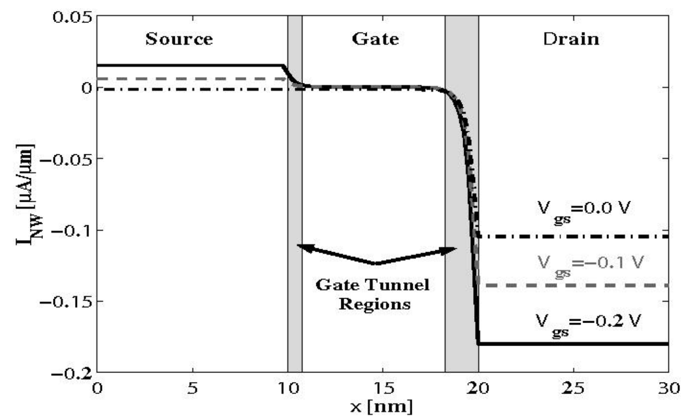

Fig. 11. Total nanowire current I_{NW} (TiN-SiO_2 gate configuration) along the x-axis for V_{ds}=V_{dd}=0.6 V and V_{gs}=-0.2 V (solid black line), V_{gs}=-0.1 V (dashed gray line), and V_{gs}=0.0 V (dash-dot black line).