InAs-GaSb/Si Heterojunction Tunnel MOSFETs: An Alternative to TFETs as Energy-Efficient Switches?

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Abstract

Double-gate ultra-thin-body (DGUTB) InAs-GaSb and InAs-Si gate-all-around nanowire (GAANW) tunnel MOSFETs (TMOSFETs) with realistic dimensions are investigated in this paper. The former with an atomistic and full-band quantum transport solver based on the sp^3s^* tight-binding model, the latter with an effective mass approximation mode-space non-equilibrium Green's function tool. In the InAs-Si GAANW TMOSFETs, band-to-band tunneling is computed in a post-processing step using a rigorous analytical model that accounts for quantization effects. It is found that thicker devices are more promising regarding the ON-state current and low sub-threshold swing, e.g. $I_{\rm ON} = 520\mu{\rm A}/\mu{\rm m}$ and ${\rm SS_{av}} = 37.5$ mV/dec for a InAs-GaSb DGUTB TMOSFET with thickness of 4 nm.

Introduction

Band-to-band tunneling (BTBT) field-effect transistors (TFETs) have received a wide attention from the device community due to their potentially very steep sub-threshold slopes. This feature makes them promising candidates as next generation low-power transistors [1]. To obtain ON-currents high enough to challenge conventional Si MOSFETs, the usage of broken or staggered gap heterojunctions such as InAs-GaSb [2] or InAs-Si [3] is necessary.

However, so far, there has been no experimental demonstration of TFETs that simultaneously exhibit a steep slope (<60 mV/dec) and high ON-current at room temperature. Despite their favorable band alignments, the InAs-GaSb and InAs-Si systems do not provide the desired characteristics because of their poor sub-threshold performance. They are both penalized by the OFF-state leakage currents induced by the material interface quality or the presence of trap-assisted tunneling (TAT), which together increase the sub-threshold swing (SS) above 100 mV/dec.

The negative influence of TAT on hetero-TFETs can be mitigated by slightly modifying their structure and by creating so-called tunnel MOSFETs (TMOSFETs), as illustrated in Fig. 1. The concept of TMOSFETs has been proposed in Ref. [4]. These devices have one more doped region than TFETs, i.e. p-n-i-n or p-i-p-n instead of p-i-n. They are, therefore, composed of an Esaki p-n diode in series with a conventional MOSFET (n-i-n or p-i-p). This architecture preserves the advantages of hetero-TFETs in the ON-state, whereas it is more robust to non-idealities in its OFF-state. In a p-n-i-n configuration the electrons injected from the valence band of the p-type source can always enter the conduction band of the first n-type region, but they are then blocked by the n-i-n MOSFET barrier. Hence, TAT or leaking electrons cannot reach the drain as long as the gate-modulated barrier has not been pushed below a certain level. As a consequence, the TMOSFET is expected to deliver both lower SS and higher ON-current than conventional TFETs.

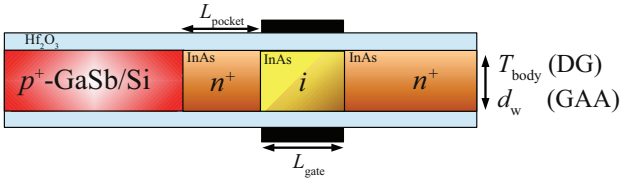

Fig. 1. Schematic view of the cross section of the InAs-GaSb/Si DGUTB/GAANW TMOSFETs considered here. The doping concentrations in the n^+-source (InAs) and p^+-drain (GaSb/Si) regions are $N_{\rm D} = 10^{19}\,{\rm cm}^{-3}$ and $N_{\rm A} = 2 \times 10^{19}\,{\rm cm}^{-3}$, respectively. The supply voltage is set to $V_{\rm DD} = 0.4$ V. The oxide thickness is 2 nm with a permittivity $\varepsilon_{{\rm high}-k} = 20$. The n^+ pocket region of length $L_{\rm pocket} = 20$ nm is needed to enable band-to-band tunneling and MOSFET operations at the same time. The gate length varies from 40 nm to 80 nm. The temperature of devices is assumed to be 300 K.

To date, solely planar bulk-like and size-limited double-gate ultra-thin-body (DGUTB) InAs-GaSb TMOSFETs have been analytically investigated [4], [5]. In this work, we present for the first time quantum transport simulations of both DGUTB InAs-GaSb and InAs-Si gate-all-around nanowire (GAANW) TMOSFETs with realistic dimensions. We compare different gate lengths, body thicknesses and diameters for the DGUTB and GAANW TMOSFETs, respectively, and demonstrate that thicker devices offer a favorable playground for high ON-currents and low SS.

Simulation Approach

The InAs-GaSb DGUTB TMOSFETs are simulated with a two-dimensional (2D) atomistic and full-band quantum transport solver based on the sp^3s^* tight-binding (TB) model [6]. For the InAs-Si GAANW TMOSFETs, a three-dimensional (3D) effective mass approximation (EMA) mode-space non-equilibrium Green's function (NEGF) tool [7] is employed. It self-consistently solves the Schrödinger and Poisson equations. The BTBT currents are computed in a post-processing step using the analytical model of Ref. [8] that accounts for quantization effects. The accuracy of such an approach has been verified with full-band and atomistic calculations for small simulation domains. This allows one to investigate large device structures at low computational costs. The main expressions used to compute the BTBT current are summarized in the following.

In low-dimensional devices, such as nanowire TFETs, the BTBT transmission probability can be calculated straightforwardly from [8]

$$T(E) = \sum_{\nu\nu'} \left| \int \mathrm{d}x\, \tilde{M}_{\nu\nu'}(x)\, \mathcal{S}_{\nu\nu'}(x,E) \right|^2, \quad (1)$$

where the function $\mathcal{S}_{\nu\nu'}(x,E)$,

$$\mathcal{S}_{\nu\nu'}(x,E) = \sqrt{A_{\mathrm{c}\nu}(x,x;E) A_{\mathrm{v}\nu'}(x,x;E)}, \quad (2)$$

contains the overlap of the electron $A_{\mathrm{c}\nu}$ and hole $A_{\mathrm{v}\nu}$ spectral functions. The conduction-valence bands (CVBs) coupling strength is re-defined as

$$\tilde{M}_{\nu\nu'}(x) = \int \mathrm{d}^2\mathbf{r}_\perp\, M_{\mathrm{cv}}(x,\mathbf{r}_\perp) F^*_{\mathrm{c}\nu}(\mathbf{r}_\perp;x) F_{\mathrm{v}\nu'}(\mathbf{r}_\perp;x), \quad (3)$$

where $\mathbf{r}_\perp = (y,z)$. $F_{\mathrm{c(v)}\nu}$ is the electron (hole) wave function in the direction of confinement for the state ν. Special attention has to be payed to the CBVs coupling strength in low-dimensional structures since the electric field polarizes the momentum matrix elements [9]. Hence, the latter depend on the directionality of the total electron wave vector, and the coupling strength M_{cv} is generally expressed as [8]

$$M_{\mathrm{cv}} = \frac{\hbar p_{\mathrm{cv}}}{\sqrt{3 m_0 E_{\mathrm{g}}}} \sqrt{\sum_{j=1}^{n} C_j(\theta) \mathcal{E}_j^2}. \quad (4)$$

Here, j denotes the x, y ($n = 1, 2$) and z ($n = 3$) directions, and $\mathcal{E}_j$ is the j-component of the electric field. In case of the conduction and light hole band coupling, the functions $C_j(\theta)$ are [8], [9]:

$$C_x(\theta) = \frac{1}{2} + \frac{3}{2}\cos^2\theta \quad (5)$$

$$C_y(\theta) = C_z(\theta) = \frac{5}{4} - \frac{3}{4}\cos^2\theta \quad (6)$$

with

$$\cos^2\theta = \begin{cases} 1 - \frac{W_\nu}{E} & \text{if } |E| \geqslant |W_\nu| \\ 0 & \text{otherwise} \end{cases}. \quad (7)$$

Note that in low-dimensional semiconductor devices the sub-band energies W_ν may be position-dependent. The current can be computed by the Landauer formula once the transmission probability is known.

Quantum generation rate

Based on the semi-classical expression of the BTBT current, $I_{\mathrm{s-c}} = q \int G(\mathbf{r}) \mathrm{d}^3\mathbf{r}$, and by using Eqs. (1) to (3) together with the Landauer formula, an expression for the BTBT generation rate G can be established:

$$G(\mathbf{r}) = \frac{2}{\hbar} \int \frac{\mathrm{d}E}{2\pi}\, \mathcal{T}(\mathbf{r},E)\, (f_{\mathrm{v}}(E) - f_{\mathrm{c}}(E)). \quad (8)$$

The function $\mathcal{T}(\mathbf{r},E)$ is related to the BTBT probability as,

$$\mathcal{T}(\mathbf{r},E) = \sum_{\nu\nu'} \tilde{M}_{\nu\nu'}(\mathbf{r}) \mathcal{S}_{\nu\nu'}(x,E) \int \mathrm{d}x' \tilde{M}_{\nu\nu'}(x') \mathcal{S}_{\nu\nu'}(x',E), \quad (9)$$

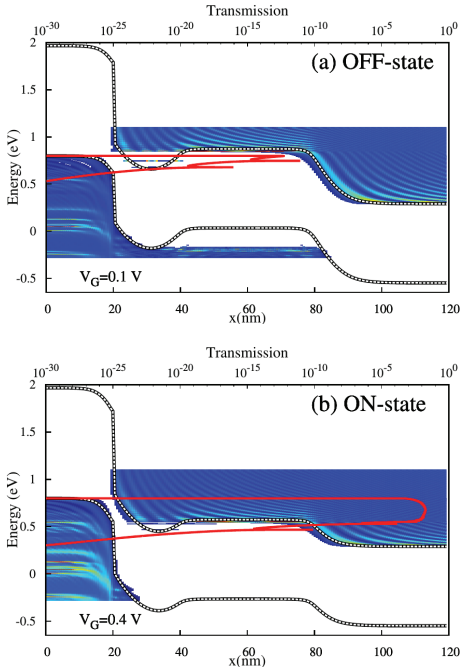

Fig. 2. Full-band, and atomistic simulation of a InAs-GaSb DGUTB TMOSFET with $T_{\mathrm{body}} = 2$ nm. (a) OFF-state band diagram: the electrons tunneling through the InAs-GaSb junction are blocked by the barrier that forms inside the intrinsic region and that is controlled by the gate contacts. (b) ON-state band diagram: the potential barrier in the intrinsic region is lowered below the valence band edge of the source, allowing the BTBT-electrons to flow to the drain side and contribute to the current. In both sub-plots (a) and (b), $V_{\mathrm{DS}} = 0.4$ V. The BTBT tunneling probability (red lines) and contour of the relevant local density-of-states (LDOS) are superimposed to the band diagrams (dashed curves).

with the CVBs coupling $\tilde{M}_{\nu\nu'}(\mathbf{r})$ defined such that $\tilde{M}_{\nu\nu'}(x) = \int \mathrm{d}^2\mathbf{r}_\perp \tilde{M}_{\nu\nu'}(\mathbf{r})$.

RESULTS

The InAs-GaSb DGUTB and InAs-Si GAANW TMOSFETs of Fig. 1 are considered in this work. The ON-and OFF-state band edge diagrams of the InAs-GaSb device with a body thickness $T_{\mathrm{body}} = 2$ nm and $L_{\mathrm{gate}} = 40$ nm are plotted in Fig. 2 to shed light on the functionality of TMOSFETs. The BTBT transmission probability and the local density-of-states (LDOS) are also shown. The resonance levels situated at the p-n heterojunction induce the observed peaks in the BTBT transmission. Electrons that tunnel through the p-n InAs-GaSb interface are stopped by the potential barrier arising in the intrinsic region and controlled by the gate contact (Fig. 2(a)). The leakage current is thus reduced to approximately $I_{\mathrm{D}} \approx 10^{-5}\mu\mathrm{A}/\mu\mathrm{m}$.

Increasing the gate-to-source voltage V_{GS} pushes down the MOSFET barrier so that the injected electrons can flow to the drain side. This occurs when the maximum of the conduction band edge in the intrinsic region becomes lower than the valence band edge of the source. The ON-state band diagram is reported in Fig. 2(b), the corresponding transfer characteristics in Fig. 3(a-c) for $T_{\mathrm{body}} = 2$ nm, and 4 nm with $L_{\mathrm{gate}} = 40$,

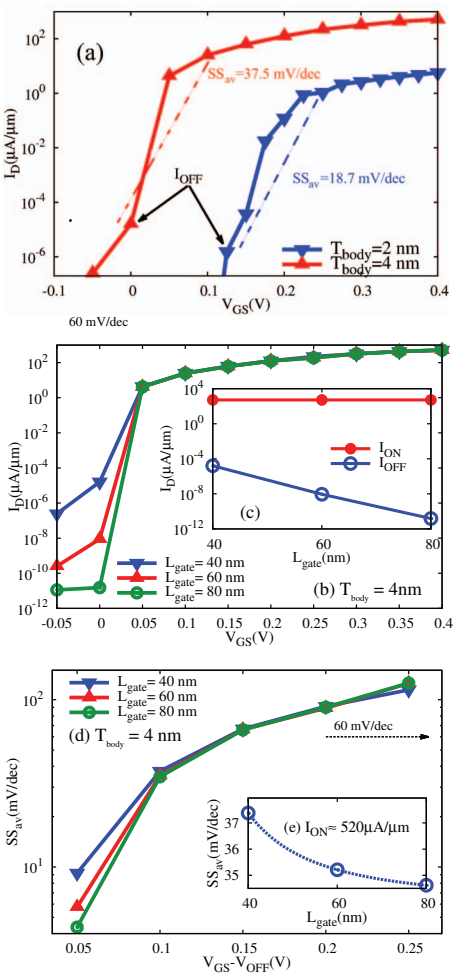

Fig. 3. Room temperature $I_{\rm D}$-$V_{\rm GS}$ transfer characteristics at $V_{\rm DS} = 0.4$ V of the InAs-GaSb DGUTB TMOFET with (a) body thicknesses: $T_{\rm body} = 2$ nm (blue line) and $T_{\rm body} = 4$ nm (red line) with $L_{\rm gate} = 40$ nm. Note that the average sub-threshold swing $\rm SS_{av}$ depends on the body thickness whereas the $I_{\rm ON} = I_{\rm D}(V_{\rm GS} = V_{\rm OFF} + V_{\rm DD})$ increases by 2 orders of magnitude in the thicker device (520 vs. 6 μA/μm). $V_{\rm DD}$ is set to 0.4 V. $\rm SS_{av}$ is calculated over six orders of magnitude starting from the OFF-state current, i.e. $I_{\rm OFF} = I_{\rm D}(V_{\rm GS}$=0 V) and $I_{\rm OFF} = I_{\rm D}(V_{\rm GS}$ =0.12 V) for the devices with $T_{\rm body} = 4$ and 2 nm, respectively. (b) Comparison of the $I_{\rm D} - V_{\rm GS}$ characteristics for $T_{\rm body} = 4$ nm with different $L_{\rm gate} = 40$, 60, and 80 nm. The inset (c) shows $I_{\rm ON}$ and $I_{\rm OFF}$ as a function of $L_{\rm gate}$. While $I_{\rm ON}$ remains almost constant, $I_{\rm OFF}$ exponentially decreases. (d) $\rm SS_{av}$ vs. $V_{\rm GS}$-$V_{\rm OFF}$: $\rm SS_{av}$ increases as the difference $V_{\rm GS}$-$V_{\rm OFF}$ increases. $\rm SS_{av}$ vs. $L_{\rm gate}$ is plotted in the inset (e): $\rm SS_{av}$ slightly improves as $L_{\rm gate}$ increases. The simulations were performed with an atomistic quantum transport solver relying on the TB model.

60, and 80 nm. At $L_{\rm gate} = 40$ nm, a $I_{\rm ON}/I_{\rm OFF}$ ratio of 10^6 with $I_{\rm ON} = 6\mu$A/μm and $\rm SS_{av} = 18.7$ mV/dec is observed for the thinner TMOSFET, 10^8 with $I_{\rm ON} = 520\mu$A/μm and $\rm SS_{av} = 37.5$ mV/dec for the larger one (Fig. 3(d-e)).

Figure 4 shows the ON- and OFF-state band diagram of the InAs-Si GAANW TMOSFET with $d_{\rm W} = 8$ nm and $L_{\rm gate} = 40$ nm as well as the BTBT transmission probability and LDOS. As compared to the InAs-GaSb case, there is a second BTBT component active in the OFF-state while

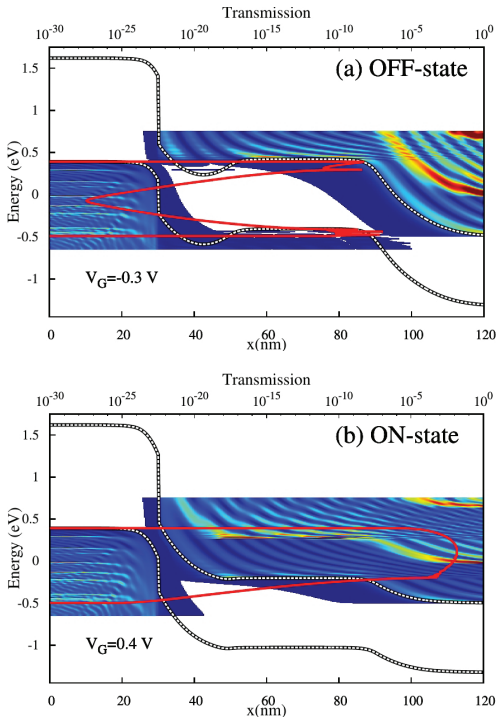

Fig. 4. Band diagram of the InAs-Si GAANW TMOSFET at $V_{\rm DS} = 0.4$ V with $d_{\rm W} = 8$ nm as simulated with an EMA-based mode-space NEGF quantum transport solver. BTBT is added in a post-processing step with the analytical model of Ref. [8]. The same plotting conventions as in Fig. 2 are used. (a) OFF-state band diagram: A second, intra-InAs BTBT component appears because of the hole states localized in the channel. (b) ON-state band diagram: BTBT only occurs through the n-InAs and p-Si heterojunction.

is situated in the InAs region. The $I_{\rm D}$-$V_{\rm GS}$ curves of the GAANW TMOSFETs with $d_{\rm W} = 10$ nm, and 8 nm with $L_{\rm gate} = 40$, 60, and 80 nm are given in Fig. 5(a-c). Higher currents are obtained for the thicker nanowire, $I_{\rm ON} \approx 1.1\mu$A or 110μA/μm (diameter normalization), while the thinner one with $I_{\rm ON} \approx 0.15\mu$A or 19μA/μm has the lowest $\rm SS_{av}$, e.g. 28 instead of 37.5 mV/dec. $\rm SS_{av}$ vs. $V_{\rm GS}$-$V_{\rm OFF}$ is reported in Figs. 3 and 5(d-e). In both cases, $\rm SS_{av}$ increases as the difference $V_{\rm GS}$-$V_{\rm OFF}$ increases. $\rm SS_{av}$ vs. $L_{\rm gate}$ is plotted in the inset of Fig. 5(e): $\rm SS_{av}$ slightly improves as $L_{\rm gate}$ increases.

Finally, the quantum generation rate (QGR) of the InAs-Si GAANW TMOSFET with $d_{\rm W} = 8$ nm and $L_{\rm gate} = 40$ nm is depicted in Fig. 6. It clearly appears that due to confinement the QGR is mainly located at the center of the nanowire and happens at the InAs-Si heterojunction. It is worthwhile noting that carriers start to be generated close to the channel-oxide interface when a large gate voltage is applied.

TABLE I.
MATERIAL PARAMETERS USED IN THE EMA-BASE MODE-SPACE NEGF QUANTUM TRANSPORT SIMULATIONS OF INAS-SI GAANW TMOSFETS.

Material	$m_{\rm c}(m_0)$	$m_{\rm v}(m_0)$	$E_{\rm g}$(eV)	$\chi_{\rm EA}$(eV)
InAs	0.023	0.026	0.354	4.9
Si	0.258	0.144	1.12	4.05

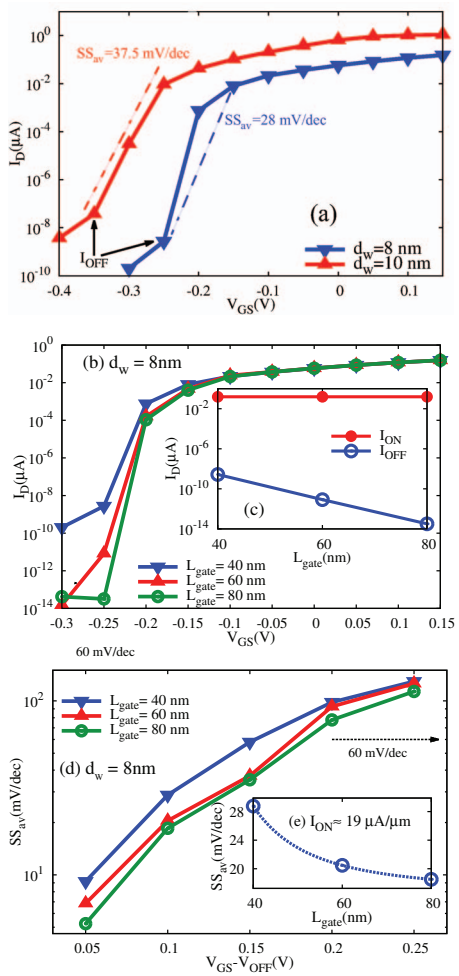

Fig. 5. Room temperature $I_{\rm D}$-$V_{\rm GS}$ transfer characteristics at $V_{\rm DS} = 0.4$ V of the InAs-Si GAANW TMOFETs with (a) different diameters: $d_{\rm W} = 8$ nm (blue line) and $d_{\rm W} = 10$ nm (red line) with $L_{\rm gate} = 40$ nm. Increasing the nanowire diameter reduces its band gap, which amplifies the leakage current caused by intra-InAs BTBT. In spite of that, the average sub-threshold swing $\rm SS_{av}$ remains very small and comparable to the one obtained with the thinner structure, while the ON-current, as defined in Fig. 3, is boosted. $\rm SS_{av}$ is averaged over eight orders of magnitude from the OFF-state current, i.e. $I_{\rm OFF} = I_{\rm D}(V_{\rm GS} = -0.25$ V) and $I_{\rm OFF} = I_{\rm D}(V_{\rm GS} = -0.35$ V) for the devices with $d_{\rm W} = 8$ nm and $d_{\rm W} = 10$ nm, respectively. (b) Comparison of the $I_{\rm D}$-$V_{\rm GS}$ characteristics for $d_{\rm W} = 8$ nm with different $L_{\rm gate} = 40$, 60, and 80 nm. The inset (c) shows $I_{\rm ON}$ and $I_{\rm OFF}$ as a function of $L_{\rm gate}$. Similar to Fig. 3, $I_{\rm ON}$ remains almost constant, whereas $I_{\rm OFF}$ exponentially decreases. (d) $\rm SS_{av}$ vs. $V_{\rm GS}$-$V_{\rm OFF}$: $\rm SS_{av}$ increases as the difference $V_{\rm GS}$-$V_{\rm OFF}$ increases. $\rm SS_{av}$ vs. $L_{\rm gate}$ is plotted in the inset (e): $\rm SS_{av}$ improves as $L_{\rm gate}$ increases. The simulations were performed with the same EMA tool as in Fig. 4.

Conclusions

InAs-GaSb DGUTB and InAs-Si GAANW tunneling MOSFETs with realistic dimensions have been simulated via an atomistic TB model and a well-calibrated EMA-based mode-space NEGF tool, respectively. It has been shown that such devices can provide a high ON-current with a low SS and that thicker devices are more promising regarding the ON-current.

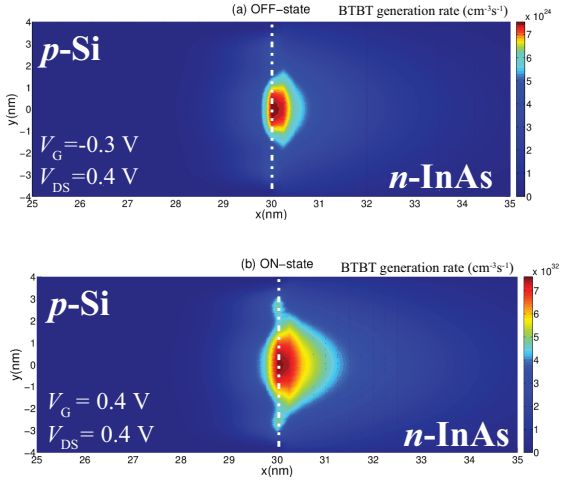

Fig. 6. Room temperature quantum generation rate (QGR) of the InAs-Si GAANW TMOFET with a diameter $d_{\rm W} = 8$ nm at (a) $V_{\rm GS} = -0.3$ V (OFF-state) and (b) $V_{\rm GS} = 0.4$ V (ON-state). Due to confinement the QGR is located at the center of the nanowire and occurs at the InAs-Si heterojunction. At high gate voltage, an electron channel forms in the MOSFET part of the device. Carriers start to tunnel and be generated close to the semiconductor/oxide interface. QGR is computed by means of Eqs. (8) and (9).

Acknowledgments

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