Materials Science and Engineering B 114–115 (2004) 15–19

www.elsevier.com/locate/mseb

Influence of HALO and drain-extension doping gradients on transistor performance

Axel Erlebach[a,*], Thomas Feudel[b], Andreas Schenk[c], Christoph Zechner[a]

[a] *ISE AG, Affolternstr. 52, 8050 Zurich, Switzerland*
[b] *AMD Saxony LLC and Co. KG, Wilschdorfer Landstrasse 101, D-01109 Dresden, Germany*
[c] *ETH Zurich, Integrated Systems Laboratory, Gloriastr. 35, CH-8092 Zurich, Switzerland*

Abstract

For achieving a physical gate length lower than 50 nm and keeping at the same time good transistor performance, a careful design of drain-extension and channel doping profiles is required. For this we investigate the influence of drain-extension and HALO doping gradients at the drain-extension channel junction (DECJ). It is found that the influence of the drain extension doping gradient on the threshold voltage roll-off behavior is small for steep profiles when keeping saturation current and overlap capacitance constant. On the other hand, the shape of the HALO profile influences the threshold voltage roll-off characteristics and allows to adjust the roll-off behavior without degrading the saturation current dramatically. The effect of process parameters like HALO implantation angle and energy on the transistor performance is studied.
© 2004 Published by Elsevier B.V.

Keywords: Drain-extension; Doping; Transistor; HALO; Threshold voltage roll-off; Saturation current

1. Introduction

For very deep sub-μm technologies, down scaling and transistor performance are strongly connected with the design of appropriate doping profiles close to the drain-extension channel junction (DECJ) under the gate. Thereby, the roll-off behavior of the threshold voltage as well as the saturation current play an important role and are in the focus of attention in improving transistor performance. The goal is to get a high stability of threshold voltage against gate length variation for gate lengths close to the value of the nominal transistor, to obtain high saturation current I_{on} (I_{on}: drain current at $V_g = V_{dd}$ and $V_d = V_{dd}$, V_{dd}: operating voltage), and low I_{off} current (I_{off}: drain current at $V_g = 0\,V$ and $V_d = V_{dd}$) simultaneously. On the one hand, this means to suppress both the punch through from the drain side and the lowering of the source-channel potential barrier. On the other hand, one needs to decrease the source-channel potential barrier and thus, the net concentration at the channel side of the DECJ in order to have high I_{on}. Concluding, one has to find a trade-off between improving the threshold voltage roll-off behavior and keeping constant I_{on} and overlap capacitance C_{ov}.

A simple increase of channel doping concentration would give a higher stability against gate length variations and a low I_{off} value. However, this way one also has to accept a higher threshold voltage and a lower mobility in the inversion layer and, as a consequence, a lower saturation current. The improvement of the roll-off behavior can also be achieved by increasing the doping profile gradient of the drain-extension profile. The price one has to pay is an increase of the threshold voltage and a degradation of the saturation current for the nominal gate length. Optimizing HALO implantation dose and distance between DECJ and gate edge in order to compensate for the change of threshold voltage, saturation current, and overlap capacitance, results in a worsening of the roll-off behavior. Therefore, one needs to find another way in order to improve the threshold voltage roll-off behavior.

The main tools used for the present investigation are 2D process and device simulation with $DIOS_{ISE}$ [1] for process and $DESSIS_{ISE}$ [2] for device simulation, respectively. The process simulator is applied to generate doping profiles and

* Corresponding author.
E-mail address: erlebach@ise.ch (A. Erlebach).

0921-5107/$ – see front matter © 2004 Published by Elsevier B.V.
doi:10.1016/j.mseb.2004.07.022

device structures. The simulated drain-extension and channel profiles are adjusted to match typical device data of very deep sub-μm technologies like threshold voltage, saturation current, junction depth, and overlap capacitance. However, no specific calibration is done and many process steps are simplified. Device simulation is performed with the drift diffusion model using quantum corrections. The parameter set of Darwish [3] is used for the inversion layer mobility. The poly depletion effect is taken into account by solving the Poisson equation in the poly silicon gate. It is well-known that quasi-ballistic effects play an important role in the case of ultra-short gates. Monte Carlo device simulation [4,5] is therefore, well suited for those investigations, whereas hydrodynamic and drift diffusion models give either too high or too low values for the saturation current. However, since Monte Carlo simulation still requires too much computation time, it can hardly be used for daily industrial applications where many different process and device variants have to be considered. Thus, we fit the high-field mobility in the drift diffusion model to MC simulation results and then perform all other simulations with the calibrated drift diffusion model. The resulting failure will most probably not change the influence of the doping concentration on the electrical transistor behavior.

In chapter II, we show results of the investigation of the influence of the drain-extension doping gradient on the threshold voltage roll-off characteristics. Chapter III explains the effect of the compensation of threshold voltage shift and saturation current degradation by the adjusting distance between DECJ and gate edge and by decreasing the HALO implantation dose. The last section, investigates the influence of the shape of the HALO profile on the roll-off curves.

Table 1
Saturation current for different drain-extension doping gradients with and without compensation of saturation current degradation and overlap capacitance lowering

Variant	I_{on} (μA)
A	590
B	**360**
C	490
D	530
E	550

(A: offset = 4 nm/low doping gradient, B: offset = 1 nm/high doping gradient, C: offset = 1 nm/high doping gradient, D: offset = 1 nm/high doping gradient, E: offset = 1 nm/high doping gradient). The HALO dose for the variants A, B, and C is 4.0×10^{13} cm^{-2}, whereas the HALO dose for the variants D and E is 3.5×10^{13} cm^{-2} and 3.0×10^{13} cm^{-2} respectively. The saturation current is always for a constant I_{off} of 10 nA.

2. Influence of drain-extension profile on threshold voltage roll-off behavior

Fig. 1 presents the influence of the drain-extension doping gradient on the threshold voltage at a drain bias of 1 V. The threshold voltage is determined at a drain current level of 0.1 μA, where the current is normalized by the gate length. The slope of the drain-extension profile is varied between 2 and 10 nm per decade, where an abruptness of 3. . .5 nm per decade is required for a gate length of 32. . .37 nm according to the ITRS roadmap [6]. Fig. 1 clearly shows that steeper profiles result in a better roll-off behavior. On the other hand, the threshold voltage is strongly increased by about 100 mV for the longest channel considered here. The increase of the threshold voltage causes a decrease of the saturation current due to the lowering of the inversion charge. The saturation current is further degraded by the lowering of the mobility

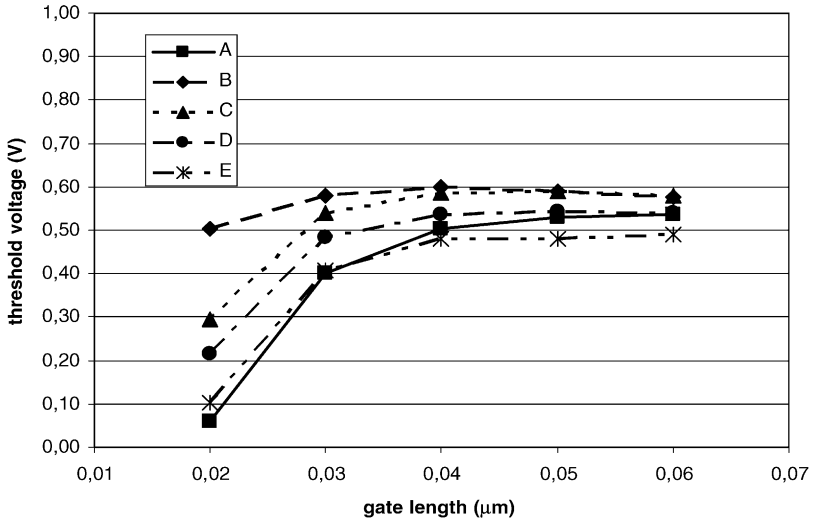

Fig. 1. Dependency of threshold voltage on gate length for different drain-extension doping gradients with and without compensation of saturation current and overlap capacitance lowering (A: offset = 4 nm/low doping gradient, B: offset = 1 nm/high doping gradient, C: offset = 1 nm/high doping gradient, D: offset = 1 nm/high doping gradient, E: offset = 1 nm/high doping gradient). The HALO dose for the variants A, B, and C is 4.0×10^{13} cm^{-2}, whereas the HALO dose for the variants D and E is 3.5×10^{13} cm^{-2} and 3.0×10^{13} cm^{-2}, respectively.

due to the higher doping concentration (higher doping concentration results in higher electric field at the silicon-oxide interface). The higher threshold voltage is always connected with a lower I_{off}, whereas the mobility degradation affects mainly the saturation current. The overlap capacitance is reduced by about 50%. For a fair evaluation of the different variants (see Table 1), we have to compare the saturation currents at constant I_{off}. For each variant the same I_{off} of 10 nA is adjusted and the saturation current is extracted. In Table 1 we see that the saturation current of variant B drops down by a factor of two compared to all other variants. Therefore, the increase of the abruptness of the drain-extension profiles results in a strong degradation of the saturation current. The different compensation methods reduce the degradation. However, they also cancel out the improvement of the threshold voltage roll-off behavior.

3. Compensation of degradation of saturation current

The increase of the abruptness of the drain-extension profile results in a degradation of the saturation current. This is a collateral effect of the improvement of the roll-off behavior and has to be corrected in order to obtain the same performance of the nominal transistor as before. The correction can be done by tuning the offset between gate edge and DECJ and by decreasing the HALO dose.

3.1. Distance between DECJ and gate edge

The change of the drain-extension doping gradient results in a change of the overlap capacitance, where steeper profiles give less capacitance. For some configurations and very steep profiles one can even obtain a degraded transistor without any overlap resulting in a high channel resistance and a very low saturation current. In order to keep the overlap capacitance constant the distance between DECJ and gate edge is varied using selected process parameters. This mainly results in a lateral shift of the drain-extension profile and, therefore, in a change of the effective channel length. When increasing the doping gradient of the drain-extension profile one has to generate a shift of the junction of 2–5 nm on both sides of the channel in order to correct for overlap capacitance and saturation current. This correction cancels already a part of the improvement of the roll-off curve. Fig. 2 explains the effect of increasing the drain-extension doping gradient and of compensating the current degradation and overlap capacitance lowering by shifting the DECJ back to the former position.

3.2. HALO implantation dose

The doping gradient of the extension profile changes also the doping concentration at the channel side of the DECJ. A higher drain-extension doping gradient is connected with a higher channel doping concentration. This increases the threshold voltage. The goal is therefore to re-adjust the saturation current by lowering the HALO implantation dose. Because this is accompanied by a decrease of the doping concentration at the DECJ, the space charge region towards the channel at the source and drain sides will be enlarged. This again makes the roll-off behavior worse, partially canceling the improvement achieved by increasing the drain-extension doping gradient (see Fig. 2).

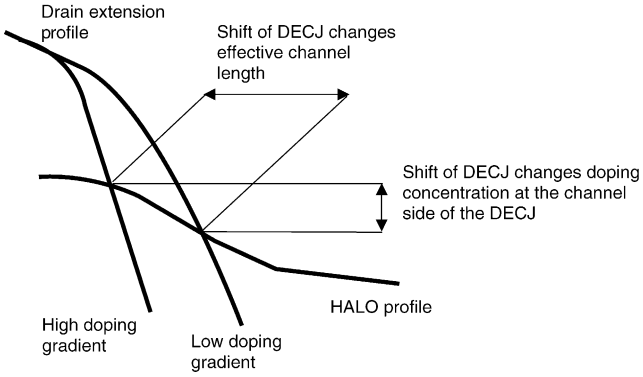

Fig. 2. Explanation of the influence of the doping gradient on channel length and net doping concentration.

The main problem of the compensation methods discussed above is the degradation of the improvement of the threshold voltage roll-off behavior achieved by increasing the drain-extension doping gradient. The degradation of the saturation current is compensated by lowering the HALO dose from 4.0E13 to 3.0E13 cm^{-2} and by increasing the overlap between drain-extension and gate by 3 nm. As one can clearly see, the compensation completely cancels the improvement of the threshold voltage roll-off behavior.

4. Influence of shape of the HALO doping profile on transistor performance

After the necessary adjustments for avoiding the degradation of the saturation current, the possibilities to use the drain-extension doping gradient for improvements of the roll-off behavior are limited. However, the shape of the HALO profile close to the DECJ gives another opportunity to improve the roll-off behavior without degrading the saturation current too much. In this case the goal is to minimize the size of the space charge region at the lateral junction and to raise

Table 2
Saturation current for different HALO implantation energies with I_{off} kept constant at 10 nA

HALO implantation energy (keV)	I_{on} (μA)
2	380
4	485
6	510
8	555
10	560
12	580

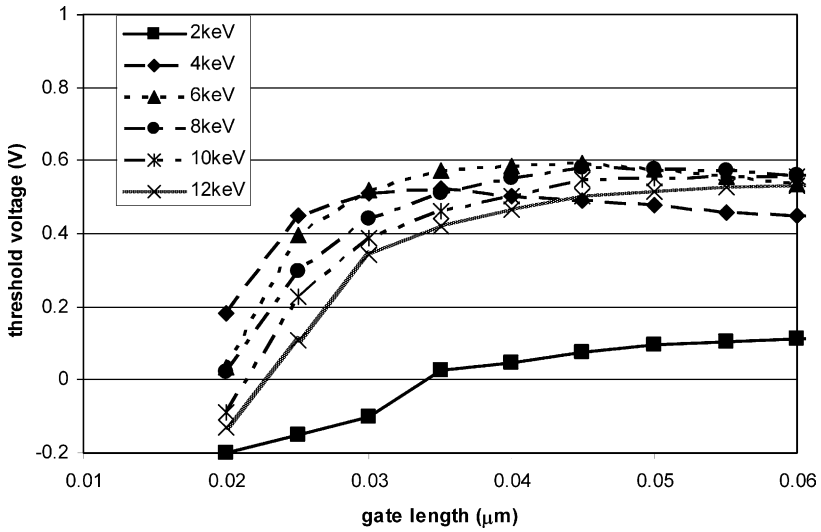

Fig. 3. Influence of the HALO implantation energy on threshold voltage for an offset between DECJ and gate edge of 2 nm, a low drain-extension doping gradient, and a HALO dose of $5.0 \times 10^{13}\,\mathrm{cm}^{-2}$.

the source-channel potential barrier. This way the electrical channel length is increased and the threshold voltage roll-off behavior is improved for a given physical gate length keeping overlap capacitance and saturation current nearly unchanged. The main task is to form the HALO profile in such a way that the net concentration at the channel side close to the DECJ is high enough and the decrease of the channel profile towards the center of the channel is strong enough in order to avoid a significant lowering of the saturation current. The extension of the space charge region at the drain side of the DECJ is in the range of some few nanometers, whereas the extension of the space charge region at the other side of the DECJ is up to 10 times higher. Therefore, a reduction of that space charge region should directly result in an improvement of the roll-off behavior. In the following we consider different ways to construct appropriate profiles using typical process parameters. First we consider the influence of the HALO implantation energy. Then we simulate the effect of the tilt angle. Table 3 gives an overview of the obtained tendencies.

4.1. Influence of HALO implantation energy

The HALO implantation energy controls the location of the maximum of the net concentration in the channel and thus also the concentration at the junction close to the gate oxide silicon interfaces. Higher energy shifts the maximum into the depth and lower energy towards the interface. A too low HALO implantation energy results in a high dopant dose loss in the poly-silicon gate and in the surrounding oxide. Therefore, there should be an optimum for the HALO implantation energy. Fig. 3 shows the effect of the HALO implantation energy on the threshold voltage roll-off. One can clearly see that extremely low and extremely high energies result in bad roll-off characteristics, whereas the medium energies show a better roll-off behavior because the concentration maximum is close to oxide silicon interface and DECJ, and the gradient of the HALO profile towards the middle of the channel is relatively high. In Table 2 the influence of the HALO implantation energy on the saturation current is presented, where I_{off} is kept constant. No pronounced degradation of the saturation current is observed.

4.2. Influence of tilt angle

Using relatively high HALO implantation energy, tilt angles in the range from 25° to 35° result in the deposition of dopant atoms deep under the poly gate fare away from the DECJ. In those cases even the doping concentration in the middle of the channel is dominated by the HALO implantation. Any change of the dose therefore directly causes a change of the threshold voltage, since the doping concentration in the entire channel is changed. The overlap capacitance

Table 3
Influence of typical doping and process parameters on transistor performance

	V_{th}	I_{on}	I_{off}	I_{on}/I_{off}	C_{ov}	Roll-off behavior
Increase of drain-extension doping gradient	↑	↓	↓	↑	↓	Improved
Increase of HALO implantation dose	↑	↓	↓	↑	–	Improved
Influence of HALO implantation energy	O	O	O	O	–	O
Decrease of HALO implantation angle	↓	↑	↑	O	–	Degraded
Decrease of offset between gate edge and DECJ	↓	↑	↑	↓	↑	Degraded

(↓) decrease; (↑) increase; (O) optimum to adjust; (–) no or small influence only.

is only slightly influenced. In general the threshold voltage roll-off behavior is becoming worse with smaller tilt angles. A decrease of the tilt angle down to 25° should result in degraded roll-off curves. For very low tilt angles the transistor has a high off-current and is open for zero gate voltage at gate lengths shorter than 40 nm. However, a higher HALO dose could result in both good roll-off behavior and high saturation current. Further investigations are necessary to confirm this.

5. Conclusion

It has been shown by process and device simulation that the improvement of the roll-off behavior of a deep sub-μm transistor by increasing the doping gradient of the drain-extension profile is limited because of the collateral degradation of saturation current and overlap capacitance. The compensation of the degradation of I_{on} and C_{ov} deteriorates the roll-off behavior. Hence the doping profile gradient of the drain-extension profile is not the proper parameter for improving the transistor performance under these circumstances. On the other hand, it has been demonstrated that optimizing the HALO profile results in a better threshold voltage roll-off behavior without degrading saturation current and overlap capacitance too much.

Acknowledgement

This work has been partially supported by EU grant IST-2001-32061 (IMPULSE project).

References

[1] DIOS-ISE, ISE Integrated Systems Engineering AG, Zurich, 2004.
[2] DESSIS-ISE, Integrated Systems Engineering AG, Zurich, 2004.
[3] M.A. Darwish, J.L. Lentz, M.R. Pinto, P.M. Zeitzoff, T.J. Krutsick, H.H. Vuong, IEEE Trans. Electron Devices 44 (1997) 1529–1538.
[4] J.D. Bude, MOSFET Modeling into the ballistic regime, SISPAD 2000, Seattle.
[5] F.M. Bufler, Y. Asahi, H. Yoshimura, C. Zechner, A. Schenk, W. Fichtner, IEEE Trans. Electron Devices 50 (2003) 418–424.
[6] ITRS Roadmap, 2003.