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Monte Carlo, Hydrodynamic and Drift-Diffusion Simulation of Scaled Double-Gate MOSFETs

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Abstract. Double-gate MOSFETs with gate lengths of 50 and 25 nm are theoretically analyzed by drift-diffusion (DD), hydrodynamic (HD) and self-consistent full-band Monte Carlo (MC) simulation. The underestimation of the on-current I_{on} by DD is found to be stronger than the overestimation by HD. The main differences to the case of bulk MOSFETs are: (i) not only the velocities in the source-side of the channel, but also the sheet densities vary appreciably between the different transport models, (ii) current conservation leads to strong non-equilibrium in the highly doped source region with high velocities and electric fields and (iii) surface roughness appears to become more effective for reduced silicon film thicknesses which might jeopardize the performance enhancement upon further scaling.

Keywords: double-gate MOSFETs, ballistic transport, Monte Carlo device simulation

1. Introduction

Double-gate (DG) MOSFETs are considered as device structures which may take us to the ultimate limit of CMOS scaling [1]. In the sub 0.1 μm regime, however, the on-state of a MOS device is increasingly influenced by quasi-ballistic transport. This raises the question about the physical processes which determine the on-current I_{on} in this regime and how the scaled devices can be predictively simulated. The classical drift-diffusion (DD) and hydrodynamic (HD) device models are expected to fail in this regime [2], but are nevertheless used to estimate the scaling dependence of nanoscale DG-MOSFET performance [3]. An assessment of their accuracy by Monte Carlo (MC) simulation, which considers quasi-ballistic transport on a sound physical basis, was so far concentrated on bulk MOSFETs with gate lengths above around $L_G = 50$ nm (e.g. [4,5,6]) confirming an over- and underestimation of I_{on} by HD and DD, respectively, essentially due to over- or underestimated source-side velocities. In contrast, MC simulations of DG-MOSFETs were not systematically compared to corresponding DD and HD simulations and were often restricted to one device with given L_G (compare e.g. [1,7,8]). It is therefore the aim of this paper to compare MC, HD and DD simulations of DG-MOSFETs with L_G scaled from 50 to 25 nm and to investigate the mechanisms affecting I_{on} in such device structures.

2. Device Structure and Short-Channel Effect

Figure 1 shows the structure and the doping profile of the DG-MOSFETs. The silicon film thickness t_{Si} is always four times smaller than the gate length L_G in order to suppress the short-channel effect, i.e., the increase of the off–current I_{off} upon scaling [1]. This leads for $L_G = 50$ nm to $t_{\text{Si}} = 12.5$ nm and for $L_G = 25$ nm to $t_{\text{Si}} = 6.25$ nm (the configuration $L_G = 25$ nm and $t_{\text{Si}} = 12.5$ nm will also be investigated). The oxide thickness is kept constant at $t_{\text{ox}} = 1$ nm, and a metal gate with a work function of $\Phi_M = 4.72$ eV corresponding to tungsten is assumed. The source/drain regions are doped with 10^{20} cm^{-3} and the doping steepness towards the channel is 5 nm/dec for $L_G = 50$ nm and 2.5 nm/dec for $L_G = 25$ nm. The doping concentration at the center and the edges of the channel is 5×10^{14} cm^{-3} and 5×10^{19} cm^{-3}, respectively. Figure 2 displays the results of the DD model for the transfer

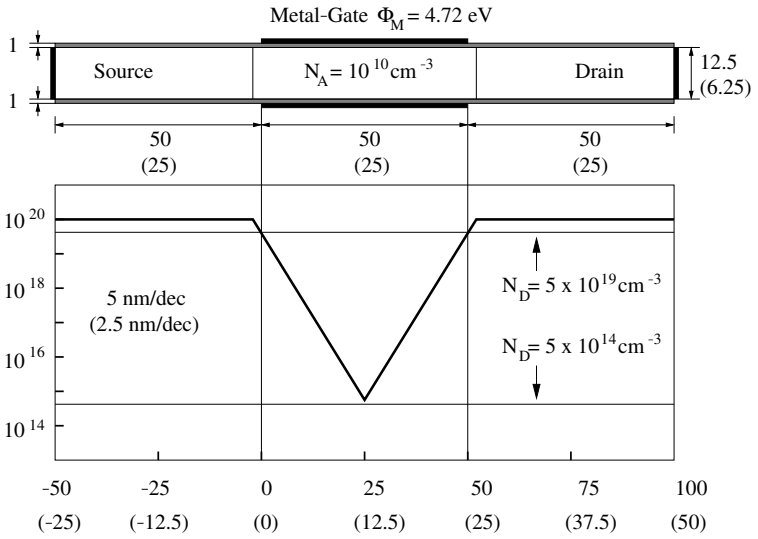

Figure 1. Structure and doping profile of the double-gate MOSFETs. The gate length L_G is scaled from 50 to 25 nm, the silicon film thickness t_{Si} from 12.5 to 6.25 nm and the doping steepness from 5 to 2.5 nm/dec. In addition, a structure with $L_G = 25$ nm and $t_{Si} = 12.5$ nm is considered.

characteristics at a drain voltage of $V_{DS} = 50$ mV for the three configurations. It can be seen that scaling with t_{Si} four times smaller than L_G [1] leaves indeed I_{off} unchanged, whereas I_{off} strongly increases when keeping t_{Si} fixed.

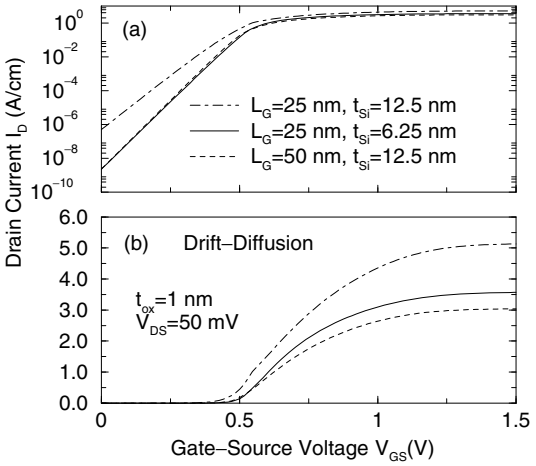

Figure 2. Logarithmic (a) and linear (b) plot of the transfer characteristics at a drain voltage of $V_{DS} = 50$ mV computed with the drift-diffusion model. The results of the configurations $L_G = 50$ nm and $t_{Si} = 12.5$ nm, $L_G = 25$ nm and $t_{Si} = 6.25$ nm as well as $L_G = 25$ nm and $t_{Si} = 12.5$ nm are shown.

3. Simulation Results and Discussion

In Fig. 3, the output characteristics of the DG-MOSFET with $L_G = 50$ nm and $t_{Si} = 12.5$ nm are shown. They are computed by the MC simulator SPARTA [6], by a conventional HD simulation using a constant energy relaxation time of $\tau_w = 0.3$ ps or by a DD simulation.

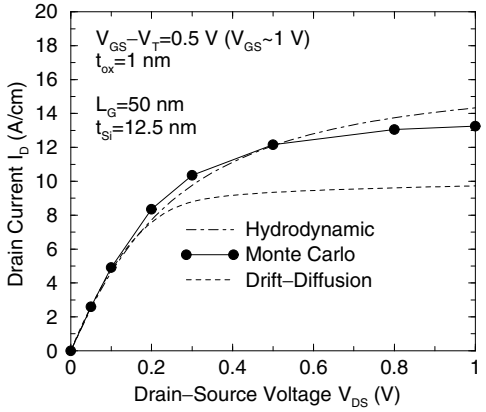

Figure 3. Output characteristics for the double-gate MOSFET with $L_G = 50$ nm and $t_{Si} = 12.5$ nm as resulting from the hydrodynamic (HD), the Monte Carlo (MC) and the drift-diffusion (DD) model. The DD and HD surface mobilities are adjusted to match the MC drain current at $V_{DS} = 50$ mV.

The MC model incorporates surface roughness scattering by a combination of specular and diffusive scattering with 15% diffusive scattering. In the classical simulations, the surface mobility model of Darwish [9] is adopted. However, these different surface mobility models lead to different drain currents also in the linear regime. Therefore, adjustment is necessary to enable a sound comparison of the different simulations in the nonlinear regime. Since the MC surface roughness scattering model was found to reproduce the transfer and output characteristics of state-of-the-art bulk MOSFETs down to effective channel lengths of $L_{\text{eff}} = 40$ nm [6] without any fitting, the Darwish model was always adjusted to yield the same drain current as Monte Carlo at a drain voltage of $V_{\text{DS}} = 50$ mV. Figure 3 shows a smaller overestimation of I_{on} by HD and a stronger underestimation by DD compared to bulk MOSFET simulations [6]. The output characteristics of the scaled DG-MOSFET in Fig. 4 reveal, however, that the validity of the DD model extends to higher drain voltages and that the overestimation of I_{on} by the HD model increases. This indicates that surface roughness scattering is more effective in the MC model than in the Darwish model of DD and HD for thinner Si films.

An additional remark has to be made concerning the hydrodynamic model. In the present simulations, an energy relaxation time of $\tau_w = 0.3$ ps resulting from bulk Monte Carlo simulations has been used. It is true that a smaller hydrodynamic on-current can be obtained when employing a smaller value for τ_w. However, we found that there is no unique choice for τ_w which would match the Monte Carlo on-current at all gate lengths. For example, with $\tau_w = 0.1$ ps the hydrodynamic simulation reproduces the MC on-current at $L_G = 25$ nm, but underestimates the MC on-current at $L_G = 50$ nm by 20%.

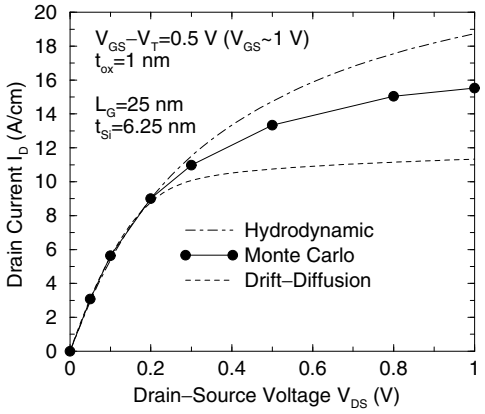

Figure 4. Output characteristics for the double-gate MOSFET with $L_G = 25$ nm and $t_{\text{Si}} = 6.25$ nm as resulting from the hydrodynamic (HD), the Monte Carlo (MC) and the drift-diffusion (DD) model. For comparison, the on-currents for the device with $L_G = 25$ nm and $t_{\text{Si}} = 12.5$ nm are 25.3 A/cm (HD), 21.1 A/cm (MC) and 13.8 A/cm (DD).

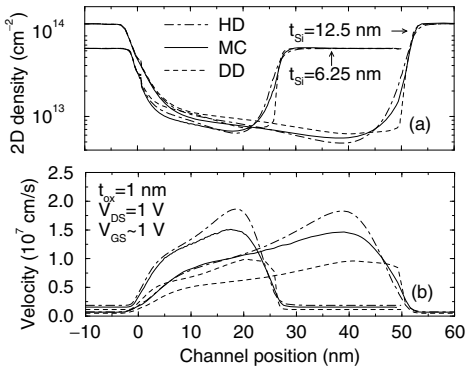

Figure 5. Profiles along the channel of (a) the sheet density obtained by integration of the density perpendicular to the Si/SiO_2 interface and (b) the averaged velocity in the devices with $L_G = 50$ nm/$t_{\text{Si}} = 12.5$ nm and $L_G = 25$ nm/$t_{\text{Si}} = 6.25$ nm.

Figure 5 shows the profiles of sheet density and drift velocity along the channel corresponding to the on-states in Figs. 3 and 4. The most striking features are the nearly equal source-side velocities of MC and HD despite higher I_{on}'s of HD. The reason for the smaller I_{on}'s of MC is the smaller MC sheet density in the source-side of the channel, which should be related to deviations from equilibrium transport in the highly-doped regions and the different effects of surface roughness scattering. This is an important difference to state-of-the-art bulk MOSFETs where the source–side sheet density is almost the same for all three models and the different I_{on}'s can be mainly attributed to different source–side velocities [6]. Another important feature of the DG-MOSFET structures investigated is the non-equilibrium situation in the highly doped source region. The corresponding MC drift velocities (in 10^7 cm/s) are 0.16 and 0.07 in the 25 and 50 nm DG-MOSFET, respectively, in contrast to around 0.015 in the source region of a 0.1 μm bulk MOSFET [6]. This is a consequence of the continuity equation which implies that the current through a cross-section of the DG-MOSFET in Fig. 1 must be the same at every position. For a given doping concentration, an increased on-current therefore involves an increased drift velocity in the source-region which in turn is associated with a high

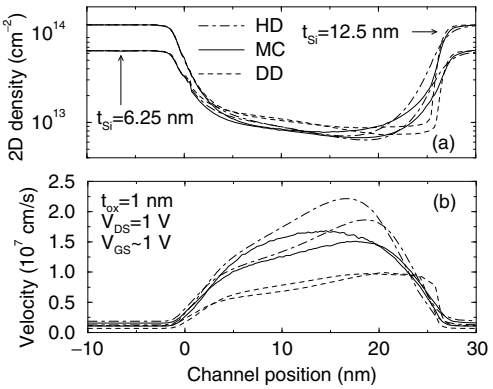

Figure 6. Profiles along the channel of (a) the sheet density and (b) the averaged velocity in the devices with $L_G = 25$ nm/$t_{\rm Si} = 12.5$ nm and $L_G = 25$ nm/$t_{\rm Si} = 6.25$ nm.

electric field in the highly-doped source region of up to 50 kV/cm in the smallest DG-MOSFET.

Figure 6 shows the profiles in the shorter DG-MOSFET for two different $t_{\rm Si}$. The sheet densities are similar for the same models in the source-side, whereas the velocities are much higher for the larger $t_{\rm Si}$ being therefore responsible for a higher $I_{\rm on}$. This emphasizes the important impact of surface roughness scattering for small $t_{\rm Si}$. Its effectiveness in the MC model therefore suggests that further scaling with associated smaller $t_{\rm Si}$ might not further enhance $I_{\rm on}$.

4. Conclusion

DD, HD and MC simulations of scaled DG-MOSFETs were performed. The results show that the on-current is not only associated with the source-side velocity, but also with the sheet densities that vary more strongly for different models and gate lengths than in bulk MOSFETs. Because of the law of current conservation the high on-currents lead to a non-equilibrium situation in the highly doped source region with enhanced drift velocities and electric fields. Surface roughness scattering becomes appreciably more effective for smaller film thicknesses which might jeopardize an on-current improvement upon further scaling.

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