Si-InAs Nanowire Tunnel Diodes

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We report on the electrical characterization of one-sided p^+-Si/n-InAs nanowire heterojunction tunnel diodes to provide insight into the tunnel process occurring in this highly lattice mismatched material system. The lattice mismatch gives rise to dislocations at the interface as confirmed by electron microscopy. In spite of this, a negative differential resistance with peak-to-valley ratios of up to 2.4 at room temperature and large current densities of up to 250 kA/cm2 at 0.5V reverse bias is observed, indicating a very abrupt and high-quality interface. Dislocations and other defects that increase the excess currents appear in the first and the second derivative of the *I-V* characteristics as distinct peaks arising from trap- and phonon-assisted tunneling via the corresponding defect levels. We observe this tunneling mainly in the forward direction and at low reverse bias, but not at higher reverse biases because the band-to-band generation rates are peaked in the InAs, which was also confirmed by modeling. This indicates that most of the peaks are due to dislocations and defects in the immediate vicinity of the interface. To evaluate the potential of this heterostructure material system as Tunnel FET device, additional investigations are performed by increasing the doping concentration in the InAs nanowires to achieve highly doped p^+-Si/n^+-InAs tunnel diodes. Such highly doped diodes serve as a benchmark for the performance of Tunnel FETs.