Impact of Trap-assisted Tunneling and Channel Quantization on InAs/Si Hetero Tunnel FETs

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As a potential candidate for solid-state switches in low-power electronic circuits, the Tunnel Field Effect Transistor (TFET) has attracted the attention of device designers in the past few years. Although simulations have shown that ideal hetero TFETs can achieve sub-thermal sub-threshold swing (SS), the fabrication of a TFET with sufficient on-current and sub-thermal SS over a few decades of drain current remains to be done. Non-idealities in a TFET such as interface traps, band tails, or surface roughness exhibit stronger influence on TFET characteristics in the sub-threshold region. In Ref. [1] we observed that among all of these non-idealities the strongest effect is due to interface traps. On the other hand, simulations have shown that channel quantization severely degrades the on-current [2]. In this work, we analyse experimental transfer characteristics of InAs/Si nanowire TFETs (diameter ≈ 100 nm) and find reasons for the degradation of SS and on-current. We give an estimate for the D_{it} that still would allow a sub-thermal SS.

The experimental InAs/Si vertical nanowire TFETs consisted of p+ doped Si drain ($N_A = 3 \times 10^{19}$cm^{-3}), 100 nm long intrinsic Si channel, and 500 nm long n+ doped InAs ($N_D = 2 \times 10^{18}$cm^{-3}) as shown by the TEM image in Fig. 1(a) [3]. The gate stack was Al$_2$O$_3$/HfO$_2$ with an EOT of 1.3 nm. The critical region of the device was simulated with the semi-classical TCAD simulator S-Device [4] (see. Fig. 1(b)). To account for the effect of channel quantization, a new band-to-band tunneling (BTBT) model based on the path rejection method [2] was implemented using the external Physical Model Interface in S-Device. In this model, a tunnel path is accepted if its energy is above the first sub-band level, but is rejected otherwise (Fig. 2(a)). Trap-assisted tunneling (TAT) at interface traps was modeled with the nonlocal TAT model of Ref. [5]. In its S-Device implementation, the tunnel rate is calculated in WKB approximation with numerical integration over the imaginary dispersion. The work function was set to 4.8 eV.

Generation centers ("traps") at the InAs/oxide interface can capture an electron from the valence band (VB) by a multi-phonon process and emit it to the conduction band (CB) by a tunneling process (Fig. 2(a)). At the InAs/Si interface, traps can mediate a phonon-assisted tunneling process between the Si VB and the InAs CB (Fig. 2(b)). The steady-state trap occupation changes the electrostatics self-consistently. A proper non-local mesh (Fig. 1(b)) has to be constructed to accurately calculate the tunnel rate to and from the traps. Traps at the InAs/Oxide interface were assumed to be uniformly distributed across the band gap. A maximum D_{it} of 1×10^{13}cm^{-2}eV^{-1} was considered in accordance with experimental data [6]. A value of 10 Å^3 was used for the interaction volume of the trap. At the InAs/Si hetero interface, a Gaussian distribution was assumed for the D_{it} with its peak at the VB edge. The peak value was set to 1×10^{13} cm^{-2}eV^{-1}, the FWHM to 55 meV, and the interaction volume to 50 Å^3. These parameters gave a reasonable fit to the experimental data at 300 K and 130 K (Fig. 1(c)).

The comparison of simulated and measured transfer characteristics using the above set-up is shown in Fig. 1(c). Fig. 2(b) presents the effect of channel quantization, showing a severe degradation of the on-current. The good agreement between measured transfer characteristics and simulations including quantization suggests that the quantization effect is indeed present in these devices. The reduction of the on-current is due to the rejection of shorter tunnel paths leading to an increase of the average tunnel length. Fig. 3(c) depicts the impact of TAT on the SS at 300 K. In the sub-threshold region, the drain current is entirely dominated by TAT with negligible contribution from BTBT. The initial branch of the $I_D V_{GS}$-curve is solely degraded by surface SRH generation. With increasing voltage, i.e. sufficient band bending, out-tunneling from trap levels into the CB starts to become effective and provides a "short-cut" to the multi-phonon electron emission step. At 300 K, the contributions of InAs/Si and InAs/oxide TAT to the total sub-threshold drain current are of similar magnitude. However, at 130 K the contribution of InAs/oxide traps becomes negligibly small. This is because of the suppression of multi-phonon excitation of electrons from the VB (Fig. 3(a)). Since both the InAs/oxide and InAs/Si traps contribute to the total current at 300 K, it is necessary to suppress the trap density at both interfaces to achieve a sub-thermal SS as shown in Fig. 4. From these results one can conclude that a sub-thermal SS requires $D_{it} \leq 1 \times 10^{12}$ cm^{-2}eV^{-1} at both interfaces.

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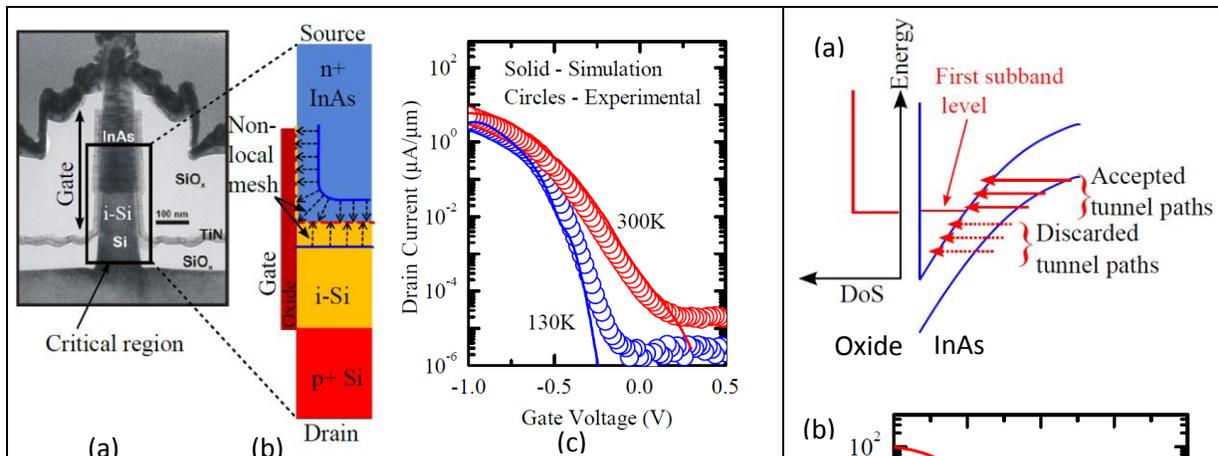
Figure 1: (a) TEM image of the InAs/Si vertical nanowire TFET. **(b)** Radial cross-section of the critical region for TCAD simulation. **(c)** Comparison of experimental and simulated transfer characteristics. Parameters- InAs: E_g=0.36eV, m_e=0.023, m_h=0.026; Silicon: E_g=1.11eV, m_e=0.19, m_h=0.15.
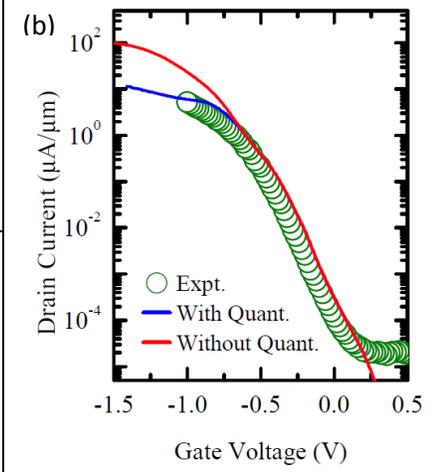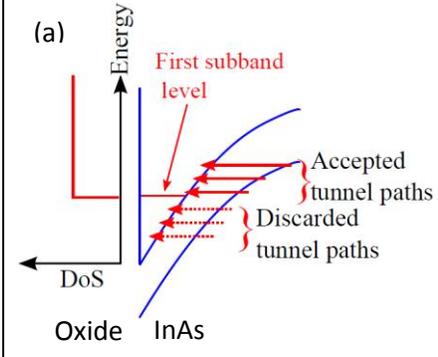
Figure 2:(a) Illustration ofthe path rejection method implemented to model the effect of channel quantization. **(b)**Simulated transfer characteristics with and without considering quantization.
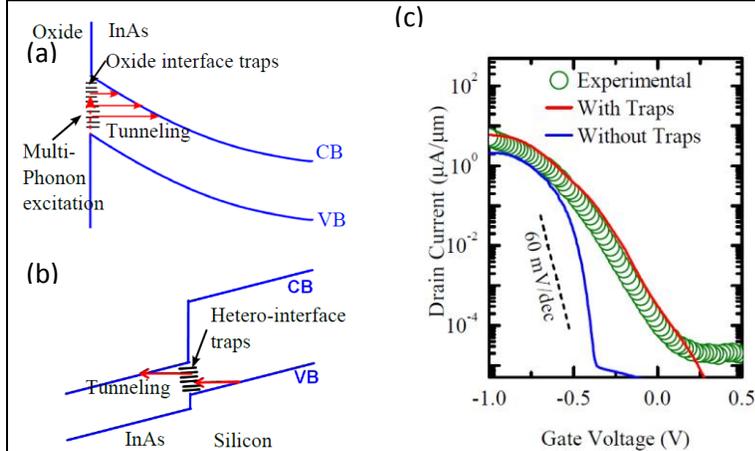
Figure 3: Trap-assisted tunneling at **(a)** oxide/InAs interface and **(b)** InAs/Si interface. **(c)** Simulated ransfer characteristics with and without considering TAT.
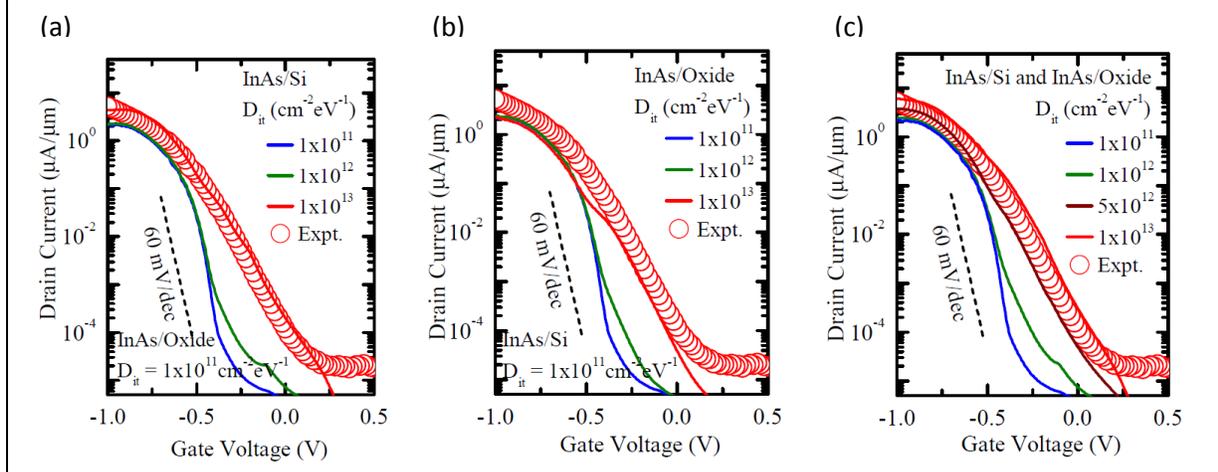
Figure 4: Predictive simulations to analyse the effect of traps at **(a)** InAs/Si interface, **(b)** InAs/oxide interface, and **(c)** both InAs/Si and InAs/Oxide interfaces.