Self-consistent calculations of the ground state and the capacitance of a 3D Si/SiO_2 quantum dot

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Abstract

We perform self-consistent electronic structure calculations in the framework of inhomogeneously and anisotropically scaled local density functional theory of a fully 3D modeled Si/SiO_2 quantum dot. Electrons are laterally confined in the semiconductor/oxide heterojunction by a metallic gate atop of the device. Total charge densities, total free energies, chemical potentials for different numbers of electrons in the dot, and the differential capacitances for various dot sizes are calculated. We observe shell filling effects in the differential capacitance. The *magic*-numbers are governed by the six valley bandstructure of silicon, which leads to four fold degenerated single particle levels in the dot.

Keywords:

Si/SiO_2 quantum dots, capacitance, self-consistent calculations, shell-filling effects

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I. INTRODUCTION

With VLSI/ULSI production technology rapidly approaching the 100 nm range, simulation of quantum effects plays an increasingly important role in nowadays device simulation efforts. For most of the state of the art device simulation tools available today, work is already under way to include the effects of one dimensional quantum confinement in silicon MOSFET channels [1]. Typically, the Schrödinger–Poisson equation is solved and corrections to the charge density, which enters the semiclassical device equations are given. However, with device features below the 100 nm range in silicon and zero dimensional confinement in quantum dots dominating the device operation, this concept is bound to fail to give accurate descriptions.

Throughout the last decade there has been intense research focusing on so called single electron devices. These devices utilize effects as Coulomb blockade and single electron charging, which arise with zero dimensional confinement. Various concepts are pursued which encompass for instance single electron transistors (SET) [2] or two state switching cells in an adiabatic switching paradigm [3]. However, all these concepts suffer from severe limitations. The demands on the purity of materials to avoid random offset charges will be difficult to meet. Phase coherent switching as in the Lent/Porod cells [3] requires virtually defect-free materials over a considerably large spatial extent. Other limitations arise from the very device principles. SETs need to have capacitances in the aF range in order to be operated at room temperature. Therefore, the switching power to achieve reasonable response times will be unsuitably large for large scale integration [4].

A different concept was put forward by IBM researchers J. J. Welser and S. Tiwari [5]. A quantum dot is embedded in the gate oxide of a field effect transistor (FET). The dot is charged with a small but finite number of electrons and changes the threshold voltage of the FET according to the electron number. The device was already shown to have stable room temperature operation by various groups [6], and hence, is a very promising candidate for further silicon based memory devices.

One of the key requirements for device simulation arising from all these concepts is the ability to model zero dimensional confinement. Here, we present a concept and first results of self-consistent calculations of quantum dots in Si/SiO_2 heterojunctions. The model dot is a somewhat artificial device, however, it already incorporates features that will arise with more realistic structures.

II. MODEL QUANTUM DOT

Our model consists of a 90 nm thick undoped Si layer and a 10 nm thick SiO_2 layer. The lateral dimensions of the supercell are 50 nm x 50 nm with a metallic gate on the bottom covering the whole bottom side. Atop of the structure we modeled another metallic square gate, the size of which was varied between 10 nm x 10 nm and 20 nm x 20 nm. The gate voltage is applied between the top and the bottom gate. The size of the top gate defines the lateral size of the quantum dot in the Si/SiO_2 heterojunction.

III. NUMERICAL METHOD

We used a nonuniform tensor product mesh with Dirichlet boundary conditions at the gates and Neumann boundary conditions elsewhere. The operators are discretized using a finite difference approach. We solve the coupled Kohn-Sham (Schrödinger)–Poisson equation system self-consistently including exchange and correlation in the local density approximation. Weak coupling of the dot to the reservoir (leads) is assumed. This constraint imposes vanishing wavefunctions at the boundaries of the supercell. The six valley bandstructure of silicon is taken into account via the kinetic operator

$$T = \frac{1}{2} \sum_{i,j} w_{ij} p_i p_j, \tag{3.1}$$

where $p_j = -i\hbar(\partial/\partial x_j)$. w_{ij} is the reciprocal effective mass tensor. In terms of the transformation matrix a_{ij} from the principal axes of a constant energy ellipsoid we write

$$p_j = \sum_k a_{jk} p'_k \tag{3.2}$$

$$w_{ij} = \sum_k a_{ik} a_{jk} w'_{kk} = w_{ji} \tag{3.3}$$

where $w'_{kk} = 1/m'_k$ are the principal reciprocal effective masses of the semiconductor. Total charge densities, total free energies (F), chemical potentials (μ) for different numbers of electrons in the dot, and the differential capacitances ($C_{\rm d}$)

$$F(N) = -kT \ln \sum_\alpha \exp\left[-F_\alpha/kT\right] \delta_{{\rm N}_\alpha,{\rm N}} \tag{3.4}$$

$$\mu(N) = F(N) - F(N-1) \tag{3.5}$$

$$C_{\rm d}(N) = \frac{q^2}{\mu(N+1) - \mu(N)} \tag{3.6}$$

are calculated. Using these results, we are able to determine the number of electrons in the dot

$$\bar{N} = \frac{\sum_\alpha N_\alpha \exp[-(F_\alpha - \mu N_\alpha)/kT]}{\sum_\alpha \exp[-(F_\alpha - \mu N_\alpha)/kT]} \tag{3.7}$$

as the thermodynamical average over all configurations of occupation numbers $\alpha = \{n_i\}$ Here, μ denotes the chemical potential in the reservoir (leads).

IV. RESULTS

We assumed the gate to be perpendicular to the <100> substrate orientation. Applying the transformations of equations 3.1, 3.2 and 3.3 we obtain three different Hamiltonian operators, which differ in their kinetic parts by different effective masses perpendicular to the interface. However, they contain the same effective potential. The single particle levels are four-fold degenerate. This is in contrast to the spherical total energy surface of GaAs where only spin degeneracy is present. In silicon we have an additional ($-k$,$+k$) degeneracy,

since two equivalent valleys occur in the $-k$ and the $+k$ directions. All calculations are performed for a low temperature of 4.2 K, neglecting intervalley splitting effects.

The self-consistent single particle potential has shown to be quasi parabolic. Consequently, the single particle eigenvalue spectrum exhibits a shell structure similar to the harmonic oscillator spectrum.

Following the arguments of Macucci *et al.* [7] for GaAs systems, we discuss the differential capacitance curves displayed in Figure 1 and Figure 2. When adding electrons to the dot, the free energy increases almost linearly when adding to the same shell, however, the slope increases from shell to shell. Therefore, a minimum in the capacitance occurs, when a shell is filled. In contrast to GaAs, the shell-filling in silicon is governed by the four-fold degenerate single particle levels. Since the confinement in the z-direction, perpendicular to the Si/SiO_2 interface, is stronger than the in-plane confinement due to the top gate, only eigenstates from the Hamiltonian with the longitudinal effective mass in z-direction contribute to the total charge at low electron filling. We observe a minimum of the capacitance at the 4th electron, which is due to the complete filling of the first four-fold degenerate eigenstate. The minimum is more pronounced with the smaller gate (Figure 1) which leads to stronger confinement in the x- and y-directions. The larger gate, and therefore, weaker confinement (Figure 2) leads to an almost linear increase of the capacitance. Shell-filling effects are suppressed, and the dot electrons behave more like a classical circular charge distribution, that increases its capacitance with increasing radius as $C = 8\epsilon_0\epsilon_r r$. The classical value for the capacitance of this dot is 8 aF ($r = 10$nm, $\epsilon_r = 11.8$), which means a slight overestimation of our value of 6 aF ($N = 4$). However, the effective size of the dot underneath the gate is somewhat smaller than the actual gate size.

The simple picture of harmonic oscillator-like shells is not valid when higher electron numbers occur. States from the other Hamiltonians with different symmetries of the wavefunctions then constitute almost arbitrary shells. This is especially evident for a stronger confinement in the x- and y-direction due to a smaller gates. Some shell-filling at the 13th electron is indicated (Figure 1).

V. CONCLUSIONS

We showed that shell-filling effects occur in silicon quantum dots. Due to the larger effective masses, however, these effects are not as dominant as in GaAs dots of the same size. However, since room temperature operation of quantum dot devices requires a considerable level separation compared to the thermal level broadening, overall smaller device features are needed with silicon and shell-filling effects will dominate again.

Magic-numbers are governed by the six valley bandstructure of silicon. Four-fold degenerate single particle levels are occupied. This again is in contrast to GaAs, where only spin degeneracy is present. The three principal directions of the constant energy surface lead to a system of three different Schrödinger equations, which have to be solved self-consistently with respect to the effective single particle potential. The problem of inter-valley coupling has not been tackled in this paper, however, it may play a role. Further investigation in this problem is needed.

REFERENCES

[1] A. Wettstein, A. Schenk, A. Scholze, G. Garreton, and W. Fichtner, "Charge Carrier Quantization Effects in Double-Gated SOI MOSFETs", Proc. of 6th Int. Symposium on ULSI Science and Technology, 1997

[2] R. J. Haug and K. v. Klitzing, "Prospects for research on Quantum Dots and Single-Electron Transistors", FED Journal **6**, 5, 1995

[3] P. D. Tougaw, C. S. Lent, and W. Porod, "Bistable saturation in coupled quantum-dot cells", J. Appl. Phys. **74**, 3558, 1993

[4] J. E. Mooij, "Single Electronics: Status and Prospects", Proc. of Int. Conf. on Solid State Devices and Materials", 1993

[5] L. Geppert, "Solid State: Technology 1997 Analysis and Forecast", IEEE Spectrum, January 1997

[6] L. Guo, E. Leobandung, and S. Y. Chou, "A Silicon Single-Electron Transistor Memory Operating at Room Temperature", Science **275**, 649, 1997

A. Nakajima, T. Futatsugi, K. Kosemura, T. Fukano, and N. Yokoyama, "Room temperature operation of Si single-electron memory with self-aligned floating dot gate" Appl. Phys. Lett. **70**, 1742, 1997

[7] M. Macucci, K. Hess, and G. J. Iafrate, "Electronic energy spectrum and the concept of capacitance in quantum dots", Phys. Rev. B **44**, 17 354, 1993.

FIGURES

FIG. 1. Si/SiO_2 quantum dot: differential capacitance vs number of electrons for a gate size of 10 nm x 10 nm. The gate voltage is 2 V. The inset shows a plot of the number of electrons vs the Fermi level in the leads.

FIG. 2. Si/SiO_2 quantum dot: differential capacitance vs number of electrons for a gate size of 20 nm x 20 nm. The gate voltage is 2 V. The inset shows a plot of the number of electrons vs the Fermi level in the leads.

FIG. 3. Si/SiO_2 quantum dot: addition energy vs number of electrons for a gate size of 20 nm x 20 nm. The inset shows the principal device structure and a plot of the charge density for 12 electrons (cut parallel to the interface).

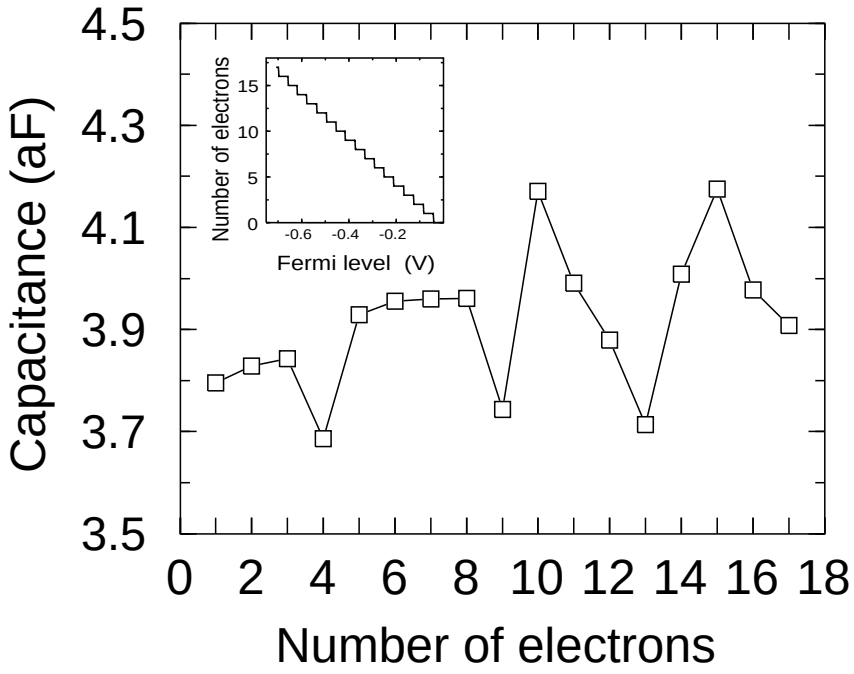
Capacitance (aF)
4.5
4.3
4.1
3.9
3.7
3.5
0
2
4
6
8
10
12
14
16
18
Number of electrons
Number of electrons
15
10
5
0
-0.6
-0.4
-0.2
Fermi level (V)

FIG. 1

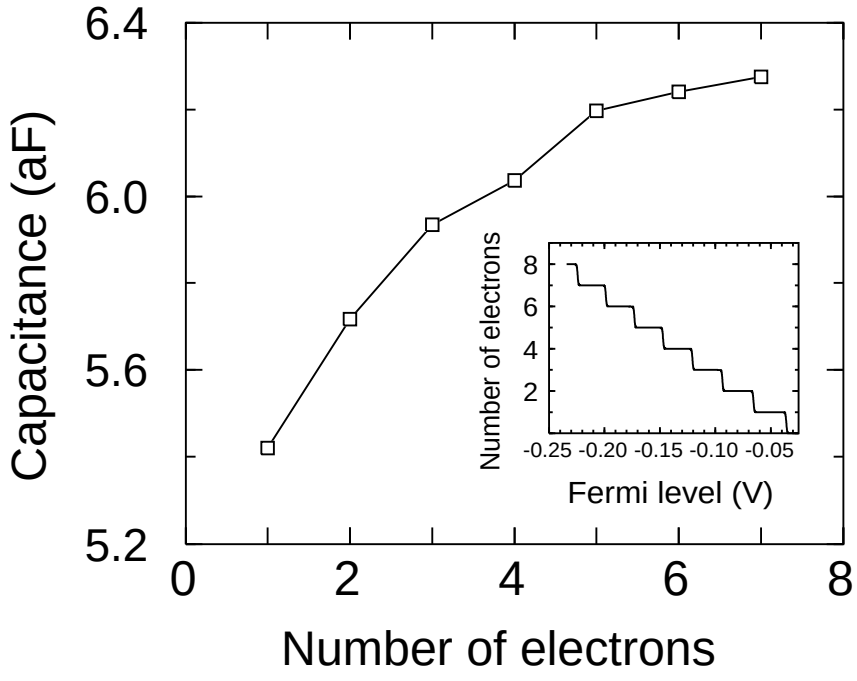
6.4
6.0
5.6
5.2
Capacitance (aF)
0
2
4
6
8
Number of electrons
Number of electrons
8
6
4
2
-0.25 -0.20 -0.15 -0.10 -0.05
Fermi level (V)

FIG. 2

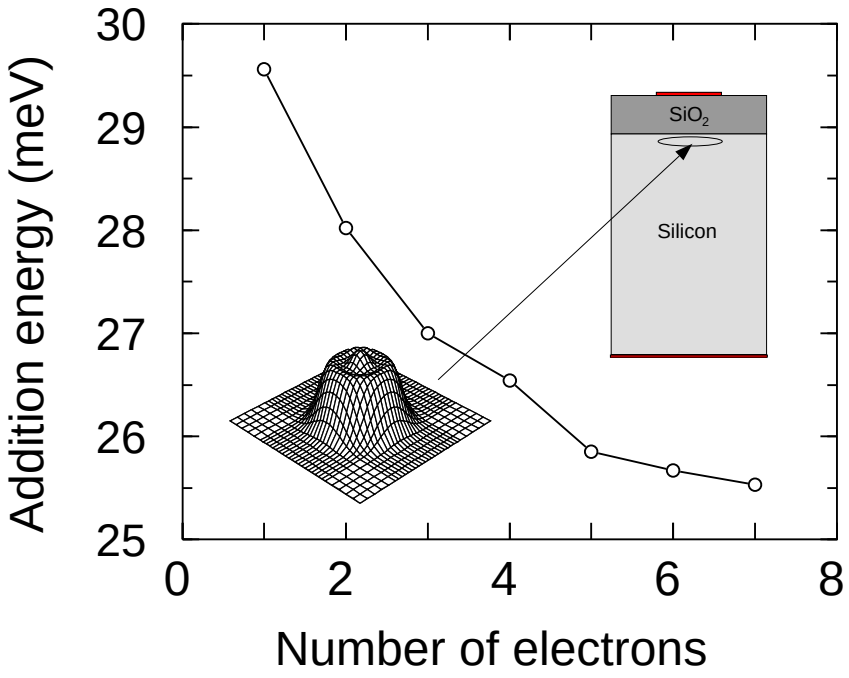
Addition energy (meV)
30
29
28
27
26
25
0
2
4
6
8
Number of electrons
SiO2
Silicon

FIG. 3

BIOGRAPHIES

Andreas Scholze

Andreas Scholze was born in 1969. He received the Dipl. Phys. degree from the University of Jena in 1995. After graduation he joined the Integrated Systems Laboratory of ETH as a research assistant, where he now works with the group of Prof. W. Fichtner in the fields of nanodevice simulation and novel device principles. He is currently working as a visiting research associate at the Beckman Institute for Advanced Science and Technology at the University of Illinois in Urbana-Champaign (UIUC) with the group of Prof. K. Hess.

Andreas Wettstein

Andreas Wettstein was born 1969. He received the Dipl. Phys. degree from the Technical University in Karlsruhe in 1995. Since then he is working with the group of Prof. W. Fichtner at the Integrated Systems Laboratory of ETH. His main research interest is on quantum effects in MOSFET inversion layers and general silicon device physics.

Dr. Andreas Schenk

Andreas Schenk was born in 1957. He received the Dipl. Phys. degree and the Ph.D. from Humboldt University in Berlin (HUB) in 1981 and 1987, respectively. From 1987 till 1991 he was working on various aspects of the physics and simulation of optoelectronic devices. In 1991 he joined the Integrated Systems Laboratory of ETH working as a senior research/teaching assistant, where he qualified to give lectures at university in 1997 for "Physics and Modeling of Microelectronic Devices". His main activities include physics-based models for advanced simulation of submicron silicon devices and their application in the TCAD software released by ISE AG Zurich.

Prof. Wolfgang Fichtner

Wolfgang Fichtner received the Dipl. Ing. degree in physics and the Ph.D. degree in electrical engineering from TU Vienna, Austria, in 1974 and 1978, respectively. From 1979 through 1985, he was member of the technical staff at AT&T Bell Laboratories, Murray Hill, NJ. Since 1985 he is Professor and Head of the Integrated Systems Laboratory at the Swiss Federal Institute of Technology (ETH Zurich). In 1993, he founded ISE Integrated Systems Engineering AG, a company in the field of technology CAD. Wolfgang Fichtner is a Fellow of the IEEE and member of the Swiss National Academy of Engineering.