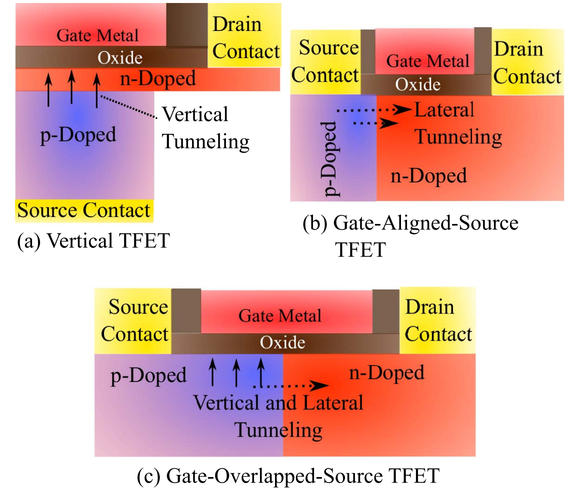
Methods to Enhance the Performance of InGaAs/InP Heterojunction Tunnel FETs

Saurabh Sant and Andreas Schenk

***Abstract*— This paper presents a simulation study of $In_{0.53}Ga_{0.47}As$/InP heterojunction gate-overlapped-source tunnel FETs (GoS-TFETs) with pocket counter-doping. The effect of channel quantization on the line tunneling is considered in the semiclassical simulations using a new model that modifies the band edge in the inversion layer. The small bandgap of the source material $In_{0.53}Ga_{0.47}As$ results in an improved tunnel rate, while the wide bandgap of the channel/drain material InP reduces ambipolar leakage. The simulations show that, for the case of perfectly aligned p-n-junction and heterojunction, the type-I band alignment and the large band offsets delay suppress lateral (point) tunneling relative to vertical (line) tunneling which improves the subthreshold swing (SS). The counter-doped pocket in the source region advances the onset of line tunneling relative to point tunneling which also assists in mitigating the effects of point tunneling. In this way, both large band offset and counter-doped pocket improve the subthreshold behavior of the TFET. Placing the p-n-junction inside the InP region makes the vertical tunneling even more dominant and, thus, reduces the SS. The suggested modifications might be useful to improve the device performance beyond that of the conventional GoS-TFETs.**

***Index Terms*— Heterojunction, InGaAs-InP, line tunneling, pocket counter-doping, point tunneling, tunnel FET (TFET).**



(a) Vertical TFET (b) Gate-Aligned-Source TFET (c) Gate-Overlapped-Source TFET

Fig. 1. (a) In a vertical TFET, a narrow n-doped layer beneath the gate ensures that the tunneling is predominantly vertical. (b) When the orientation of the p-n-junction is normal to the gate and the source is aligned with the gate, the lateral tunneling dominates. A slight misalignment would significantly alter the characteristics of the TFET. (c) When the p-n-junction is not aligned with the gate, both vertical and lateral tunneling take place. This device geometry shows low variability to the placement of the p-n-junction.

I. Introduction

IN A tunnel FET (TFET), the geometric alignment of the p-n-junction with the gate oxide/semiconductor interface has a profound effect on the band-to-band tunnel (BTBT) direction and the tunnel rate. For example, in a device with the p-n-junction parallel to the gate, the tunneling occurs via vertical (the so-called line) BTBT paths [Fig. 1(a)] [1], [2]. On the contrary, when the p-n-junction is perpendicular to the gate oxide/semiconductor interface and the source is perfectly aligned with the gate, the BTBT occurs via tunnel paths parallel to the gate (the so-called point tunneling) [Fig. 1(b)]. If the heavily doped source in the latter case has a large portion overlapped with the gate [Fig. 1(c)], the vertically and laterally oriented tunneling paths exist at the same time [3], [4]. A simulation study has shown that in a homojunction gate-overlapped-source TFET (GoS-TFET), the onset of lateral tunneling occurs earlier than that of the vertical tunneling when the gate voltage is ramped up [5]. Thus, the subthreshold swing (SS) of the device is determined by the lateral tunneling rather than by the vertical tunneling. The transfer characteristics for such a case are schematically shown in Fig. 2(a). As the transfer characteristics (I_D–V_{GS}) originating from lateral tunneling are less steep compared with those determined by vertical tunneling, the SS value of a homojunction GoS-TFETs is high.

Introduction of a heterojunction at the p-n-junction improves the performance of the GoS-TFET in many ways. On one hand, a small-direct-gap material in the source region improves the ON-current. On the other hand, a wide-gap material in the channel and drain region reduces the OFF-state leakage by lowering the Shockley–Read–Hall (SRH) generation and by reducing the tunneling at the channel–drain interface. In addition to that, a favorable band offset at the heterojunction improves the SS by suppressing and delaying the lateral tunneling [5], as shown schematically in Fig. 2(b). Thus, a heterojunction GoS-TFET exhibits superior performance compared with a homojunction GoS-TFET.

The material system intended for the heterojunction GoS-TFETs must satisfy certain criteria. It must consist of a small-direct-gap and a wide-gap material. In order to suppress the lateral tunneling in TFETs, the material system

Manuscript received February 12, 2015; revised September 21, 2015; accepted October 8, 2015. Date of publication October 29, 2015; date of current version April 20, 2016. This work was supported by the European Commission Funding within the European Community's Seventh Framework Programme through the E2SWITCH Project, under Grant 619509. The review of this paper was arranged by Editor R. Huang.

The authors are with the Integrated Systems Laboratory, Department of Information Technology and Electrical Engineering, ETH Zurich, Zürich CH-8092, Switzerland (e-mail: sasant@iis.ee.ethz.ch; schenk@iis.ee.ethz.ch).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2015.2489844

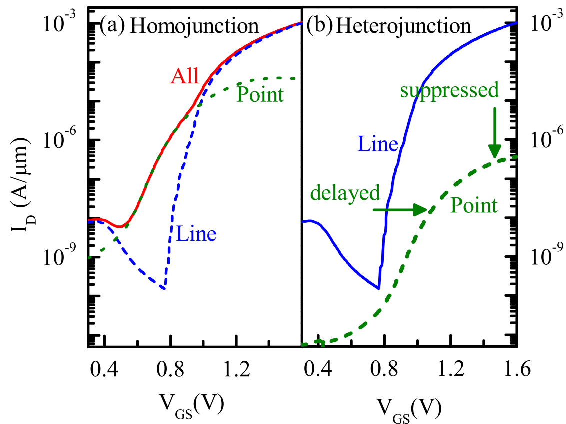


Fig. 2. Schematics showing the contributions of lateral and vertical tunneling in the I_D–V_{GS} plots of (a) homojunction GoS-TFET and (b) heterojunction GoS-TFET.

should exhibit type-I band alignment at the heterojunction. The lattice-matched $In_{0.53}Ga_{0.47}As$/InP heterosystem is well suited for a heterojunction GoS-TFET. The $In_{0.53}Ga_{0.47}As$ alloy is a direct gap semiconductor with a bandgap of 0.74 eV at 300 K, while InP has a relatively large gap of 1.34 eV at room temperature. In addition, the alloy system exhibits type-I band alignment at the interface. As the alloy system is lattice-matched, the defect concentration at the interface is expected to be low, which implies the reduction of trap-assisted tunneling leakage.

In this paper, the $In_{0.53}Ga_{0.47}As$/InP alloy system is analyzed for the application in heterojunction GoS-TFETs. The device geometry, the band structure parameters required to model BTBT, and the simulation setup used in this paper are explained in Section II. Validity of these parameters is confirmed by comparing the simulated transfer characteristics of a vertical TFET with the experimental data. The effects of conduction band (CB) and valence band (VB) offsets, the counter-doped pocket, and the separation between p-n-junction and heterojunction are presented in Section III. The simulation study is concluded in Section IV.

II. Simulation Setup

A double-gate GoS-TFET with $In_{0.53}Ga_{0.47}As$ as a source material and InP as a channel material (See Fig. 5) was simulated using the commercial TCAD simulator Sentaurus-Device [6]. In an n-type TFET, the source is p+ doped and the channel is n− doped, while in a p-type TFET, the source is n+ doped and the channel is p− doped. Only the n-type TFET is analyzed in this paper.

SRH generation was activated in the simulations to consider the thermal leakage in the OFF-state. In order to include the effect of the thermionic band-offset barrier, in which the carriers must overcome when flowing across the heterojunction, the thermionic emission model [6] was also activated. The effect of quantization in the channel region was accommodated semiclassically using a new approach which can model the increase in the effective bandgap due to the subband formation in the channel. The approach is outlined below. The tunneling of electrons between the VB and the CB was modeled by the dynamic nonlocal path BTBT model in Sentaurus-Device. It is based on Kane's two-band theory of BTBT [7] and involves integration over the imaginary dispersion along all possible tunnel paths. The model requires the direct CB and light hole (LH) effective masses, the direct bandgap, and the degeneracy factor to simulate BTBT between the Γ-valley and the LH band. The degeneracy factor is given by $g = 2 \times g_C \times g_V$ which is equal to 2 for BTBT between the Γ-valley and the LH band. As the heavy hole (HH) effective mass is an order of magnitude larger than that of the LH effective mass, the tunneling between HH band and CB is negligible compared with that between LH band and CB. Therefore, the tunneling between the Γ-valley and the HH band is ignored in the simulations.

TABLE I
Values of Band Structure Parameters Required for Kane Model

Parameter	Unit	$In_{0.53}Ga_{0.47}As$ Direct gap	InP Direct gap
E_g	eV	0.74	1.35
ΔE_C	eV	0.27	
ΔE_V	eV	0.34	
$m_C\langle 100\rangle$	m_0	0.043	0.08
$m_{LH}\langle 100\rangle$	m_0	0.052	0.12
Degeneracy (g)	1	2	2
Δ_C	eV	0.0	0.0

The bandgaps of $In_{0.53}Ga_{0.47}As$ and InP were set to 0.74 and 1.34 eV, respectively [8]. The experimental values of the CB offset at the $In_{0.53}Ga_{0.47}As$/InP interface reported in the literature spread over the range from 0.2 to 0.3 eV [9]–[12]. The CB offset of 0.27 eV, which was obtained by density functional theory calculations [12], was used in the simulation. The resulting VB offset is then equal to 0.34 eV. The effective masses of Γ-valley and LH band were taken from [8]. All the band structure parameters required to model the TFET are listed in Table I. The gate work function was set to 4.75 eV.

A. Modeling the Effect of Channel Quantization on BTBT

Increasing the gate bias results in the formation of an inversion layer in the source region underneath the gate. Confinement of the wave functions in the triangular-shaped potential well of the channel results in the formation of subbands. The alignment of the ground-state subband level with the VB edge in the inner marks the onset of line tunneling. A simple method to model the quantization effect within the semiclassical framework has been proposed in [14]. Tunnel paths with an energy above the lowest subband level are accepted, while those with a lower energy are rejected, as shown in Fig. 3. As the implementation of this technique requires substantial effort, a much simpler way was followed here which makes use of the quantum potential correction available in Sentaurus-Device. It is possible to find a quantum potential that mimics the quantization effect by creating an effective bandgap in the inversion layer. In our implementation using the so-called physical model interface, the value

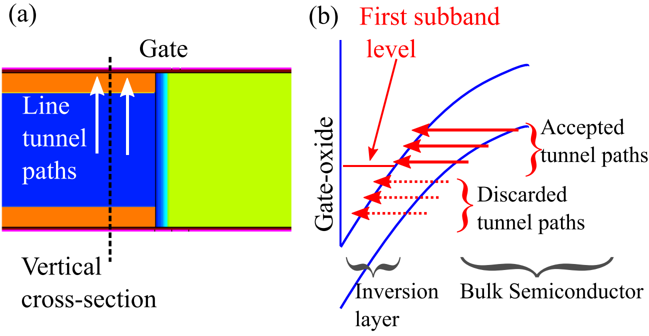


Fig. 3. (a) Representative vertical cross section in the GoS region along with the line tunnel path. (b) Schematic band diagram along the cross section adjacent to the gate oxide.

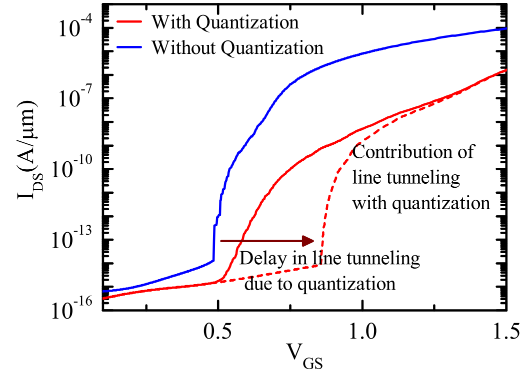


Fig. 4. Transfer characteristics of the GoS TFET of Fig. 5(a) without pocket counter-doping. Blue line: when the channel quantization model is deactivated. Red line: when the model is active. In the absence of channel quantization, line tunneling and point tunneling begin nearly at the same gate bias. When the model is activated, the onset of line tunneling (dotted red line) is delayed due to the inclusion of channel quantization.

of the quantum potential adjacent to the gate dielectric is calculated as

$$E_{\mathrm{QM}} = \begin{cases} \left(\dfrac{q^2 \cdot F^2 \cdot \hbar^2}{2m_e}\right)^{(1/3)} * |a_1| - d_{\mathrm{ox}} \cdot F, & \text{if } E_{\mathrm{QM}} > 0, \\ 0 & \text{otherwise} \end{cases} \quad (1)$$

where a_1 is the first zero of the Airy function, q is the magnitude of the elementary charge, m_e is the electron effective mass, $F(x, y)$ is the local electric field perpendicular to the nearest oxide interface, and d_{ox} is the distance from the oxide interface. The quantum potential is set to zero when its value is negative. The quantum potential is then added to the CB edge, which results in an effective CB edge

$$E_{\mathrm{CB}}^{\mathrm{eff}} = E_{\mathrm{CB}} + E_{\mathrm{QM}}. \quad (2)$$

It is obvious that the almost horizontal effective CB edge is equivalent to an explicit rejection of all energy levels below the lowest subband energy. As the contributions of higher subbands are small because of their weak population, they are neglected. In the case of a constant electric field, this approach is exactly the same as the technique suggested in [14]. In real devices, the vertical component of the electric field is never constant in the channel region. Hence, a moderate variation of the CB edge profile near the gate oxide interface is observed. Nevertheless, the above model can correctly account for the delay in the onset of line tunneling due to channel quantization and is, therefore, employed in the following simulations.

The impact of the above-described model on the transfer characteristics of a GoS-TFET without counter-doped pocket is captured in Fig. 4. When channel quantization model is deactivated, the line and the point tunneling begin at nearly the same gate bias point owing to delay in the point tunneling due to the high CB offset as noted earlier. When the model is active, the line tunneling gets delayed due to channel quantization. The high CB offset is not sufficient to push the onset of point tunneling beyond that of line tunneling which degrades the transfer characteristics of the TFET. Therefore, pocket counter-doping is necessary in addition to the high CB offset as described below and in the subsequent section.

A counter-doped layer under the gate (Fig. 5) creates a p-n-junction parallel to the gate and changes the shape of the

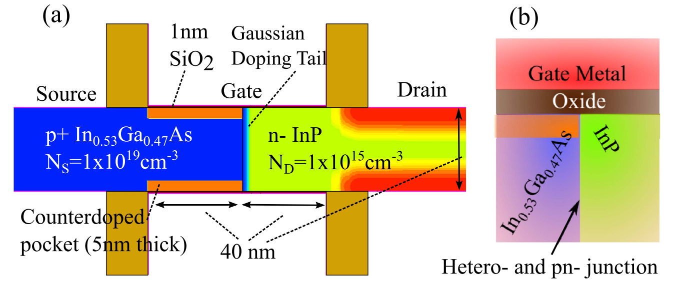


Fig. 5. (a) Device geometry of the n-type GoS-TFET simulated in this paper. (b) Subthreshold characteristics are determined by the alignment of p-n-junction and heterojunction and their placement normal to the gate. The device properties discussed in this paper will be the same for any TFET with such a general arrangement.

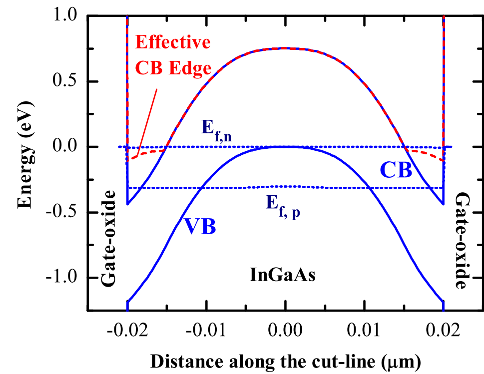


Fig. 6. Band diagram along a vertical cross section [see Fig. 3(a)]. The effective CB edge is obtained by adding electron quantum potential (E_{QM}) to the CB edge. Due to variations in the vertical electric field, the effective CB edge in the channel region is slightly tilted.

band edge. Under strong inversion condition, the CB edge is almost linear in the channel region even in the presence of a counter-doped pocket. As the line tunneling starts at strong inversion, the above model can be applied in the presence of a counter-doped pocket below the gate. Fig. 6 shows the simulated band edge profile at the onset of line tunneling along a vertical cross section of an nTFET with a counter-doped

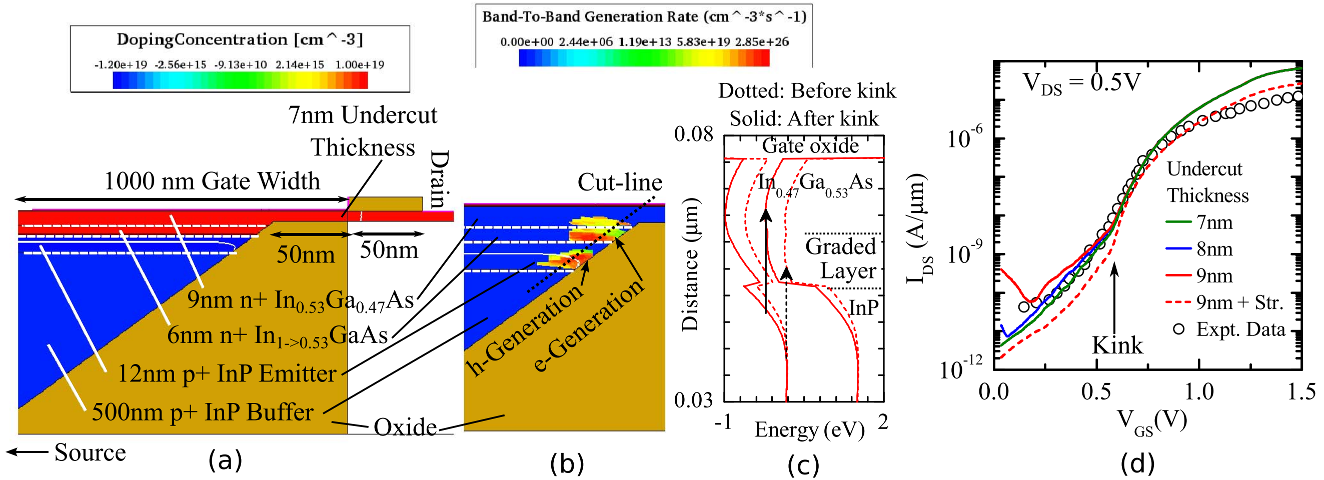


Fig. 7. (Color online) (a) Vertical cross section of the device structure simulated with the simulation setup. (b) Color-mapped electron and hole BTB generation rates at the gate bias at which the kink appears in the I_D–V_{GS} plot. The diagram shows that the electron generation is happening primarily in the graded layer at this bias and is beginning to expand in the $In_{0.53}Ga_{0.47}As$ layer. (c) Band diagram along the cut-line is plotted versus the distance along the cut-line for the gate-bias before the kink and one after the kink. For low bias, InP→$In_{0.53}Ga_{0.47}As$ tunneling is absent due to the lack of direct tunnel path between the VB of InP and the CB of $In_{0.53}Ga_{0.47}As$. At a higher gate bias, a direct InP→$In_{0.53}Ga_{0.47}As$ tunnel path opens and the tunneling begins. (d) A comparison of the simulated and experimental transfer characteristics of the vertical TFET. A good match in the subthreshold region is achieved with the given set of band structure parameters.

pocket of 5-nm thickness. It confirms the applicability of the above model in the presence of a counter-doped pocket below the gate.

In the simulations presented in the following, the quantization model was activated in the source region only, whereas in the channel and drain regions, the classical CB edge was kept unmodified because of the absence of confinement in these regions.

B. Verification of Model Parameters

In order to verify the chosen parameter values, an experimental TFET is simulated first, using the above setup. The calculated transfer characteristics are then compared with the measured ones.

An n-type $In_{0.53}Ga_{0.47}As$/InP heterojunction TFET with mesalike fabrication process was reported in [2]. The geometry of the vertical cross section near the edge of the mesa structure is shown in Fig. 7(a) along with the composition and the thickness of the various layers. The active region in the mesa structure is located near the edge. The device geometry is categorically similar to that given in Fig. 1(a) and supports vertical tunneling. Since the TFET has a 15-nm-thick counter-doped region adjacent to the gate, the effects of channel quantization, as explained earlier, will not arise in this device. Therefore, no channel quantization model was activated. The simulated transfer characteristics are shown in Fig. 7(c) in comparison with the experimental data [2]. The thickness of the $In_{0.53}Ga_{0.47}As$ layer under the gate undercut was not measured and could show a small deviation from the target value. In order to analyze this effect, the simulated characteristics for a few values of the undercut thickness are presented. The simulations agree well with the experimental characteristics in the subthreshold region for the device with an undercut thickness of 7 nm. In the above simulations, the graded $In_{1\rightarrow0.53}GaAs$ layer was assumed to be fully relaxed. The strain in the graded layer would change the bandgap of the material, which in turn would affect the transfer characteristics. The simulated transfer characteristics of the device for the case of a strained graded layer (i.e., without relaxation) are also shown in Fig. 7 for comparison. The band structure parameters of the strained layer were obtained by empirical pseudopotential calculations [13].

A kink is observed in the simulated transfer characteristics of the device. The simulations reveal that the kink is a result of the expansion of the electron generation region from the $In_{1.0\rightarrow0.53}GaAs$ graded layer to the $In_{0.53}Ga_{0.47}As$ layer. When the BTBT path starting in InP ends in the graded layer, it is at least 9-nm away from the gate, and the SS degrades due to reduced gate control. The SS improves as this point moves closer to the oxide interface with the increasing gate voltage.

The difference between the simulated and experimental characteristics at high gate voltages may be attributed to the omission of the doping dependence of the mobility and the contact resistance from the simulation setup. In the subthreshold regime, the drain current is primarily determined by BTBT. At high drain current levels, the voltage drop at the contacts would reduce the effective V_{DS} across the active region leading to a lower drain current than predicted by the simulations.

It can be concluded that the simulation setup, the BTBT model, and the parameter values listed in Table I provide a good match with the experimental data in the subthreshold range. Since the device characteristics in the subthreshold region of operation are of main interest in this paper, the simulation setup can be used to analyze $In_{0.53}Ga_{0.47}As$/InP heterojunction TFETs. It may be noted that the values of the BTBT model parameters were obtained from measured band structure parameters. No fitting was performed with the experimental transfer characteristics.

III. Simulation Results and Discussion

Having confidence in the validity of the parameters, a simulation-based analysis of the n-type GoS-TFET (Fig. 5) is performed to study the influence of source doping, band offsets, and misalignment between p-n-junction and heterojunction on its performance.

The operation of the n-type GoS-TFET is explained in detail in [5] and [15]. As the gate voltage increases, an inversion layer begins to form at the source/gate oxide interface. The lightly n-doped region overlapped with the gate does not form an inversion layer at high V_{GS}. At sufficiently high gate bias, electrons tunnel from the inner source region (with bulk properties) to the inversion layer, which marks the onset of vertical tunneling. Increasing the source doping reduces the width of this tunnel barrier, and thus increasing the tunnel rate and the ON-current. In this way, the SS becomes smaller with higher source doping. However, above a certain value, the effect of barrier thinning saturates and other effects, such as channel quantization and reduced gate control, due to stronger screening begin to surface which in turn degrade the SS. As in [15], the optimum value of the source doping was found to be 8×10^{18} cm^{-3}. This value was used for the simulations reported in the subsequent sections.

A. Effect of Counter-Doped Pocket

In a GoS-TFET, the onset of line tunneling occurs after (i.e., at a higher gate voltage) that of point tunneling. As a result, the SS of the TFET degrades [5]. The SS can be improved by advancing the onset of line tunneling before (i.e., at a lower gate voltage) that of point tunneling. This can be achieved by a pocket counter-doping below the fraction of the gate which overlaps with the source [16], [17]. Pocket counter-doping creates a p-n-junction parallel to the gate in the GoS region. The depletion layer is formed and band bending occurs even at zero bias. Therefore, a smaller gate bias is sufficient to start line tunneling. In this way, the pocket counter-doping advances the line tunneling relative to the point tunneling. This effect is shown in Fig. 8. As shown in Fig. 8, the onset of line tunneling moves to a smaller gate bias with the increasing pocket thickness (for a fixed pocket doping), whereas the onset of point tunneling remains fixed at a certain gate bias.

However, a thick counter-doped pocket results in a shift of the p-n-junction away from the gate, which reduces the gate control over line tunneling, and the SS degrades. Therefore, the pocket must be thin. As observed in Fig. 8, the line tunneling begins before point tunneling for a pocket thickness of 5 nm. In other words, 5 nm is the minimum pocket thickness required to let the line tunneling start before the point tunneling. Therefore, the pocket thickness is fixed at 5 nm in the subsequent simulations. It may be noted that for the above simulations, the CB offset was set to 0.27 eV, as mentioned earlier.

B. Effect of the Band Offset

When the heterojunction in a TFET coincides with the p-n-junction, the CB offset at the interface is capable of suppressing and delaying the lateral tunneling, as shown in Fig. 2. This results in an improved SS since vertical tunneling becomes dominant. The simulated I_D–V_{GS} characteristics in Fig. 9 demonstrate this effect. These plots were obtained by changing the electron affinity of InP artificially to generate the desired CB offsets. At low gate bias, a bulge is observed in the I_D–V_{GS} curve for zero band offset due to the early onset of point tunneling. This feature starts to disappear with the increasing CB offset and completely vanishes for $\Delta E_C > 0.32$ eV. The transfer characteristics for $\Delta E_C = 0.24$ eV, marked in bold, seem to be optimal.

Introduction of the heterojunction at the p-n-junction results in a steplike band edge profile at the p-n-junction. It may be argued that this steplike profile would cause blockade of electrons drifting from the inversion layer toward the drain contact when they cross the heterointerface [see Fig. 10(a)]. The CB offset would act as a steplike potential barrier with height ΔE_C which would force the electrons to cross the interface by thermionic emission and thereby reduce the drain current. However, this feature is not observed in the transfer characteristics even for the large values of the band offset (see Fig. 9). Instead, the transfer characteristics of the TFET for different values of ΔE_C converge to a single curve. This is the result of channel quantization, which is activated in

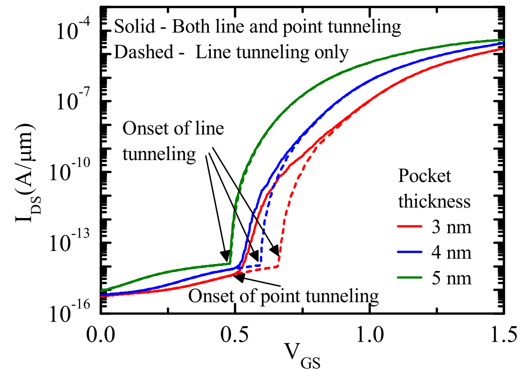


Fig. 8. (Color online) Transfer characteristics of an nTFET for different values of counter-doped pocket thickness. Solid lines: I_D–V_{GS} plots which include the contribution of both line and point tunneling. Dashed lines: contribution of only line tunneling.

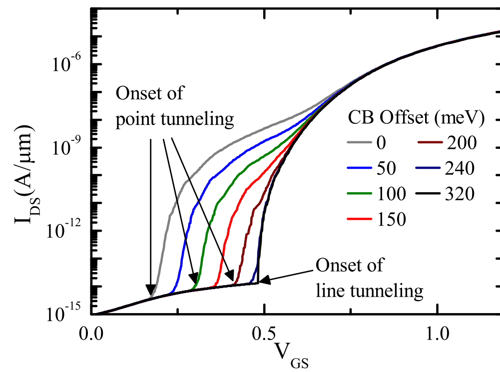
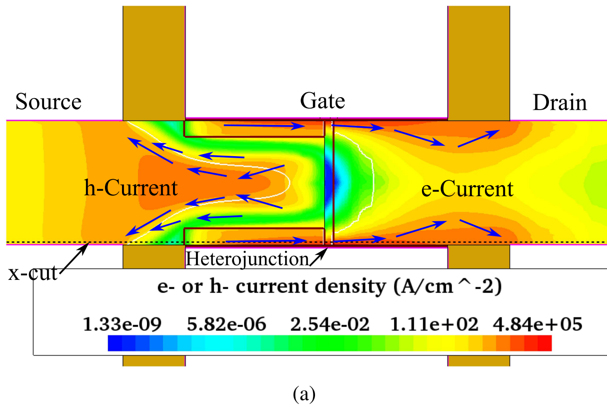
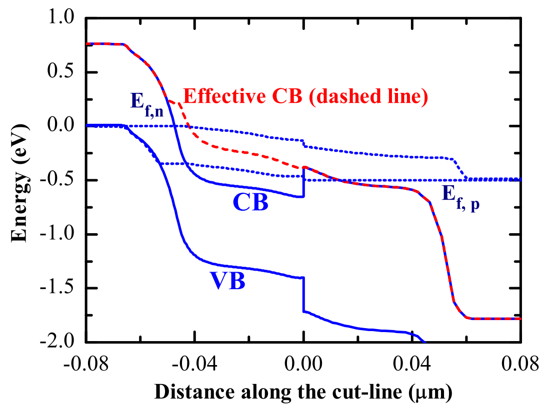


Fig. 9. (Color online) Transfer characteristics for different values of the CB offset between $In_{0.53}Ga_{0.47}As$ and InP. As the exact values of the band offsets are not established yet, this plot shows how the characteristics would change with the changing CB offset. The average SS degrades due to the early onset of lateral tunneling.



(a)



(b)

Fig. 10. (a) Color-mapped plot of the electron and hole current densities. Blue arrows: predominant flow lines of electrons and holes. A black dotted line running horizontally adjacent to the lower gate is the cut-line 1-nm away from the gate oxide along which the band diagram in (b) is plotted. (b) Extracted band diagram at the onset of line tunneling. Effective CB edge in the band diagram does not exhibit any steplike behavior despite the high band offset at the heterointerface.

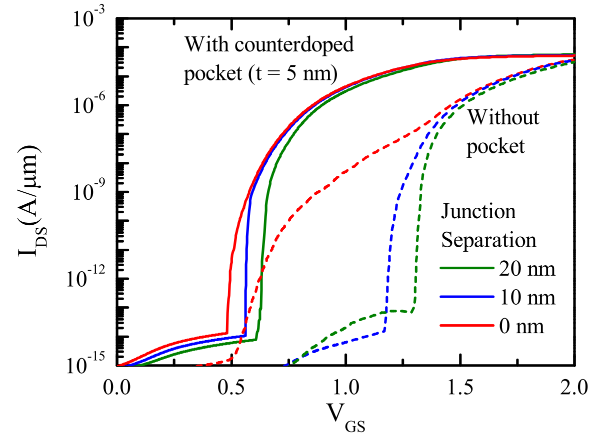


Fig. 11. (Color online) Transfer characteristics of the TFET with the p-n-junction shifted into the wide-gap material (InP). Solid lines: characteristics of the device with pocket counter-doping. Dashed lines: characteristics of the device without pocket counter-doping. It is observed that shifting the p-n-junction improves the SS significantly. Dashed curves: SS even improves without pocket counter-doping. However, the onset voltage increases drastically.

the simulation. A band edge profile along the channel adjacent to the gate oxide is shown in Fig. 10(b). Fig. 10(b) shows that the effective CB edge, which includes the effect of channel quantization, does not exhibit a steplike profile at the heterointerface. Thus, the electrons traveling across the heterointerface are not hampered by a thermionic barrier.

In short, the band offsets delay the point tunneling relative to the line tunneling and suppress it, whereas the counter-doped pocket advances the line tunneling relative to the point tunneling. Thus, both the band offset and pocket counter-doping have the same effect on the TFET characteristics. This can be utilized to obtain an optimum value of the counter-doped pocket thickness for a given band offset such that the line tunneling begins prior to the point tunneling as the gate bias is ramped up.

C. Separation Between p-n-Junction and Heterojunction

Both the p-n-junction and the heterojunction were placed at the same position in the GoS TFET in the simulations until now. However, the p-n-junction can be displaced from the heterojunction and the distance between them can be used as an additional variable to tune the performance of the TFET. The impact of this distance on the TFET characteristics is explained below.

The variation of the transfer characteristics due to the separation of p-n-junction and heterojunction is presented in Fig. 11. It is observed that the I_D–V_{GS} characteristics are steeper when the p-n-junction is located in the wide-gap material (InP). The SS degrades as the p-n-junction moves toward the heterointerface (i.e., when the separation becomes zero). The case where the p-n-junction is located inside the narrow-gap material (InGaAs) is not considered, as this only further degrades the transfer characteristics.

The above-described effect is due to the suppression of point tunneling when the p-n-junction is located in the wide-gap material. This can be observed in colored contours of the BTB generation rates in the GoS-TFET (Fig. 12). When the p-n-junction is in the wide-gap material (InP), the onset of point tunneling at the p-n-junction is significantly delayed due to the large bandgap. Point tunneling at the heterointerface is prevented because of insufficient band bending in the horizontal direction in the absence of the p-n-junction. Thus, only the vertical tunneling takes place inside InGaAs, as shown in Fig. 12(a), which results in a very steep onset. When the p-n-junction and heterojunction coincide, the large CB offset (0.27 eV in this case) suppresses the point tunneling. Some lateral tunneling occurs nonetheless as a result of strong band bending in the horizontal direction due to the p-n-junction, as shown in Fig. 12(b). This tunneling along point tunnel paths degrades the SS. In this way, positioning the p-n-junction inside the wide-gap material significantly enhances the vertical tunneling and improves the SS in the case of an $In_{0.53}Ga_{0.47}As$/InP hetero-TFET.

As observed in Fig. 11, the effect of the displaced p-n-junction is so strong that the transfer characteristics of the TFET without a counter-doped pocket become as steep as those with pocket and aligned junctions. Thus, a proper separation of the junctions eliminates the necessity of a counter-doped pocket. However, in the absence of

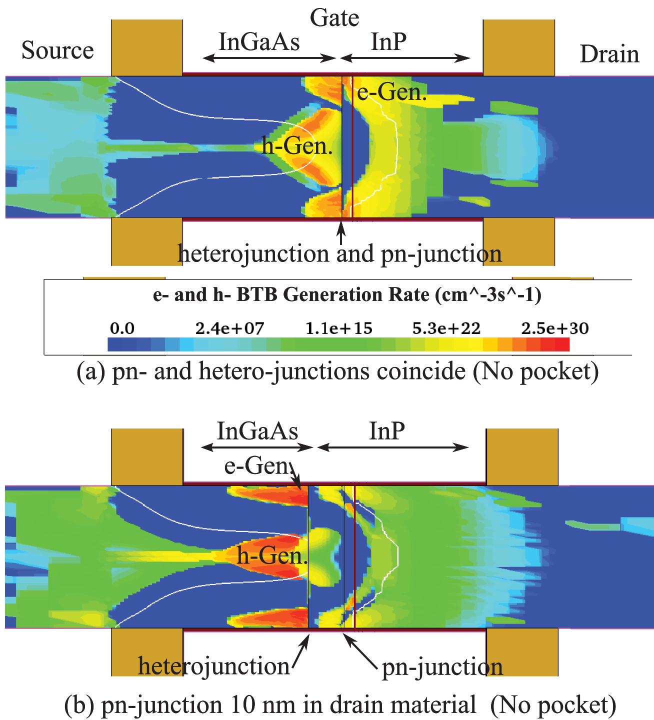


Fig. 12. Color-mapped diagram showing the electron and hole generation rates in the TFET with p-n-junction and heterojunction separated by a distance of (a) 0 and (b) 10 nm. The CB offset was set to 0.27 eV. The TFET was simulated without a counter-doped pocket.

a counter-doped pocket, the onset voltage is shifted by ~1 V. This huge shift would have to be compensated by gate material engineering in order to maintain a sufficient ON-current.

IV. Conclusion

The applicability of the $In_{0.53}Ga_{0.47}As$/InP heterosystem for an n-type GoS TFET was analyzed. A new, convenient model to consider the effect of channel quantization on the line tunneling in a semiclassical framework was presented. The set of parameters used to model the BTBT in such a system enabled to reproduce the transfer characteristics of a measured vertical TFET in the subthreshold regime. These parameters were used to simulate the $In_{0.53}Ga_{0.47}As$/InP double-gate GoS-TFET with p-n-junction and heterojunction at the same location. It was shown that the CB offset at the heterointerface suppresses the lateral tunneling which results in a smaller SS. In addition, the pocket counter-doping advances the onset of line tunneling and, thus, has the same effect as that of a large band offset. Contrary to intuition, a step in the CB edge arising from the CB offset does not obstruct the electron current toward the drain. This is a result of subband formation due to the channel quantization, which compensates for the step in the CB edge.

The separation of p-n-junction and heterojunction can be used as an alternate mean to improve the performance of a TFET. The simulations have shown that for a GoS-TFET, placing the p-n-junction in the wide-gap material, such as InP, would decrease the SS by suppressing the point tunneling, even in the absence of a counter-doped pocket. The placement of the p-n-junction in the small-gap material ($In_{0.53}Ga_{0.47}As$) degrades the SS. In this way, the type-I band alignment at the InGaAs/InP interface with a large CB/VB offset and the p-n-junction in InP can suppress the point tunneling in a $In_{0.53}Ga_{0.47}As$/InP GoS-TFET, which would consequently improve the SS. This could also suppress the trap-assisted tunneling caused by traps at the $In_{0.53}Ga_{0.47}As$/InP interface.

References

[1] R. Asra, M. Shrivastava, K. V. R. M. Murali, R. K. Pandey, H. Gossner, and V. R. Rao, "A tunnel fet for V_{DD} scaling below 0.6 V with a CMOS-comparable performance," *IEEE Trans. Electron Devices*, vol. 58, no. 7, pp. 1855–1863, Jul. 2011.

[2] G. Zhou *et al.*, "InGaAs/InP tunnel FETs with a subthreshold swing of 93 mV/dec and I_{ON}/I_{OFF} ratio near 10^6," *IEEE Electron Device Lett.*, vol. 33, no. 6, pp. 782–784, Jun. 2012.

[3] G. Dewey *et al.*, "Fabrication, characterization, and physics of III–V heterojunction tunneling field effect transistors (H-TFET) for steep sub-threshold swing," in *Proc. IEEE Int. Electron Devices Meeting*, Dec. 2011, pp. 33.6.1–33.6.4.

[4] S. Mookerjea, D. Mohata, T. Mayer, V. Narayanan, and S. Datta, "Temperature-dependent $I - V$ characteristics of a vertical $In_{0.53}Ga_{0.47}As$ tunnel FET," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 564–566, Jun. 2010.

[5] S. Sant and A. Schenk, "Band-offset engineering for GeSn-SiGeSn hetero tunnel FETs and the role of strain," *IEEE J. Electron Devices Soc.*, vol. 3, no. 3, pp. 164–175, May 2015.

[6] *Sentaurus Device User Guide, Version 2013.03*, Synopsys, Inc., Mountain View, CA, USA, 2013.

[7] E. O. Kane, "Theory of tunneling," *J. Appl. Phys.*, vol. 32, no. 1, pp. 83–91, 1961.

[8] I. Vurgaftman, J. R. Meyer, and L. R. Ram-Mohan, "Band parameters for III–V compound semiconductors and their alloys," *J. Appl. Phys.*, vol. 89, no. 11, pp. 5815–5875, 2001.

[9] P. Philippe, P. Poulain, K. Kazmierski, and B. de Cremoux, "Dark-current and capacitance analysis of InGaAs/InP photodiodes grown by metalorganic chemical vapor deposition," *J. Appl. Phys.*, vol. 59, no. 5, pp. 1771–1773, 1986.

[10] J. R. Waldrop, E. A. Kraut, C. W. Farley, and R. W. Grant, "Measurement of InP/$In_0.53Ga_0.47As$ and $In_0.53Ga_0.47As/In_0.52Al_0.48As$ heterojunction band offsets by X-ray photoemission spectroscopy," *J. Appl. Phys.*, vol. 69, no. 1, pp. 372–378, 1991.

[11] K. Uchida, H. Yamato, Y. Tomioka, A. Koizumi, and S. Nozaki, "Characterization of MOVPE-grown p-InGaAs/n-InP interfaces," *J. Crystal Growth*, vol. 311, no. 16, pp. 4011–4015, 2009.

[12] A. Wadehra, J. W. Nicklas, and J. W. Wilkins, "Band offsets of semiconductor heterostructures: A hybrid density functional study," *Appl. Phys. Lett.*, vol. 97, no. 9, pp. 092119-1–092119-3, 2010.

[13] *Sentaurus Device Monte Carlo User Guide, Version 2013.03*, Synopsys, Inc., Mountain View, CA, USA, 2013.

[14] W. G. Vandenberghe, B. Soree, W. Magnus, G. Groeseneken, A. S. Verhulst, and M. V. Fischetti, "Field induced quantum confinement in indirect semiconductors: Quantum mechanical and modified semiclassical model," in *Proc. Int. Conf. SISPAD*, Sep. 2011, pp. 271–274.

[15] A. Schenk, S. Sant, K. Moselund, and H. Riel, "Comparative simulation study of InAs/Si and all-III–V hetero tunnel FETs," *Trans. Electrochem. Soc.*, vol. 66, no. 5, pp. 157–169, 2015.

[16] S. Agarwal, G. Klimeck, and M. Luisier, "Leakage-reduction design concepts for low-power vertical tunneling field-effect transistors," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 621–623, Jun. 2010.

[17] K. Ganapathi, Y. Yoon, and S. Salahuddin, "Analysis of InAs vertical and lateral band-to-band tunneling transistors: Leveraging vertical tunneling for improved performance," *Appl. Phys. Lett.*, vol. 97, no. 3, p. 033504, 2010.

Authors' photographs and biographies not available at the time of publication.