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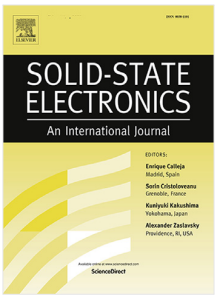

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A Generalizable TCAD Framework for Silicon FinFET Spin Qubit Devices with Electrical Control

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ABSTRACT

We present a TCAD-based simulation framework established for quantum dot spin qubits in a silicon FinFET platform with all-electrical control of the spin state. The framework works down to 1 K and consists of a two-step simulation chain, from definition of the quantum dot confinement potential with DC bias voltages, to calculation of microwave response electric field at qubit locations using small-signal AC analysis. An average field polarization vector at each quantum dot is extracted via a post-processing step. We demonstrate functionality of this approach by simulation of a recently reported two-qubit device in the form of a 5-gate silicon FinFET. The impact of the number of holes in each quantum dot on the MW response E-field polarization direction is further investigated for this device. The framework is easily generalizable to study future multi-qubit large-scale systems.

1. Introduction

Scalability is vital for building useful quantum computers with quantum error correction, but a tough task with respect to actual physical implementation. One promising platform to overcome this challenge is quantum dot (QD) spin qubits embedded in multi-gate silicon FinFETs [1, 2]. Recently, hole spin qubits hosted by double QDs in a 5-gate silicon FinFET that can operate above 4 K have been reported [3]. The device fabrication is compatible with standard CMOS technology [4], and qubit manipulation is realized by electric dipole spin resonance (EDSR) with microwave (MW) electrical signals applied to a single gate electrode. This makes it a good candidate towards large-scale integration of spin qubit devices. To scale up the system in the near future, a simulation-aided analysis for the design of all-electrical qubit control is highly desirable. For this purpose, we developed a TCAD-based framework that can perform DC and AC simulations down to 1 K. The MW response electric field (E-field) polarization vector averaged over each QD is extracted in post-processing steps. Gate cross-talk is also included in these AC simulations by a first-order capacitive coupling model.

We illustrate the simulation framework by taking the reported two-qubit device [3] as an example, while the generalization to multi-qubit devices is straightforward. The simulated device structure is shown in Fig. 1. In the following, we first introduce the simulation workflow and explain the AC method for MW E-field polarization vector calculation, including the gate cross-talk estimation model. Then, we employ an example of single-hole QDs to show how AC simulation and post-processing work. Afterwards, we discuss the impact of the number of holes in the QDs on the averaged response E-field polarization vector.

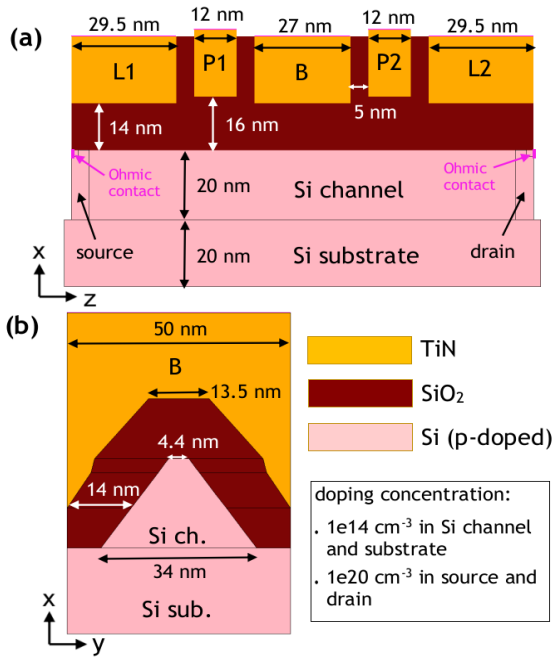

Figure 1: Sketch of simulated 5-gate Si FinFET. (a)/(b) side/cross section view along/vertical to fin direction. MW signal (5 GHz, 12 mV amplitude) for spin qubit control is applied on gate P1.

2. Simulation Methodology

The entire simulation chain includes four steps, as shown in Fig. 2. To calculate the response E-field polarization vectors, first, we run a quasi-stationary DC simulation to generate QDs with a specific number of holes. Quantum confinement is modeled with the density-gradient method [5, 6], where a potential-like quantity Γ_p is derived solving an additional equation. The hole density is then obtained

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from

$$p(\mathbf{r}) = N_{\mathrm{v}} F_{1/2}\Big[\beta\big(E_{\mathrm{v}}(\mathbf{r}) + \Gamma_{\mathrm{p}}(\mathbf{r}) - E_{\mathrm{f,p}}\big)\Big] \tag{1}$$

with $\beta = 1/k_{\mathrm{B}}T$ and $E_{\mathrm{f,p}} = 0$. Obviously, Eq. (1) is based on local thermodynamic equilibrium and Fermi-Dirac statistics, which breaks down in the SET regime of the transistor. Options like Gibbs statistics are not available in S-Device. As a consequence, the dot charge changes continuously with gate voltage, and no tunnel barriers can be generated in the limit $T \to 0$ K. Transverse confinement is in good agreement with 2D k·p Schrödinger-Poisson reference calculations [5], but longitudinal confinement effects cannot be easily calibrated. Therefore, the exact density overlap between the dots remains vague. However, this is not expected to impact the AC analysis significantly.

In the second step, AC simulations are performed using the electrical small-signal analysis method [5]. This method is valid for qubit device simulation because the MW signal amplitude is usually much smaller than the applied DC bias and the device size (few hundreds of nanometers) is much smaller than the MW wavelength (centimetre range).

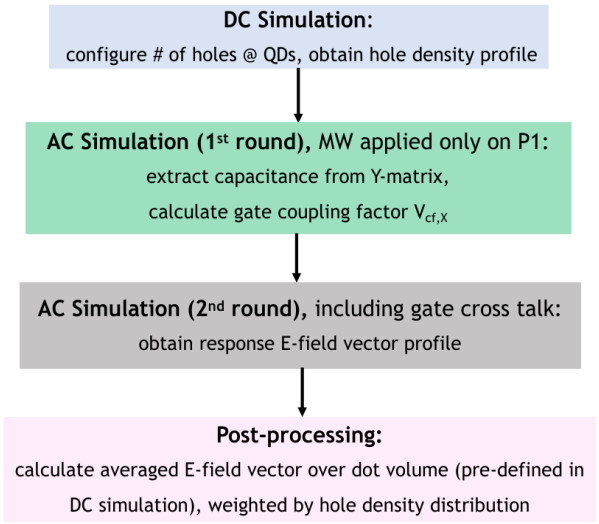
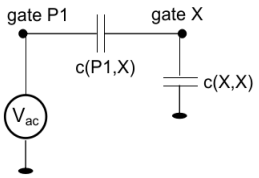


Figure 2: Simulation workflow for calculation of MW response E-field polarization vector.

To take the cross talk between gates into account, we introduce a simplified capacitive coupling model based on the first-order approximation. This is achieved by running two AC simulation rounds. A first round is performed with the AC signal applied on gate P1 only to extract the Y-matrix of the device. The obtained capacitance elements are then used to calculate a capacitive coupling factor $V_{\mathrm{cf,X}}$ between P1 and any other gate X, based on a voltage divider circuit (see Fig. 3 (a)). Then, a second-round simulation is performed with AC signals also applied to other gates, where their AC voltage amplitudes depend on their respective coupling factors $V_{\mathrm{cf,X}}$. Fig. 3 (b) shows the results of the coupling factors in case of one hole in each QD. The coupling is strong only for gates L1 and B that are close to P1.

(a)



$$V_{ac,X} = V_{ac} * \frac{c(P1,X)}{c(P1,X)+c(X,X)}$$

- capacitive coupling factor

$$V_{cf,X} = V_{ac,X} / V_{ac}$$

(b) Gate coupling factor calculation for 1/1 hole at QD 1/2

gate X	cross cap. c(P1,X) [aF]	self cap. c(X,X) [aF]	$V_{cf,X}$ [1]
L1	11.238	14.689	**0.433**
B	11.379	25.212	**0.311**
P2	0.110	24.014	0.00456
L2	0.148	14.415	0.0102

Figure 3: (a) Simplified 1st-order capacitive coupling circuit model for gate cross talk calculation. (b) Calculated voltage coupling factor for the case of two single-hole QDs.

The desired AC-response E-field polarization vector is obtained based on the S-Device default output $\mathfrak{I}(J_D)$ after the second AC run including the gate cross talk. This extraction relies on the following relations:

$$E = -\nabla\varphi \tag{2}$$

$$J_D = -i\omega\epsilon\nabla\varphi \tag{3}$$

$$\mathfrak{R}(E) = \mathfrak{I}(J_D)/\omega\epsilon \tag{4}$$

According to Eq. (4), the imaginary part of the displacement current response $\mathfrak{I}(J_D)$ (default output) is representative for the real E-field response $\mathfrak{R}(E)$. Their magnitudes differ only by a scaling factor, whereas the vector directions are exactly the same. This one-to-one correspondence facilitates the subsequent calculation of a normalized field polarization vector averaged over the QD for each qubit by a post-processing step (see the results in Sec. 3).

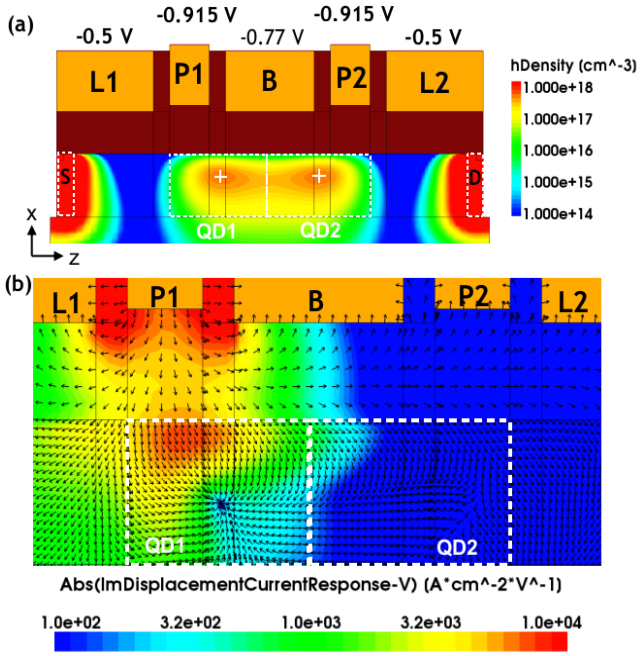
3. Simulation Results

In this section, we first present results obtained for a (1,1) charge configuration with one hole in each QD, to demonstrate the simulation workflow. Then we study the influence of an increasing hole number on the field polarization, as this parameter can be hard to determine experimentally.

3.1. AC-response field for single-hole QDs

Fig. 4 (a) shows the hole density profile in presence of two single-hole QDs, obtained from the DC simulation. The QD hole number is calculated by integrating the hole density over a defined quantum dot volume (indicated by white dashed lines). Then, after running two-round AC simulations, the field response vector profile is calculated (see

Fig. 4 (b)). Two singularities show up in the AC-response E-field vector distribution due to the low response at the dot centers ((labeled by white crosses in Fig. 4 (a)). In order to assign a single field polarization vector to the three-dimensional distribution, we introduce a normalized field vector averaged over the dot volume weighted by the DC hole density. It is calculated in post-processing by multiplying the hole density with each of the x/y/z-components of the field vector, then integrating the resulting quantity over the dot volume, and finally dividing the integrals by their root sum square. In this way the DC hole density acts as a weighting factor in the field extraction procedure.



(c) normalized averaged E-field polarizarion vectors (1/1 hole case)

	E_x	E_y	E_z
QD1	**-0.864**	-1.16e-3	0.503
QD2	**-0.988**	-2.37e-3	0.157

Figure 4: (a) DC hole density profile along the fin direction. White dashed lines (cross labels) indicate the QD volume used for integration to obtain the number of holes (dot centers). (b) $\Im(J_D)$ response profile, taken at V_{ac} = -12 mV. The arrows exactly represent the field polarization. (c) Calculated normalized x/y/z-components of the averaged response field polarization vector at each QD.

The calculated normalized average field polarization vectors for the QDs in a (1,1) charge configuration are shown in Fig. 4 (c). As we see, the E-field vectors at both QDs are mostly polarized along the -x-direction. This observation is related to the specific location of the QD centers. For QD1, as its center is shifted towards gate B, a hotspot of the response field amplitude occurs directly in the dot region under gate P1 (see Fig. 4 (b)). This results in a larger contribution pointing along the -x axis when averaging the field vectors over the QD volume. For QD2, there is no clear hotspot, but the vertical (-x-direction) components of the field vectors in the upper part of the QD contribute more.

3.2. Impact of number of holes at QDs

To tune the hole number simultaneously at both QDs, we choose to adjust the DC bias on the plunger gates P1 and P2, while keeping the bias values on all the other gates unchanged. The required plunger gate voltages for inducing hole configurations from (1,1) to (5,5) in (QD1,QD2) are shown in Fig. 5 (a). It turns out that the relation between

(a)

# of holes @ QD1/2	1/1	2/2	3/3	4/4	5/5
V_{P1} [V]	-0.915	-1.024	-1.123	-1.222	-1.318
V_{P2} [V]	-0.915	-1.024	-1.123	-1.222	-1.318

(b)

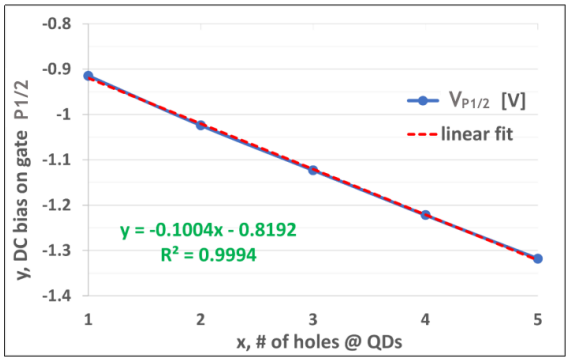


Figure 5: (a) Values of DC bias voltages on plunger gates P1/P2 to create hole configurations from (1,1) to (5,5) in (QD1,QD2). (b) DC bias on plunger gates vs. number of holes at QDs. The linear fit (red dashed line) is given by the green-colored equation. The slope represents the required change of DC bias on gate P1/2 to accumulate one more hole at the QDs.

P-gate voltage and QD hole number is almost linear, as seen from the fitted line (red dashed) in Fig. 5 (b). From the extracted slope one can infer that, in order to accumulate one more hole on each QD, the gate bias on P1 and P2 should be reduced simultaneously by ~ 0.1 V. This observation could be useful for future device design to improve qubit control.

The impact of an increasing hole number on the averaged field polarization vector of the QDs is shown in Fig. 6 (a). From the highlighted values in the tables we conclude that as the dot hosts more holes, the field polarization along -x-direction becomes stronger/weaker at QD1/QD2 respectively. However, the size of this effect is much smaller for QD2 than for QD1 simply because of the longer distance to the AC control gate P1. As a further post-processing step, instead of directly using the normalized field component, we define a field polarization angle, which is the angle between the extracted E-field vector and the -x-axis (see the upper

(a) averaged norm. E-field @ QD1

# of holes @ QD1/2	E_x	E_y	E_z
1/1	**-0.864**	-1.16e-3	0.503
2/2	**-0.951**	-1.36e-3	0.307
3/3	**-0.978**	-1.69e-3	0.209
4/4	**-0.989**	-2.07e-3	0.146
5/5	**-0.994**	-2.44e-3	0.105

averaged norm. E-field @ QD2

# of holes @ QD1/2	E_x	E_y	E_z
1/1	**-0.988**	-2.37e-3	0.157
2/2	**-0.989**	-2.98e-3	0.150
3/3	**-0.977**	-3.27e-3	0.214
4/4	**-0.970**	-3.49e-3	0.245
5/5	**-0.964**	-3.67e-3	0.264

(b)

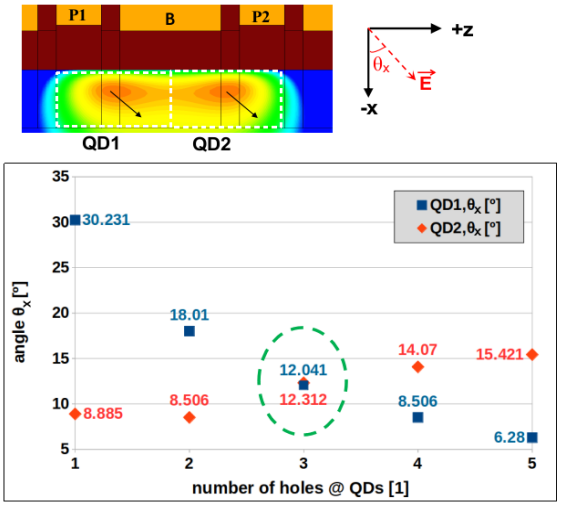


Figure 6: (a) Calculated normalized x/y/z-components of the averaged response-field polarization vector at QD1/2 for hole configurations from (1,1) to (5,5) at (QD1,QD2). (b) Plot of response field polarization angle θ_x vs. number of holes. The slope represents the required change of DC bias on P1/2-gates to accumulate another hole at the QDs.

plot in Fig. 6 (b)). The dependence of this field polarization angle on the number of holes (see the lower plot in Fig. 6 (b)) gradually saturates with increasing hole number. A special situation occurs for the (3,3) hole configuration, where the polarization angles become almost the same at both QDs, as a consequence of the opposite trends (slopes) for QD1 and QD2.

4. Conclusion

A TCAD-based simulation framework for the computation of the microwave response *E*-field polarization is demonstrated using a 5-gate FinFET hole spin qubit device. The extracted field polarization angle at the qubit location will be used for future study of the Rabi driving strength. We showed that the location of the center of the quantum dot has a strong influence on the average field polarization. The latter also depends on the number of holes in the QDs, but this effect quickly saturates with increasing hole number.

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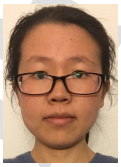

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Prof. Dr. Andreas Schenk had been heading the Nano-Device Physics Group at the Integrated Systems Laboratory (IIS) of ETH Zurich. Since 1991 he had been working as scientific adjoint at the IIS, where he habilitated in 1997 and became honorary professor in 2004. His research focus is on the physics-based modeling of nano- and optoelectronic devices. He authored and co-authored two books and more than 200 refereed papers.

Highlights

- TCAD-based simulation framework is developed to study hole spin qubit in Silicon FinFET
- Microwave response E-field polarization vector at qubit location depends strongly on the dot center location
- Number of holes at quantum dot also impacts field polarization but saturates with more holes

Declaration of interests

☒ The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

☐ The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: