Full-band atomistic study of source-to-drain tunneling in Si nanowire transistors

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Abstract

Source-to-drain tunneling is investigated for Si triple-gate nanowire transistors. The full-band quantum transport problem is solved in an atomistic basis using the nearest-neighbor $sp^3d^5s^*$ tight-binding method. It is self-consistently coupled to the three-dimensional calculation of the electrostatic potential in the device using the finite element method. This procedure is applied to the computation of $I_d - V_{gs}$ transfer characteristics of transistors with different channel orientations such as [100], [110], [111], and [112] for gate lengths ranging from 4 nm to 13 nm. The subthreshold swing S is then extracted from the results to determine the scaling limit of nanowire transistors.

1 Introduction

To further reduce the size of active devices, such as field-effect transistors (FETs), the emergence of new structures and materials is highly required. Nanowire FETs illustrate this miniaturization trend. They are composed of source, gate, and drain regions with extensions of only a few nanometers in the directions of confinement[1]. If the physical gate is long, the current will flow above the gate-induced potential barrier only. However, as the gate length of these nanowire transistors decreases, tunneling from source to drain becomes important for electrons. It increases the subthreshold swing S and the OFF-current, and therefore degrades the transistor performances. Ideally, S should be equal to 60 mV/decade at room temperature. In this paper, a three-dimensional full-band study of source-to-drain tunneling is performed for Si triple-gate nanowire transistors.

2 Method

To model source-to-drain tunneling, the three-dimensional full-band Schrödinger equation is solved for each injection energy with open boundary conditions[2]. The resulting atomistic wave functions are used to obtain the transmission from source to drain and the local density-of-states, which lead to the drain current I_d and the electron charge n, respectively. The Schrödinger equation is self-consistently coupled to the Poisson equation, which is solved with a finite element ansatz assigning point charges only to atom positions. The oxide layers are excluded from the transport calculation, but are included in the computation of the electrostatic potential.
The nearest-neighbor tight-binding method[3] is chosen as band structure model. In the $sp^3d^5s^*$ variant, 19 independent fitting parameters are necessary to reproduce the

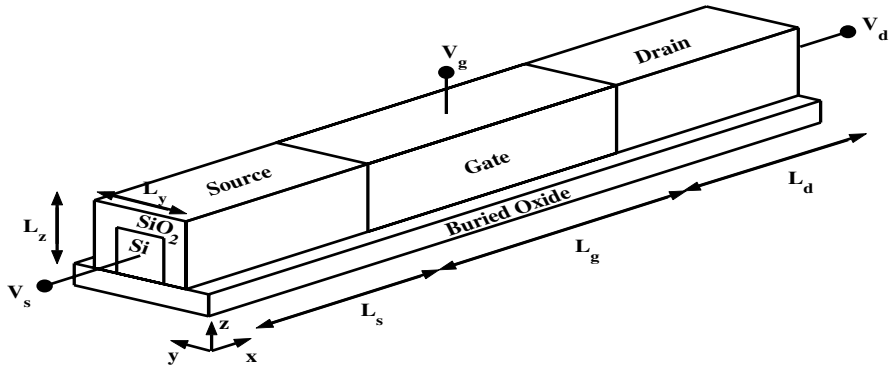
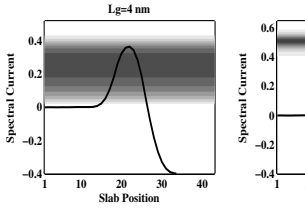


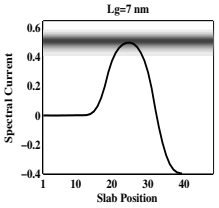
Figure 1: Schematic view of a triple-gate Si nanowire transistor deposed on a buried oxide and surrounded by three oxide layers of thickness t_{ox}=1 nm. The source and the drain measure L_s=10 nm and L_d=10nm, respectively, the gate length L_g is comprised between 4 nm and 13 nm. x is the transport direction, y and z are directions of confinement. The cross section of the nanotransistor (neglecting the buried oxide) is L_y=4.1 nm times L_z=3.1 nm, while the Si nanowire itself has a cross section of 2.1 $\times$ 2.1 nm^2. Voltages V_g, V_s, and V_d are applied to gate, source, and drain, respectively. The n-doped source and drain have a stoichiometric ratio f=2×10^{-3} of fully ionized donors (N_D=10^{20} cm^{-3}). All calculations were done at room temperature.

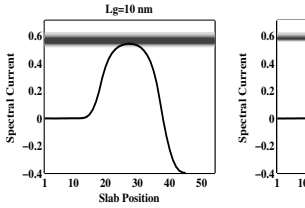
complete Si bulk band structure[4]. It is assumed that these parameters do not change when used for nanostructures. The surface atoms are passivated by increasing their dangling bond energy[5]. Surface reconfiguration is not considered in this paper.

3 Results

Figure 1 shows the schematic view of a Si triple-gate nanowire transistor with a gate length L_g varying from 4 nm to 13 nm. The transport direction x is divided into slabs, or wire unit cell, containing N_A atoms and having a width of Δ. It is aligned with either [100] (N_A=128, Δ=0.543 nm), [110] (N_A=88, Δ=0.384 nm), [111] (N_A=210, Δ=0.941 nm), or [112] (N_A=154, Δ=0.665 nm). In order to illustrate the behavior of source-to-drain tunneling, the energy- and position- resolved drain current is depicted in Figs. 2 and 3 for different channel lengths and crystal orientations. Scattering has no significant effect on the subthreshold slope. Hence it is not included in the simulation, which conserves the spectral current along the device. The shorter the gate becomes, the higher the probability that an electron travels from source to drain through the barrier. This can be seen in the transfer characteristics $I_d - V_{gs}$ in Fig. 4 and in the corresponding subthreshold swing curves in Fig. 5. Values for S are also reported in Table 1.
Source-to-drain tunneling drastically increases the subthreshold swing S when L_g shrinks to 4 nm. For all the transport directions considered in this work, S becomes larger than 80 mV/decade in this case. A gate length L_g as short as 7 nm does not affect too much the transistor performances for a channel along the [100], [111], and [112] crystal axis.







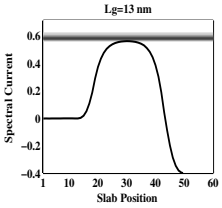
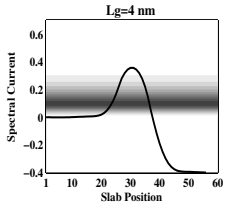
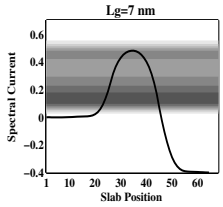
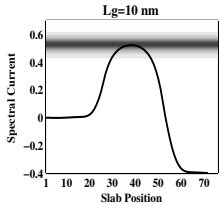


Figure 2: Source-to-drain spectral current in the nanowire transistor of Fig. 1 when x is aligned with [100]. The simulations were done for L_g= 4nm, 7 nm, 10 nm, and 13 nm, V_{gs}=0 V, and V_{ds}=0.4 V.







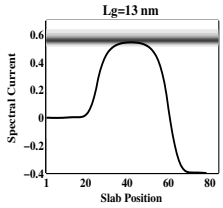


Figure 3: Source-to-drain spectral current in the nanowire transistor of Fig. 1 when x is aligned with [110]. The simulations were done for L_g= 4nm, 7 nm, 10 nm, and 13 nm, V_{gs}=0 V, and V_{ds}=0.4 V.

	[100]	[110]	[111]	[112]
L_g=4 nm	88.5	122.3	83.2	87.5
L_g=7 nm	65.7	78.8	64.7	64.9
L_g=10 nm	61.5	62.9	61.0	61.4
L_g=13 nm	60.6	62.1	60.4	60.6

Table 1: Subthreshold swing S [mV/decade] as function of channel orientation and gate length L_g.

S remains close to its ideal value of 60 mV/decade.
The highest S at L_g=4nm and L_g=7 nm are obtained for a [110] oriented channel. The electron effective mass in transport direction, m^*, is responsible for such a behavior. While a low m^*, as for the [110] orientation, is advantageous for a high mobility and a high ON-current[6], it limits the gate length scaling by increasing the tunneling probability, the OFF-current, and the subthreshold swing. On the other side, a large effective mass m^* in transport direction restricts source-to-drain tunneling, but does not allow to achieve high ON-current.

4 Conclusion

A three-dimensional full-band study of Si triple-gate nanowire transistors shows that source-to-drain tunneling is an important limiting factor in devices with a low transport effective mass and a short gate length. This particularly concerns transistors having channels aligned with [110] and gate lengths smaller or equal to 7nm.

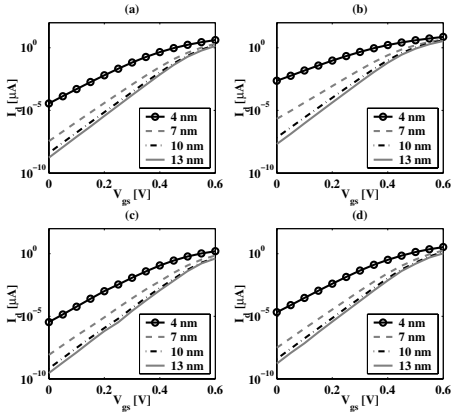


Figure 4: Transfer characteristics $I_d - V_{gs}$ at V_{ds}=0.4 V for the device of Fig. 1 with x= (a) [100], (b) [110], (c) [111], (d) [112] and L_g= 4 nm, 7 nm, 10 nm, and 13 nm.

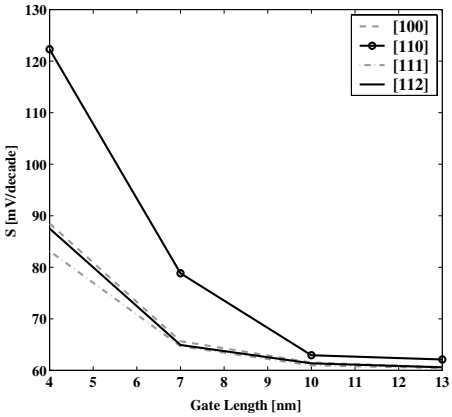


Figure 5: Subthreshold swing as function of the gate length L_g for the nanowire transistor of Fig. 1 with the transport direction x aligned with [100], [110], [111], and [112].

Acknowledgements

This work was supported by the Swiss National Fond (SNF), project 200021-109393 (NEQUATTRO).

References

[1] Y. Cui, Z. Zhong, D. Wang, J. Wang, and C. M. Lieber, "High Performance Silicon Nanowire Field Effect Transistors", Nano Lett., vol. 3, pp. 149-152, 2003.

[2] M. Luisier, G. Klimeck, A. Schenk and W. Fichtner, "Atomistic Simulation of Nanowires in the $sp^3d^5s^*$ Tight-Binding Formalism: from Boundary Conditions to Strain Calculations", Phys. Rev. B, vol. 74, pp. 205323, 2006.

[3] J. C. Slater and G. F. Koster, "Simplified LCAO Method for the Periodic Potential Problem", Phys. Rev., vol. 94, pp. 1498-1524, 1954.

[4] T. B. Boykin, G. Klimeck, and F. Oyafuso, "Valence band effective-mass expressions in the $sp^3d^5s^*$ empirical tight-binding model applied to a Si and Ge parametrization", Phys. Rev. B, vol. 69, pp. 115201, 2004.

[5] S. Lee, F. Oyafuso, P. von Allmen, and G. Klimeck, "Boundary conditions for the electronic structure of finite-extent embedded semiconductor nanostructures", Phys. Rev. B, vol. 69, pp. 045316, 2004.

[6] M. Luisier, A. Schenk, and W. Fichtner, "Three-Dimensional Full-Band Simulations of Si Nanowire Transistors", IEDM, Tech. Dig. 2006, pp. 811-814, 2006.