Trap-Aware Compact Modeling and Power-Performance Assessment of III-V Tunnel FET

Yang Xiang[1, 2], Dmitry Yakimets[2], Saurabh Sant[3], Elvedin Memisevic[4], Marie Garcia Bardon[2], Anne S. Verhulst[2], Bertrand Parvais[2, 5], Andreas Schenk[3], Lars-Erik Wernersson[4] and Guido Groeseneken[1, 2]
[1]Katholieke Universiteit Leuven, 3001 Leuven, Belgium; [2]imec, 3001 Leuven, Belgium; [3]ETH Zürich, 8092 Zürich, Switzerland;
[4]Lund University, 221 00 Lund, Sweden; [5]Vrije Universiteit Brussel, 1050 Brussels, Belgium; Email: Yang.Xiang@imec.be

***Abstract*—We report, for the first time, on a SPICE simulation study of the circuit-level power-performance impact of device traps in a state-of-the-art III-V heterojunction tunnel FET (TFET). First, the parasitic effects of junction bulk traps and oxide interface traps are incorporated in the compact model and validated against measurement-calibrated TCAD data, where we propose an analytical formulation for trap-assisted tunneling and account for the oxide interface charge with a look-up table. Then, the model is used in SPICE simulations on a ring oscillator test bench to predict the impact of traps on logic circuits. It is found that bulk and oxide traps in TFET together cause up to ~5x iso-frequency energy penalty in the desired low-supply-voltage domain (≤ 0.50 V), of which oxide traps dominate at high switching activity while bulk and oxide traps contribute comparably when switching is less active. This study quantitatively suggests that trap reduction is the key to the enablement of the full benefit of TFET.**

I. Introduction

Long known as a steep-subthreshold-slope transistor that promises as an "energy-efficient switch" [1], tunnel FET (TFET) today still suffers from various parasitic effects due to device traps [2, 3]. Despite a range of published studies on the trap effects in TFET at device level [4 – 6], a quantitative assessment of the impact of traps at circuit level is still lacking. Moreover, while such study typically prefers time-efficient implementations in SPICE-like simulators, a trap-effects-inclusive compact model of TFET, as the infrastructure for such simulations, is not yet available to our knowledge.

Based on recent TCAD modeling works of trap-related effects in a start-of-the-art experimental III-V TFET [7, 8], we here propose to extend an existing Verilog-A compact model for an ideal TFET [9, 10] to the parasitic effects due to junction bulk traps and oxide interface traps. Therefore, for the first time, we manage to elucidate the impact of traps in a realistic TFET on its circuit-level power-performance (PP) metrics through SPICE simulations on a ring oscillator (RO) circuit test bench. Further, by selectively turning on different components of the modular model we quantify the relative predominance of different types of traps in the total energy penalty where a switching activity dependence is observed.

II. Model Development and Validation

We consider I-V and C-V modeling of a TFET in Fig. 1(a). The I-V model consists of three elements: (i) band-to-band-tunneling (BTBT) as in an ideal TFET; (ii) trap-assisted tunneling (TAT) due to bulk traps; (iii) electrostatic modulation effect on the I-V curves by oxide traps.

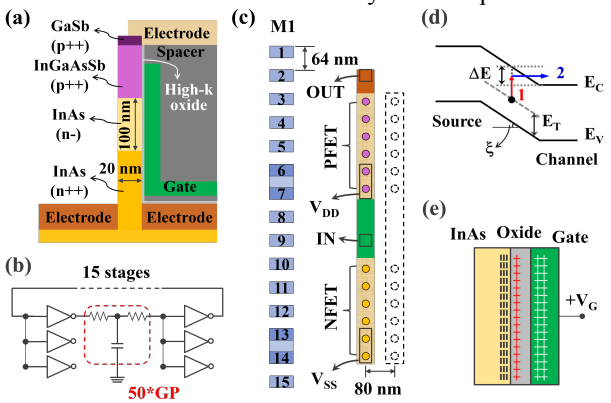

Fig. 1. Schematic of (a) an n-type nanowire (NW) TFET, representing the fabricated device in [7]; (b) the 15-stage RO test bench for PP study, with a wire load of 50 times of the gate pitch (GP); (c) the layout of a vertical TFET inverter cell used in the RO (6*NWs per device), showing a 15-track cell height, a gate pitch of 80 nm and a metal pitch of 64 nm; (d) the two-step TAT process (thermal excitation + tunneling), whereby ξ is the local electric field, E_T is the trap level relative to E_V, ΔE is the tunneling window for TAT; (e) the electrostatic effect of the donor-like oxide interface traps, i.e., the positive charge carried by unfilled traps (red) combined with gate charge (white) gives a higher effective gate voltage than the nominal.

In (i), BTBT current is modeled per the formulae in [9], which are based on the Kane-Sze model of a tunneling junction with an empirical "form factor" f that captures the V_{ds}-modulation of I-V curve (via fitting parameters λ, Γ and V_{OFF}).

In (ii), the TAT generation rate at the source-channel junction is modeled as field-enhanced Shockley-Read-Hall (SRH) generation [11], where the SRH rate is calculated per the trap density and trap level given in [7], whereas the field- and trap-level-dependent enhancement factor G_{TAT} given by (1), found in [11], is implemented numerically in Verilog-A.

$$G_{TAT} = \frac{\Delta E}{k_B T}\int_0^1 \exp\left(\frac{\Delta E}{k_B T}u - \frac{4}{3}\frac{\sqrt{2m^*}(\Delta E)^{3/2}u^{3/2}}{q\hbar|\xi|}\right)du \quad (1)$$

Next, the TAT current density is obtained by integrating the TAT rate over the fitted junction length multiplied by a form factor f' in (2), the construction of which echoes its counterpart for BTBT current in [9] and ensures the earlier onset of TAT current than BTBT (by setting $V'_{OFF} < V_{OFF}$, i.e., a smaller onset voltage of TAT than of BTBT) and the saturation of TAT current to an insignificant finite level at high V_{gs} (i.e., in superthreshold regime) where BTBT dominates.

$$f' = \{1 - \exp(-V_{ds}/\Gamma')\}/\{1 + \exp[(\lambda'\tanh(V_{gs} - V'_{OFF}) - V_{ds})/\Gamma']\} \quad (2)$$

In (iii), the positive charge carried by unfilled donor-like traps in the TFET [7] modifies its channel flat-band voltage

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and consequently results in a higher effective gate voltage that appears as an "apparent gate work function shift", which is captured by (3),

$$V_{gs,eff} = V_{gs} + S \cdot table[Q_{it}(V_{gs},V_{ds})]/C_{ox} \quad (3)$$

where the look-up table of interface charge Q_{it} is from the measurement-calibrated TCAD deck, while the scaling factor S (> 0) is determined by fitting to TCAD I-V data.

The I-V model shows excellent agreement with respect to TCAD data (see Fig. 2(a)), except that the ambipolar current I_{ambi} is switched off and replaced by V_{ds}-dependent leakage floors instead. The pitfall of operating in the ambipolar regime is avoided as we "virtually" adjust the gate work function Φ_G as a parameter in SPICE such that the logic "0" is automatically set to the highest voltage that gives the targeted off-current I_{off}, meaning that the nodes in a logic circuit are programmed not to see I_{ambi} when switched between 0 and V_{dd}.

To model the C-V characteristics, an empirical Q-V model in [10] is implemented to capture the "intrinsic" gate charge in an ideal TFET. While the bulk traps are assumed electrically inactive (per [7]) and thus cause no change in Q-V, the oxide interface charge due to oxide traps is included by way of the same table Q_{it} in (3). The derivative of Q_g to V_{gs}, namely C_{gg}-V_{gs} is then validated against TCAD data with good accuracy, as can be seen in Fig. 2(b), where the extra gate capacitance as a signature of (dis-)/charging of oxide traps is clearly visible.

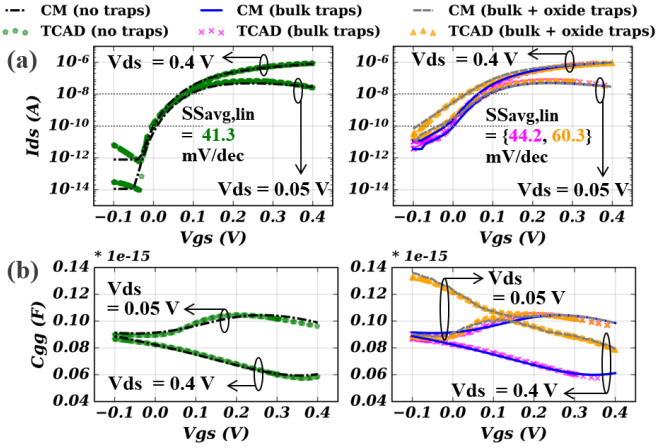

Fig. 2. (a) I_{ds}-V_{gs} and (b) C_{gg}-V_{gs} characteristics of the NW TFET in Fig. 1(a) simulated by TCAD (symbols) and the compact model (curves, "CM") at T = 298 K in three different trap scenarios: "no traps" (I-V due to BTBT; C-V due to intrinsic charge), "bulk traps" (I-V due to BTBT + TAT; C-V due to intrinsic charge) and "bulk + oxide traps" (I-V due to BTBT + TAT + electrostatic effect; C-V due to intrinsic charge + oxide interface charge). The average subthreshold swing ($SS_{avg,lin}$) is calculated at V_{ds} = 0.05 V across $I_{ds} \in [10^{-10}$ A, 10^{-8} A].

III. Circuit Simulation

Using the calibrated model above, we perform SPICE simulations on a 15-stage RO test bench (Fig. 1(b)) made of vertical-TFET-based inverters (Fig. 1(c)), where the P-TFET assumes mirrored I-V and C-V characteristics of an N-TFET. The intracell parasitic RC is calculated similar to [12].

The PP study begins with a sweep of V_{dd} and I_{off} target in all combinations of 0.10 V $\leq V_{dd} \leq$ 0.50 V and 1 pA $\leq I_{off} \leq$ 10 nA, whereby I_{off} targeting is implemented by varying Φ_G (note that pA-order I_{off} can be only met at low V_{dd} when assuming no traps). Next, the energy consumption per switch is calculated as a weighted sum of dynamic and static energy at both high (10 %) and low (0.1 %) activity factor (*af*), which represent high-performance and standby-mode applications, respectively [13]. Finally, a Pareto optimization similar to [13] is performed on all solutions to find the minimum energy at each frequency, with the optimized energy-frequency relations shown in Fig. 3.

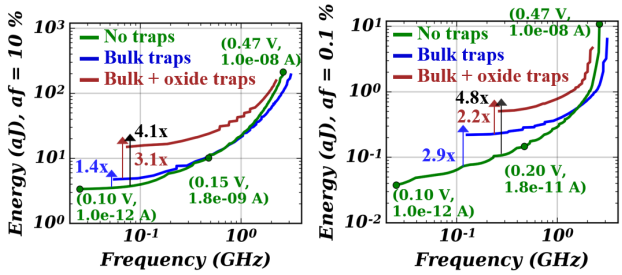

Fig. 3. The Pareto-optimized energy versus frequency in a TFET-based 15-stage RO circuit in the three different trap scenarios in Fig. 2, at activity factor of 10 % (left) and 0.1 % (right); only optimized solutions from $I_{off} \in [10^{-12}$ A, 10^{-8} A] and $V_{dd} \in$ [0.10 V, 0.50 V] are shown. Bulk traps and oxide traps increase iso-frequency energy consumption of the TFET up to 1.4x/2.9x (high/low *af*) and 3.1x/2.2x (high/low *af*), respectively, while the overall effect of two types of traps translates to an energy penalty of up to 4.1x/4.8x (high/low *af*). Note that the iso-frequency energy penalty factor of bulk traps and of oxide traps are calculated at different frequency values.

Clearly, by including all parasitic trap effects in a TFET we readily observe an iso-frequency energy penalty up to > 4x in the low-frequency corner – a regime commonly identified as more energy-efficient of TFET compared to MOSFET [13]. Notably, such negative impact is more pronounced at low *af* when static energy becomes significant, which is understandable given the rise in leakage floor and the degraded subthreshold slope due to traps (Fig. 2(a)). Meanwhile, while at low *af* bulk and oxide traps appear to contribute comparably to the total energy increase, oxide traps begin to take over as the dominant source at high *af* – this turns out to come from the extra gate capacitance seen in Fig. 2(b), which gives rise to an increased dynamic energy; since dynamic energy dominates at high *af*, the detrimental effect of oxide traps becomes principal.

IV. Conclusions

We have investigated, for the first time, the impact of bulk and oxide traps in a heterojunction TFET on its circuit-level PP metrics by including TAT and electrostatic trap effects in a compact model for SPICE simulations. We find that an iso-frequency energy penalty up to ~ 5x can be expected from trap-related effects due to device nonidealities even in a state-of-the-art TFET. This implies that further reduction in trap density at the junction hetero-interface and oxide interface is yet to be accomplished in order to exploit the full potential of TFET.

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