InAs-Si Heterojunction Nanowire Tunnel Diodes and Tunnel FETs

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Abstract

In this paper we present vertical tunnel diodes and tunnel FETs (TFETs) based on III-V–Si nanowire heterojunctions. We experimentally demonstrate InAs–Si Esaki tunnel diodes with record high currents of 6 MA/cm^2 at 0.5 V in reverse bias. Furthermore, we have fabricated vertical InAs–Si nanowire TFETs with gate-all-around architecture and high-k dielectrics. The InAs–Si combination allows achieving high I_{on}/I_{off} ratios above 10^6, with I_{on} of 2.4 µA/µm and an inverse subthreshold slope of 150 mV/dec over three decades. The achieved improvements can be attributed to increased nanowire doping and Ni alloying of the top contact. The results indicate the benefits of the InAs–Si material system combining the possibility of achieving high I_{on} with high I_{on}/I_{off} ratio.

Introduction

A primary concern for future nanoelectronic circuits and systems is to lower the power dissipation in switching devices [1]. This quest for a new nanoelectronic low power switch has triggered the investigation of a variety of emerging devices for ultra-low power integrated circuits [2]. Tunnel FETs (TFETs) promise to achieve a subthreshold swing, *SS*, of below 60 mV/dec. at room temperature as they utilize band-to-band-tunneling (BTBT) for charge injection. Compared to MOSFETs a performance advantage is especially expected at low operation voltage where a higher current level may be achieved. In order to yield high tunneling probabilities, and hence high on-currents, (I_{on}), heterojunctions are required to lower the effective energy barrier height. An effective gate coupling is even more crucial than for MOSFETS, hence new architectures such as gate-all-around structures are beneficial [3]. In this paper we present our results on the fabrication and characterization of vertical InAs–Si heterojunction nanowire (NW) tunnel diodes and TFETs with InAs as low bandgap source. This material system possesses a small effective bandgap [4], allows for integration on a Si platform and maintains the advantages of Si as channel and drain [5, 6].

Nanowire Growth and Device Fabrication

n-type InAs NWs are grown on Si <111> by selective area epitaxy within e-beam patterned SiO_x openings by metal-organic chemical vapor deposition (MOCVD). The NW diameter of ≈110 nm allows epitaxial growth with an abrupt interface despite the large lattice mismatch of 11.6%

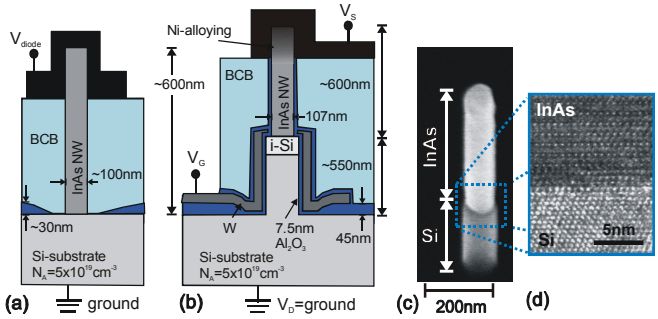

Fig. 1. Schematic of InAs–Si (a) tunnel diode and (b) TFET. (c) SEM image showing a InAs–Si heterojunction NW. The InAs NW is grown on Si <111> by selective area growth. It serves as etch mask during RIE into the Si substrate. (d) HR-TEM image of the InAs–Si interface.

(see Fig. 1d). Tunnel diodes and TFETs as illustrated in Fig. 1(a, b) were fabricated. For TFETs the wire shape was transferred into the Si wafer by reactive ion etching (RIE) (Fig. 1c). Tunnel diodes were fabricated with a *p*-doped Si substrate (N_A = 1.2·10^{20} cm^{-3}) and *n*-type InAs NWs where the doping concentration N_D was controlled by in-situ doping with disilane from 2·10^{18} cm^{-3} to 5·10^{19} cm^{-3}. For TFETs the Si drain doping was N_A = 5·10^{19} cm^{-3}, followed by a 150-nm-long intrinsic Si region. The InAs NW source was grown with N_D = 5·10^{17} cm^{-3} at the heterojunction with increasing doping concentration towards the top contact region reaching N_D = 1·10^{19} cm^{-3}. The wrap-around gate stack consists of 7.5 nm Al_2O_3 deposited by atomic layer deposition at 250°C, followed by a tungsten gate. RIE etching is used to define the gate length. Various isolation layers are used as indicated in Fig. 1(a, b). The TFET top contacts are fabricated by evaporation of Ti/Al or Ni and lift-off. To form Ni_xInAs alloy in the NW top part the device was annealed for 90 s at 230°C in Ar. For tunnel diodes Ti/Au was used as top contact without annealing.

InAs–Si Nanowire Tunnel Diodes

Tunnel diodes are an ideal system to investigate the quality of the heterointerface and the limits of the achievable tunneling current. The effect of *n*-type doping level in InAs on the current density J_D is shown in Fig. 2. For both doping levels N_D negative differential resistance (NDR) is observed (Fig. 2a). The tunnel current significantly increases with higher doping concentration reaching record high values of 6 MA/cm^2 at 0.5 V in reverse bias and peak-current densities up to 570 kA/cm^2 for N_D = 5·10^{19} cm^{-3}. This data is in

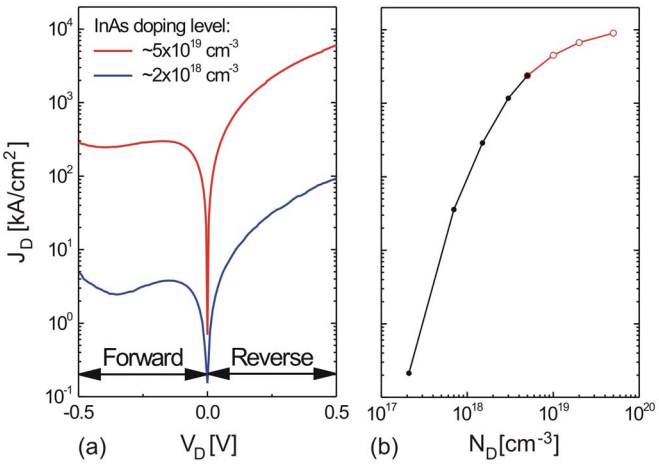

Fig. 2: (a) Measured J_D-V_D characteristics of InAs–Si heterojunction tunnel diodes with *p*-doping level in Si of N_A=1.2·10^{20} cm^{-3} and different *n*-doping level in InAs of N_D=5·10^{19} cm^{-3} and N_D=2·10^{18} cm^{-3}. Nanowire diameter: ≈130 nm. (b) Calculated current density J_D versus N_D at a reverse bias of 0.5 V. For high N_D the simulation did not converge but the extrapolation (open symbols) shows a value of 10 MA/cm^2 for N_D = 7·10^{19} cm^{-3}.

excellent agreement with TCAD simulations [7] where J_D of 10 MA/cm^2 can be reached not taking defects into account (Fig. 2b). These results show that extremely thin tunnel junctions can be achieved with in-situ doped selective NW growth of InAs on Si. The excess current rises with doping level which may be due to increasing band tails and defects at the heterointerface.

Low-temperature measurements of d^2I/dV^2 vs. V_D (Fig. 3) of tunnel diodes with N_D = 5·10^{17} cm^{-3} show pronounced peaks in forward bias which can be attributed to trap-assisted tunneling due to defect states in the bandgap [8]. In reverse bias the effect of traps is suppressed due to the one-sided nature of the InAs–Si heterojunction; the BTBT generation rate shifts with increasing reverse bias into the InAs and away from the heterointerface where trap states are no longer available for transport (see Fig. 4). In case of higher doping in InAs, the generation rates would shift toward the

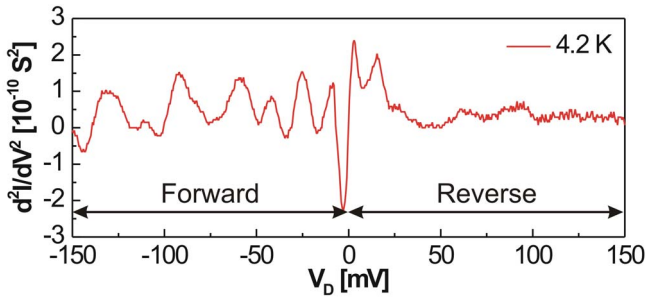

Fig. 3: Trap-assisted tunneling in InAs–Si heterojunction tunnel diodes (N_D = 5·10^{17} cm^{-3}, N_A = 1·10^{20} cm^{-3}). The second derivative of current with respect to voltage was measured at 4.2 K. Pronounced peaks in forward bias originate from trap-assisted tunneling due to defect states in the bandgap. In reverse bias peaks are less distinct.

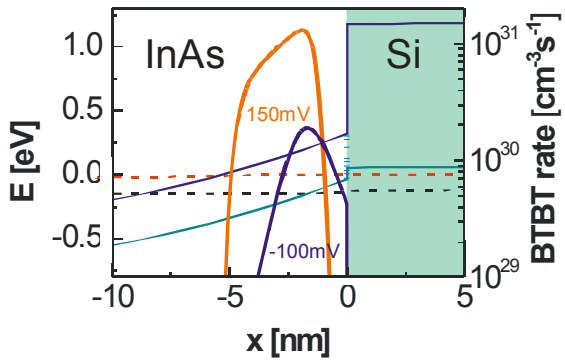

Fig. 4: Calculated band edge diagram (300 K) of the InAs–Si junction at 150 mV reverse bias. With increasing reverse bias, valence band states become available for tunneling within InAs and the tunneling rate (local model is used here) is shifted away from the interface, into the InAs where trap states are no longer available for transport (orange curve). The blue curve corresponds to the generation rate profile for 100 mV forward bias, indicating a finite tunneling rate at the interface.

heterointerface. For TFETs avoiding defects and dislocations at the heterointerface is crucial to achieve steep slope and low off current.

InAs–Si Nanowire Tunnel FETs

Fig. 5 shows the *p-i-n* diode characteristics of the TFET structure measured with floating gate before and after annealing. In this *p-i-n* structure NDR is not expected to be observed. Annealing significantly increased the current levels by two orders of magnitude which is attributed to the formation of Ni$_x$InAs alloy.

The output characteristics of an annealed TFET are shown in Fig. 6 for various gate bias levels. The typical superlinear behavior for TFETs is observed. The corresponding transfer characteristics of the annealed device are shown in Fig. 7 together with *SS* as function of temperature (inset). High

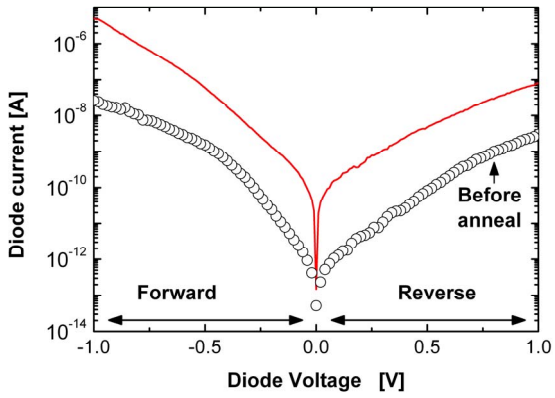

Fig. 5: *p-i-n*-Diode characteristics of the InAs–Si NW TFET with Ni contact measured with floating gate before and after annealing (NW diameter ≈ 107nm).

I_{on}/I_{off} ratios of 10^6 are attained. The highest I_{on} achieved was 2.4 µA/µm at $V_G = -1$ V and $V_S = 1$ V. Fig. 8a compares the temperature dependence of I_{on} for TFETs with alloyed Ni top contact to reference devices with Ti/Al [9]. For the TFETs with Ti/Al contact an activation energy of 80 meV was determined by temperature-dependent characterization. Improving the top contact by high doping and Ni alloying (Fig. 9) significantly reduces the temperature dependence. This indicates that a potential barrier, either from a Schottky barrier or from an ultra-thin interface layer has been removed. The remnant temperature dependence of the on current might be due to trap-assisted tunneling. Also the subthreshold swing *SS* shows slight temperature dependence (see inset Fig. 7). This may be due to the presence of interface states at the oxide interface which gradually freeze out as the temperature is reduced.

The steepest *SS* measured over two decades in current was 120 (Fig. 8b) and 150 mV/dec over three decades in current measured, on several devices. Measurements of Si nanowire MOS capacitors have shown that the interface state density D_{it} is in the range of $(4 \pm 1) \cdot 10^{12}$ cm^{-2}eV^{-1} [10]. To improve the device performance and in particular *SS* further, the quality of the gate stack, interface state density and equivalent oxide thickness need improvement. The shift of the transfer characteristics observed in Fig. 8b may be due to a remaining contact resistance or due to the complex dependence of the tunneling path on both V_S and V_G. As mentioned before the BTBT rate moves into InAs with increasing V_S bias. This can be seen also in Fig. 10 which shows the 2D image of the BTBT generation rate calculated by TCAD at $V_G = -0.5$ V for various V_S from 0.25 V to 1.0 V. The TCAD calculations of the InAs–Si heterojunction indicate in-junction and off-junction tunneling with dominant off-junction tunneling at high V_S.

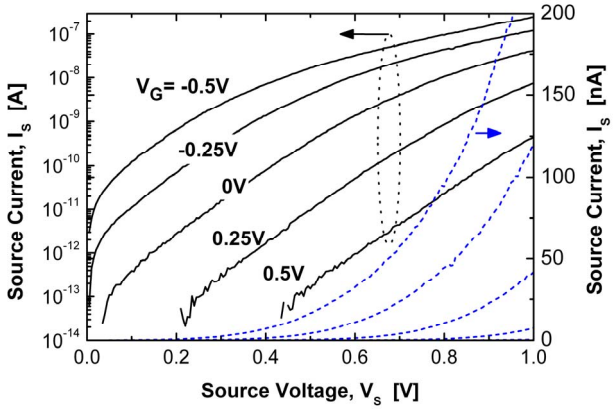

Fig. 6: Output characteristics of TFET with Ni contact for different gate bias levels, measured after annealing.

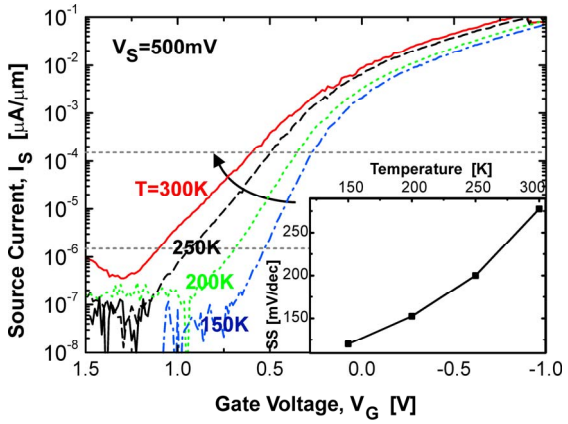

Fig. 7: Transfer curves after annealing for various temperatures from 150 to 300 K. Dashed horizontal lines indicate range used for *SS* extraction, which is shown in inset as function of temperature.

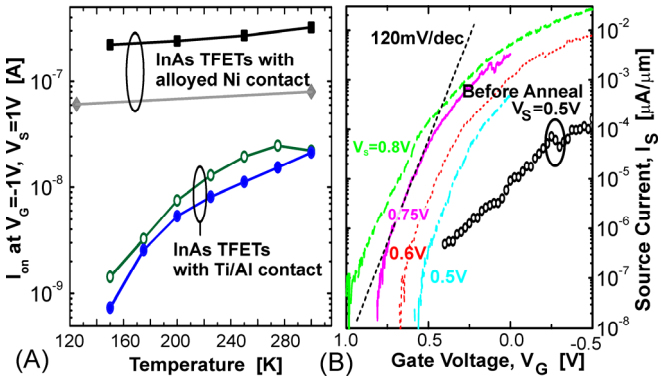

Fig. 8: (A) I_{on} vs. temperature measured at $V_G = -1$ V, $V_S = 1$ V. TFETs with improved source contact show less temperature dependence. (B) Transfer characteristics after annealing and before annealing as reference.

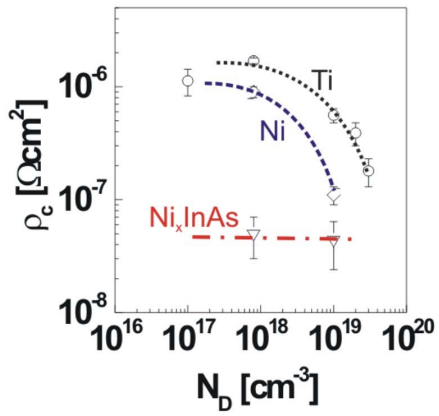

Figure 9: Specific contact resistivity ρ_C vs. doping concentration N_D for *n*-doped InAs nanowires with Ti/Au and Ni contacts. The red dashed line was measured for a fully alloyed InAs wire.

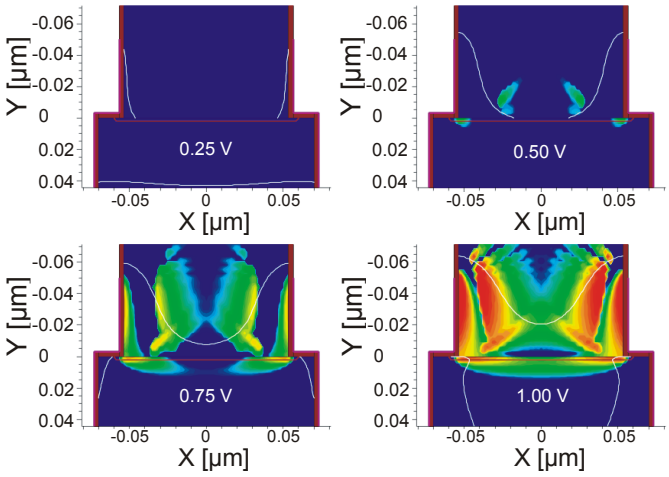

Fig. 10: 2D image of the simulated BTBT generation rate at V_G = –0.5 V for various V_S showing the contributions from in-junction and off-junction tunneling within InAs. (Si: $N_A = 1 \cdot 10^{19}$ cm^{-3} and InAs: $N_D = 5 \cdot 10^{17}$ cm^{-3})

An attempt to compare the device performance of published TFETs based on Si, SiGe, III-V–Si and all–III-V homo- and heterojunctions is shown in Fig. 11. Since these emerging devices are not all measured under the same bias conditions the maximum I_{on} (maximum reported drain current) and minimum I_{off} (minimum reported drain current) measured at V_{SD} = 0.5 V are compared for various TFET implementations. TFETs based on Si, SiGe including strained devices show typically a good I_{on}/I_{off} ratio of below 10^{-4}, however with I_{on} of typically below 1 µA/µm. Instead devices based on all–III-V homo- and heterostructures achieve high currents of up to 200 µA/µm, but with very low I_{on}/I_{off} ratio. On the contrary, the InAs-Si material systems achieves very high I_{on}/I_{off} ratio and seems promising also for high I_{on} due to the record high tunnel currents achieved in tunnel diodes.

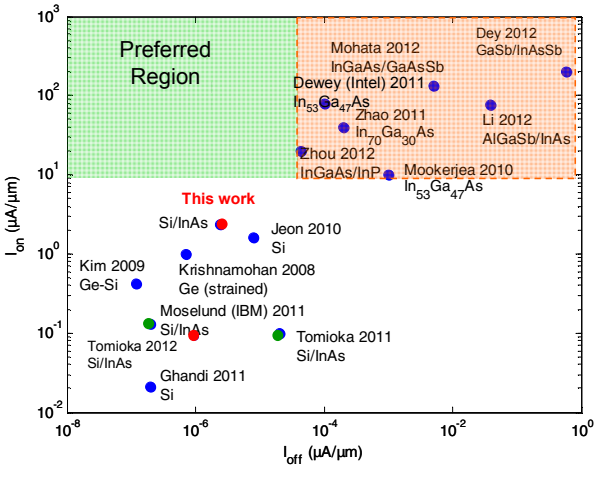

Fig. 11: Comparison of I_{on} vs. I_{off} of published TFETs. Maximum I_{on} and minimum I_{off} measured at V_{SD} = 0.5 V for various TFET implementations.

Conclusions

We have demonstrated InAs–Si vertical heterojunction NW tunnel diodes with negative differential resistance and record high currents of 6 MA/cm^2 at 0.5 V in reverse bias. In addition, gate-all-around InAs–Si TFETs are presented with I_{on} of 2.4 µA/µm, $I_{on}/I_{off} \approx 10^6$ and a slope of 150 mV/dec over three decades. The achieved improvements can be attributed to increased in-situ doping of the NW and Ni alloying of the top contact indicating the importance of contact resistances in these NW device structures. Further TFET performance enhancements can be anticipated by optimizing the electrostatic control, the source doping concentration, and the gate overlap.

Acknowledgements

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