Analysis of InAs-Si Heterojunction Nanowire Tunnel FETs: Extreme Confinement vs. Bulk

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***Abstract*—Extremely narrow and bulk-like p-type InAs-Si nanowire TFETs are studied using a full-band and atomistic quantum transport simulator based on the $sp^3d^5s^*$ tight-binding model and a drift-diffusion TCAD tool. As third option, the WKB approximation has been adapted to work in heterostructures through a careful choice of the imaginary dispersion. It is found that for ultra-scaled InAs-Si nanowire TFETs, the WKB approximation and the quantum transport results agree very well, suggesting that the former could be applied to larger hetero-TFET structures and considerably reduce the simulation time while keeping a high accuracy.**

I. Introduction

Among the new generation of devices, band-to-band tunneling (BTBT) FETs (TFETs) are considered as very promising candidates on the road towards energy-efficient transistors. However, the performance of TFETs is still limited, especially the ON-current remains very low. Heterostructures made of III-V/Si materials have been proposed to address this issue [1], [2]. Recently, InAs nanowires with diameters of few tens of nanometers have been grown on Si substrates [2]. Although these devices exhibit a good electrostatic control due to their gate-all-around configuration, they still can be considered as bulk-like. In case of InAs, it has been proved that quantum confinement effects manifest themselves when the nanowire diameter does not exceed 20 nm [3]. In order to shed light on the impact of confinement, a realistic bulk-like and an extremely narrow InAs-Si nanowire TFET are studied in this paper. A TCAD tool and an atomistic tight-binding quantum transport simulator called OMEN [4] are employed for that purpose. OMEN is a multidimensional atomistic simulator based on a $sp^3d^5s^*$ tight-binding representation of the band structure of various semiconductors [4]. Quantum transport equations are solved within the Non-Equilibrium Green's Function (NEGF) or Wave Function (WF) formalism together with Poisson's equation self-consistently. OMEN has been successfully applied to the simulation of homo-TFETs with direct and phonon-assisted band-to-band tunneling [5]. Despite a high computational efficiency, the size of the structures OMEN can handle is very limited. This does not apply to drift-diffusion TCAD tools, e.g. the Sentaurus-Device (S-Device) simulator from Synopsys [6], which offer local and non-local analytical BTBT models.

II. Test device: bulk-like InAs-Si Esaki diode

For heterostructures, the applicability of analytical BTBT models like the "*dynamical nonlocal path BTBT*" (Kane model) [7] might be called into question because no analytical theory/model exists for BTBT between a direct (InAs) and an indirect (Si) semiconductor. A very simple work-around is either to consider a zero-phonon (direct BTBT) or a phonon-assisted (indirect BTBT) tunneling path through the interface of the two materials as required by S-Device. As will be discussed below, in an InAs-Si heterostructure the first case is more appropriate and can be achieved by using the Kane model as given for the InAs side with the well-established values for gap and effective masses, but with calibrated parameters (called "A" and "B" in S-Device) for the silicon side using the experimental data of Solomon et al. [8]. Likewise, the analytical model developed for phonon-assisted tunneling in silicon [9] could be used on both sides provided that the phonon energy is set to a very small value on the InAs side and critical field and prefactor are carefully adjusted to match the BTBT rate in InAs [10]. Both variants give similar results. The first one has been used here. It is labeled "TCAD, bulk parameters" in Fig. 1 because the parameters of the bulk materials are applied piecewise. Note that the described complication only occurs for inter-material tunneling ("point tunneling") but not for under-the-gate tunneling ("line tunneling"). The latter has tunneling paths fully contained in InAs and dominates the ON-current in a bulk-like InAs-Si TFET as will be shown below.

Assuming that inter-material tunneling only occurs between the Si valence band and the InAs conduction band, BTBT in the InAs-Si heterostructure is expected to be mainly direct. This is illustrated in Fig. 1 where the ON-current density of a bulk-like InAs-Si Esaki diode (circular geometry, n-type InAs nanowire with radius of $R \approx 60\,\text{nm}$ grown on a p-type $\langle 111 \rangle$ Si substrate) is plotted as a function of donor concentration. It has been verified that the tunneling current computed with OMEN does not depend on the presence of electron-phonon scattering, indicating that the inter-material tunneling through a Si-InAs junction is direct. It can also be observed in Fig. 1 that the ballistic S-Device current simulated by the aforementioned work-around (labeled "TCAD, bulk parameters") agrees well with OMEN up to a concentration of $N_\text{D} \approx 4 \times 10^{19}\,\text{cm}^{-3}$. For higher donor concentrations the pn-junction becomes one-sided. Therefore, the tunneling path more and more penetrates into Si leading to a decreasing tunnel current since the BTBT rate in bulk silicon is much smaller than that of InAs. This behavior is not found with OMEN! The discrepancy is a clear indication for direct tunneling. The direct tunneling process can be modeled in S-Device using a "model semiconductor", i.e. a homo-junction with a common gap (called "tunnel gap") and a reduced effective mass built from the Si light-hole mass and the InAs Γ-mass. The Si light-hole mass in $\langle 111 \rangle$-direction was extracted from OMEN, and the tunnel gap was chosen as the InAs gap reduced by half of the valence band offset ($\Delta E_\text{v} = 80\,\text{meV}$). This results in the open symbols in Fig. 1. With such an approach the current does not drop anymore. Unfortunately, this method cannot be easily applied to hetero

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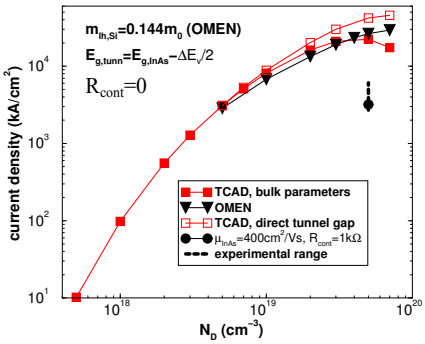

Fig. 1. BTBT current density of a bulk-like InAs-Si Esaki-diode as a function of donor concentration in InAs at a reverse bias of $V = -0.5\,\mathrm{V}$. Comparison between OMEN and different TCAD approaches (S-Device) described in the text.

TFETs as it would require to identify three types of tunnel paths - bulk-InAs, bulk-Si, and inter-material - each with its own model. Finally, TCAD allows to include the measured mobility in the InAs wires as well as the measured contact resistance. These parasitic resistances have a strong effect on the ON-current as shown in Fig. 1 by the single simulation point in comparison with the experimental range.

III. Imaginary Dispersion Models

BTBT can be interpreted as the transfer of electrons between the valence and conduction bands of one (homo) or two (hetero) semiconductor(s). In such a process, the valence and conduction band edges are bridged within the forbidden energy gap by an imaginary dispersion. Fig. 2 shows the bulk imaginary dispersion of InAs and Si along the $\langle 111 \rangle$ crystal direction. The full-band imaginary dispersion is obtained by a $sp^3d^5s^*$ tight-binding calculation with OMEN. Different analytical models are compared to this reference curve. As expected for a direct small-gap semiconductor, all 2-band models, e.g. the Kane [7] and Flietner [11] model, are equally suitable for InAs. On the other hand, the one-band EMA model fits much better the full-band dispersion of Si. The Flietner imaginary dispersion can be expressed analytically as

$$\kappa = \sqrt{\frac{2m_{\mathrm{v}}E_{\mathrm{g}}}{\hbar^2}}\,\frac{\kappa_{\mathrm{c}}\kappa_{\mathrm{v}}}{\kappa_{\mathrm{c}}^2 + (1-\alpha)\kappa_{\mathrm{v}}^2}, \tag{1}$$

where $m_{\mathrm{v(c)}}$ and $\kappa_{\mathrm{v(c)}} = \sqrt{2m_{\mathrm{v(c)}}|E - E_{\mathrm{v(c)}}|/\hbar^2}$ are the hole (electron) effective mass and the one-band imaginary dispersion for the valence (conduction) band, respectively. The variable $E_{\mathrm{g}} = E_{\mathrm{c}} - E_{\mathrm{v}}$ is the energy gap and the parameter α is defined as $1 - \sqrt{m_{\mathrm{c}}/m_{\mathrm{v}}}$.

In a 3-dimensionl (3D) extremely narrow nanowire TFET the band edges, $E_{\mathrm{v(c)}}(x,y,z) = E_{\mathrm{v(c)}} + U_{\mathrm{e}}(x,y,z)$, are position-dependent due to the 3D electrostatic potential $U_{\mathrm{e}}(x,y,z)$. Consequently, the imaginary dispersion in Eq. (1) is position-dependent, too, and the WKB transmission probability must be modified according to

$$T(E) = \frac{1}{A}\int_A dydz\, \exp\left\{-2\int \kappa(x,y,z)dx\right\}, \tag{2}$$

with A being the cross section area perpendicular to the transport direction, i.e. the x-direction. Note that the transmission

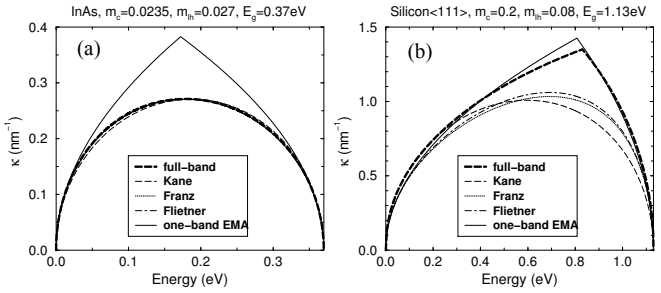

Fig. 2. Bulk imaginary dispersion along the crystal orientation $\langle 111 \rangle$ (a) InAs and (b) Si. Different analytical 2-band models are compared to each other and to the full-band imaginary dispersion obtained with the $sp^3d^5s^*$ tight-binding approach.

is averaged over the nanowire cross section. From the semi-classical expression for the BTBT current, $I_{\mathrm{s-c}} = q\int GdV$, and the Landauer formula, a relation between the generation rate G and the transmission probability $T\left(E_{\mathrm{v(c)}}\right)$ can be established

$$G_{\mathrm{v(c)}} = \frac{1}{\pi\hbar A}\,T\left(E_{\mathrm{v(c)}}\right)\left\{f_{\mathrm{L}}(E_{\mathrm{v(c)}}) - f_{\mathrm{R}}(E_{\mathrm{v(c)}})\right\}\nabla_{\mathrm{x}}U_{\mathrm{e}}, \tag{3}$$

where the x, y and z coordinates have been omitted for brevity.

Flietner model for heterostructures

In a heterostructure, electrons are transferred from one material to the other when going through the junction interface. The different materials can be incorporated into the Flietner model by making the effective masses and energy gaps position-dependent, i.e. $m \rightarrow m(x,y,z)$ and $E_{\mathrm{g}} \rightarrow E_{\mathrm{g}}(x,y,z)$, respectively. Then, the WKB approximation in Eq. (2) can be used to compute the BTBT transmission probability, e.g. in narrow InAs-Si nanowire TFETs.

IV. InAs-Si TFET Simulations

In Fig. 3(a) a schematic of the IBM p-TFET studied in this work is presented: a n^+−InAs nanowire (source) is grown on a $\langle 111 \rangle$ p^+−Si layer (drain). This realistic device can still be considered as bulk-like since the nanowire diameter exceeds 100 nm on both the InAs and Si sides, with a total length of 250 nm. The doping concentrations have been estimated to be $N_{\mathrm{A}} = 5\times10^{19}\,\mathrm{cm}^{-3}$ in Si and $N_{\mathrm{D}} = 5\times10^{17}\,\mathrm{cm}^{-3}$ in InAs. The ultra-scaled TFET depicted in Fig. 3(b) has a diameter equal to 3.5 nm and a total length of 60 nm. In this case the doping concentrations are $N_{\mathrm{A}} = 2\times10^{20}\,\mathrm{cm}^{-3}$ and $N_{\mathrm{D}} = 10^{19}\,\mathrm{cm}^{-3}$. In both devices, the gate is all-around the channel composed of an intrinsic Si region with an overlap covering a part of the InAs side. The effective oxide thickness is set to 3.5 nm for the bulk device and 0.46 nm for the extremely narrow device with the same oxide permittivity $\epsilon_{\mathrm{high}-\kappa} = 9$.

Device simulations are performed with two different TCAD tools: the S-Device simulator to solve the transport problem in the bulk device and OMEN to take into account the atomistic structure of the InAs-Si nanowire. Once the quantum transport problem has been solved with OMEN, in a post-processing step, the converged electrostatic potential is used as an input to compute the BTBT current based on the WKB approximation and the Flietner 2-band model for the imaginary dispersion.

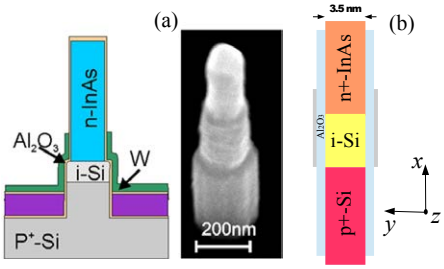

Fig. 3. Schematic of the IBM InAs-Si p-TFET [12]: (a) real size and (b) extremely narrow nanowire.

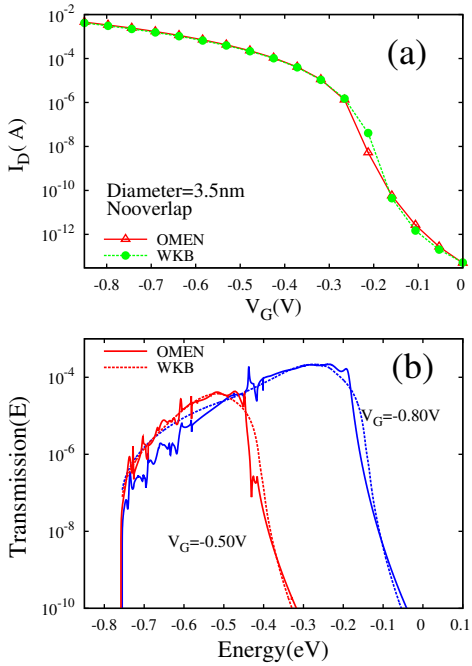

Fig. 4. (a) OMEN and WKB $I_D - V_G$ characteristics of a InAs-Si nanowire p-TFET with drain-to-source voltage $V_{DS} = -1$ V. The diameter is 3.5 nm and no gate overlap is considered. (b) Transmission probability computed with OMEN and the WKB approximation for two different gate voltages. The imaginary dispersion is described by the Flietner model for heterostructures.

Since the bandstructure is no longer bulk-like, the electron effective masses must be adjusted according to the tight-binding calculations. For a nanowire with a diameter equal to 3.5 nm, the effective masses are: $m_v = 0.095\, m_0$ for Si and $m_v = m_c = 0.058\, m_0$ for InAs. Similarly, the energy gap increases due to the strong confinement and it is found to be $E_g = 1.41$ eV and $E_g = 0.98$ eV for Si and InAs, respectively.

Fig. 4 shows the $I_D - V_G$ characteristics and the BTBT transmission probability computed using OMEN and the WKB approximation for an extremely narrow InAs-Si nanowire p-TFET with no gate overlap. It can be seen that by combining the WKB approximation and Flietner model the results obtained with OMEN can be reproduced with great accuracy as long as the appropriate electrostatic potential and material parameters are provided. In Fig. 5, the $I_D - V_G$ characteristics of the two devices considered in this work are plotted, with and without gate overlap on the InAs side. Comparing Fig. 5(a) and Fig. 5(b), it appears that the ultra-scaled TFET exhibits

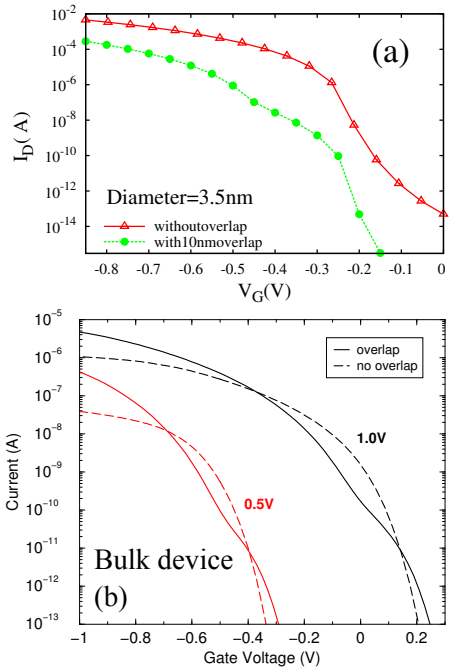

Fig. 5. $I_D - V_G$ characteristics of InAs-Si nanowire p-TFETs with and without gate overlap. Two cases are compared: (a) ultra-scaled with $V_{DS} = -1$ V and (b) real-size nanowires.

a behavior opposite to the bulk-like device; the ON-current of the device with overlap is lower in Fig. 5(a) whereas in Fig. 5(b) it is higher. Moreover, Fig. 5(a) shows that in the case of the extremely narrow nanowire TFET with gate overlap the current can be less than $10^{-14}\,\mu$A, suggesting that there is less than one electron per second flowing through the device. This can be attributed to the fact that at very low gate voltages, electrons must tunnel through a higher and wider potential barrier to transfer from Si to InAs, as compared to the case without gate overlap. Therefore, only few electrons reach the InAs conduction band and the OFF-current is significantly reduced in extremely narrow InAs-Si nanowire TFETs. In the bulk-like TFET with a gate overlap region, there is an additional tunneling path perpendicular to the transport direction ("line tunneling"), as shown in Fig. 6, where the generation rate in a real-size InAs-Si p-TFET without and with gate overlap is reproduced. Fig. 6(c) shows that a high BTBT generation occurs under the gate overlap region at $V_{GS} = -0.5$ V and $V_{DS} = -1$ V. Because these tunneling components are dominant in the ON-state, the ON-current is higher, as reported in Fig. 5(b). However, in strongly confined systems, the gate voltage required to align the highest valence and lowest conduction subbands under the gate overlap has been proven to be much higher than in bulk systems [13]. This inversion condition is never reached here and only BTBT through the Si-InAs heterojunction ("point tunneling") contributes to the current in Fig. 5(a). This can be further seen in the BTBT generation rate computed from Eq. (3) and shown in Fig. 7(a): at low gate voltages BTBT is due to electron transitions between the Si and InAs sides. At higher gate voltages in Fig. 7(b), BTBT is mainly located on the InAs side. No BTBT perpendicular to the gate under the overlap region can be identified.

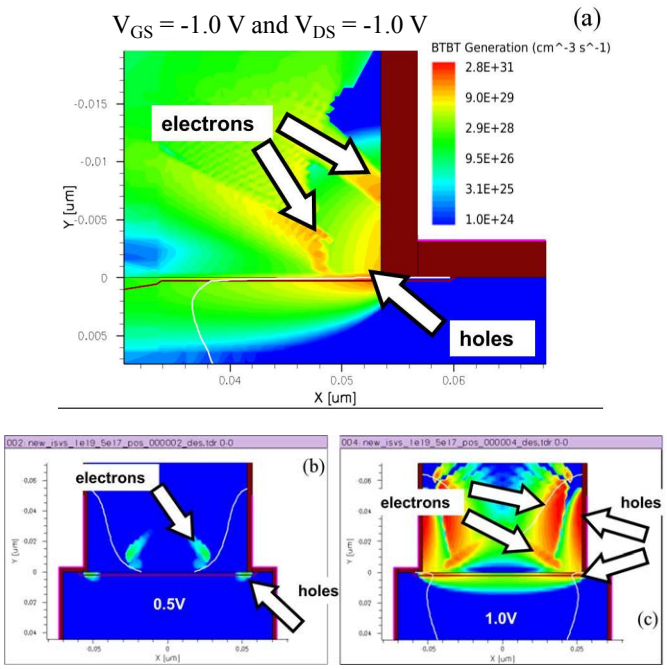

Fig. 6. Generation rate distribution in a real-size InAs-Si p-TFET without (a) and with (b)-(c) gate overlap.

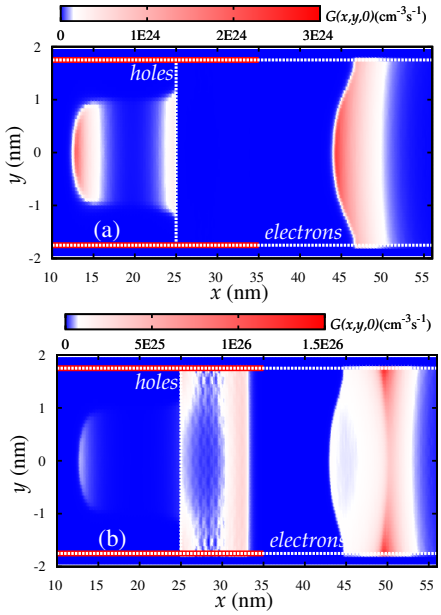

Fig. 7. Generation rate distribution in an extremely narrow InAs-Si p-TFET with 10 nm gate overlap at (a) $V_{\mathrm{G}} = -0.35\,\mathrm{V}$ and (b) $V_{\mathrm{G}} = -0.55\,\mathrm{V}$ with an applied $V_{\mathrm{DS}} = -1.0\,\mathrm{V}$. The electrostatic potential obtained from OMEN is used as input in Eq. (3). Horizontal and vertical white lines delimit the nanowire/oxide and hetero-junction interfaces, respectively. The top and bottom red lines show the gate location.

V. Conclusion

We have simulated ultra-scaled and realistic InAs-Si hetero-TFETs. Our findings suggest that BTBT is mainly direct in this material combination. We have therefore shown that by providing the proper material parameters and electrostatic potential, the Flietner dispersion model together with the WKB approximation offers an accurate way to study extremely narrow InAs-Si nanowire TFETs. The material parameters have been extracted from the nanowire bandstructure obtained from a $sp^3d^5s^*$ tight-binding approach.

It has also been found that the gate overlap plays an important role in large-scale InAs-Si TFETs by allowing line tunneling under the gate contact, while it has no influence in extremely narrow devices. Based on the results presented here, we anticipate that the electrostatic potential calculated by a TCAD tool such as S-Device could be combined with the material parameters extracted from full-band atomistic simulations to investigate large InAs-Si hetero-TFETs with a high accuracy.

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