III-V heterojunction nanowire tunnel FETs monolitically integrated on silicon

K. E. Moselund, D. Cutaia, H. Schmid, M. Borg, S. Sant, A. Schenk and H. Riel

***Abstract*— In this presentation we will discuss our recent progress on the integration of InAs/Si p-tunnel FETs (TFETs) and InAs/GaSb n-TFETs on SOI wafers. Local III-V growth is enabled by the development of Template-Assisted Selective Epitaxy (TASE) [1-4]. Both polarity devices have scaled geometries with cross-sections on the order of 30nm. The p-channel InAs/Si TFETs are developed based on our previously demonstrated vertical devices, which are now implemented horizontally in-plane on the Si wafer. The InAs/Si TFETs show excellent performance with I_{on} of about 4μA/μm at V_{GS} = V_{DS} = -0.5V, combined with average subthreshold swings (SS) of 70-80mV/dec. The SS is limited by trap mechanisms at the heterojunction, which will also be discussed. The InAs/GaSb n-TFETs represent our first devices in this material system, with doping levels and gate stack not yet optimized; the all III-V TFETs show about an order of magnitude greater current levels, but at a worse SS.**

I. Introduction

Tunnel FETs (TFETs) are a candidate for ultra-low power logic, due to their potential for achieving a subthreshold swing which is steeper than the sub-thermionic limit of MOSFETs, i.e. less than 59.5 mV/dec at 300K. Experimentally, devices sustaining a sub-60mV/dec slope over several decades and at reasonable current levels are still missing. As has recently been investigated by several groups [5-6], different types of material defects play a large role, and the reduction of defect densities is crucial to achieve the promises of TFETs. Pure Si-based complementary TFETs and inverters have been demonstrated [7]. However, the in-direct and large bandgap of Si ultimately limits the tunneling efficiency, and achieving simultaneously high current and steep slope will likely require the use of a heterostructure, which may well consist of Si on one side.

The need for heterostructures complicates matters from an integration perspective for a TFET, because different material combinations within each device will be required for the n- and p-channel device respectively. Even if operating in a common materials system like InGaAs/GaAsSb, which can be used to realize both types of devices, the different band alignments will require separate growth runs in the case of p- and n-channel TFETs. To the best of our knowledge there are only two reports on III-V based complementary TFET technologies. The first one from R. Pandey et al. [8], where InGaAs/GaAsSb mesa structures are integrated on an InP substrate using a metamorphic buffer. And the second one, the work from our group [9] which allows for the integration of scaled InAs/Si p-TFETs and InAs/GaSb n-TFETs in-plane on SOI, a schematic of this concept is shown in Fig.1. Presently, n- and p-channel devices are processed in a compatible process flow, but on separate chips for ease of processing.

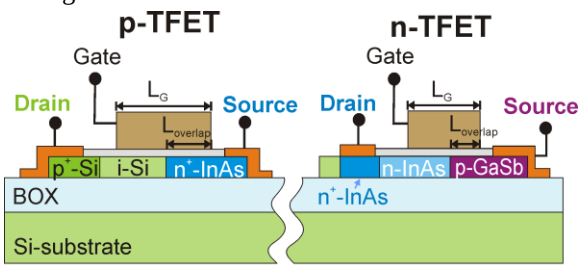

Fig. 1 Schematic showing the integration scheme of p- and n-channel TFETs. Presently fabricated devices are implemented on different substrates, but as seen in Fig. 3 the process flows are fully compatible.

II. III-V Growth and Device Fabrication

The III-V material is integrated monolithically on (100) SOI wafers, using Template-Assisted Selective Epitaxy (TASE) [1-4]. In TASE the III-V material is grown within a confined oxide nanotube which governs geometry and prevents junction overgrowth. Fig. 2 shows a top-view SEM image, of multiple Si/InAs nanostructures in parallel, to illustrate the uniformity of this growth approach.

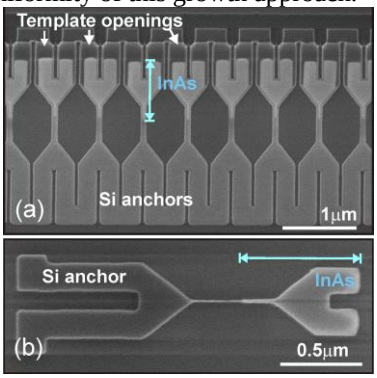

Fig. 2 Top-view SEM image of (a) several parallel InAs/Si nanostructures, while the oxide template is still on, illustrating the uniformity of the InAs growth. (b) A single InAs/Si structure after stripping the oxide template, showing the P+ doped Si anchor which serves as drain, the n+ InAs source region, and the narrow undoped Si channel in between.

A schematic of the process flow is shown in Fig. 3. The main difference between p-TFETs and n-TFETs is that for the p-TFETs, a boron diffusion doping is carried out in the drain regions (P^+) of the SOI substrate before template formation. Thus for the p-TFET the Si layer on the SOI wafer is part of the active device, whereas for the n-TFETs the Si

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serves as nucleation layer only. Fig. 4 shows a top-view and cross-sections of the individual material regions for both p- and n-TFETs. Taking into account both the average cross-section and the Ω-gate geometry, we use an effective width of 100 nm for normalization purposes in all cases.

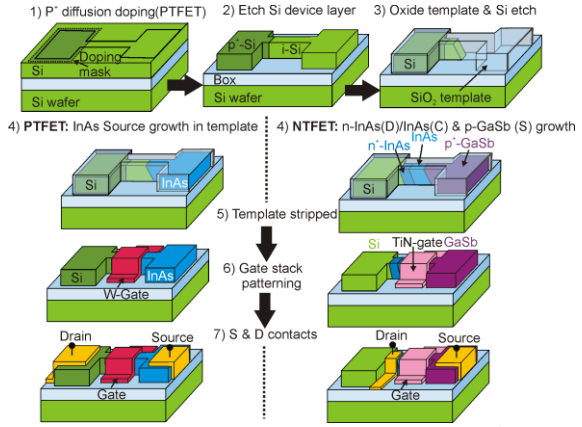

Fig. 3 Schematic of process flow. For the p-TFET a P^+ diffusion of boron is done to define the drain region. The device structures are defined by E-beam lithography and dry etching, and coated by an oxide layer, which is opened at one end to create the template. The Si is etched back in TMAH, and the III-V materials regrown. A gate stack is deposited (EOT ~1.75nm) and patterned, and at last contacts are deposited by lift-off

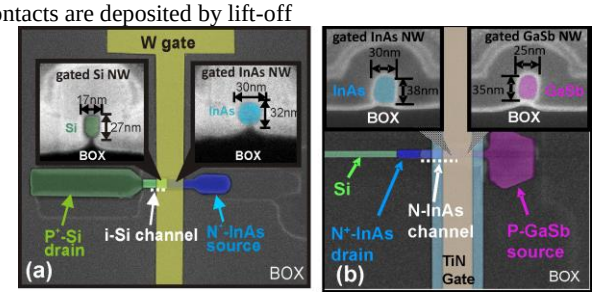

Fig. 4 Top-view before contacting as well as cross-sections (insets) of the different material regions for the (a) p-TFET, and (b) n-TFET.

III. ELECTRICAL CHARACTERIZATION

Transfer characteristics are shown for both types of devices in Fig. 5 for temperatures (T) ranging from 125K to 300K. I_{on} is relatively independent of T whereas the SS shows a strong dependence for both devices. The combination of a high trap density at the heterojunction and a fairly long gated i-Si region means that the TAT process acts as a current source generating electron-hole pairs, whose passage through the channel is controlled by a thermionic barrier. This results in the MOS-like T-dependence.

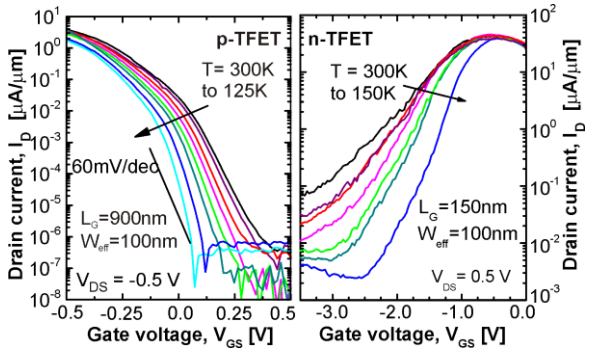

Fig. 5 Transfer characteristics for p- and n-TFETs for different temperatures.

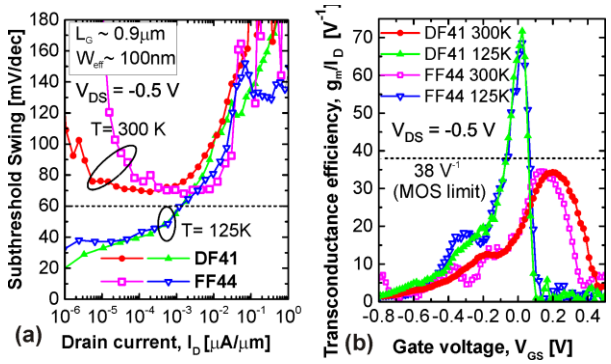

Fig. 6 (a) SS vs. I_D and (b) g_m/I_D as a function of V_{GS}, for two different InAS/Si p-TFETs, DF41 and FF44 are simply the device labels.

Fig 6. shows SS and transconductance efficiency for two different InAs/Si p-TFETs, demonstrating average slopes of 70-80 mV/dec depending on the interval, and a g_m/I_D peak of $34V^{-1}$ just short of the $38V^{-1}$ MOS limit.

IV. CONCLUSION

We have demonstrated p- and n-channel TFETs monolithically integrated on a SOI substrate using compatible process flows. InAs/Si p-TFETs show excellent performance with I_{on} of a few μA/μm and average slopes of about 70-80 mV/dec.

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