InAs/Si heterojunction nanowire tunnel FETs monolithically integrated on silicon
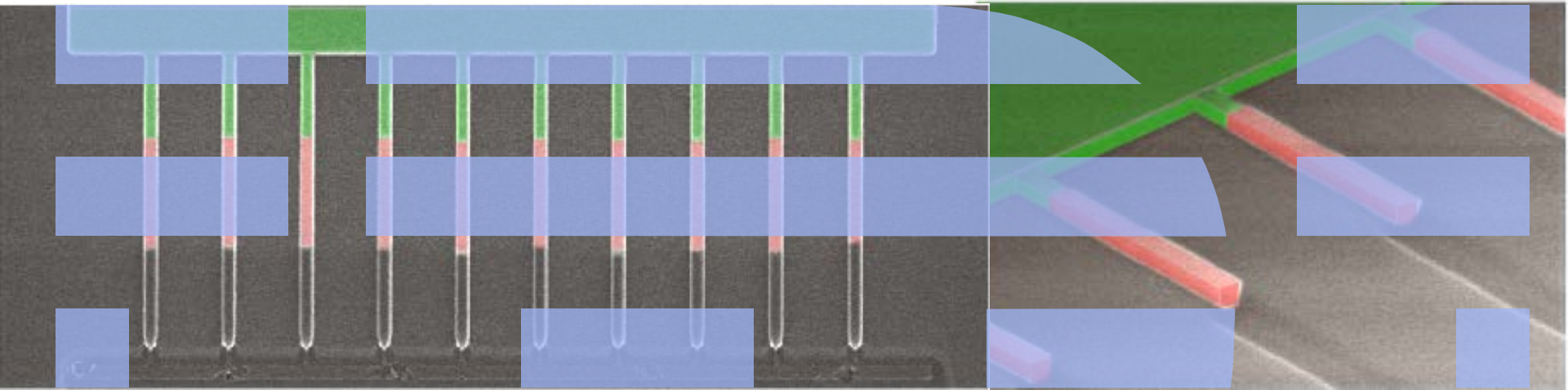
K. Moselund[1], D. Cutaia[1]. M. Borg[1], H. Schmid[1], S. Sant[2], A. Schenk[2] and H. Riel[1]

[1]IBM Research – Zurich, Switzerland
[2] ETH Zurich, Integrated Systems Laboratory

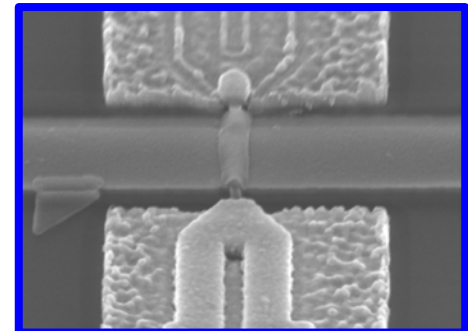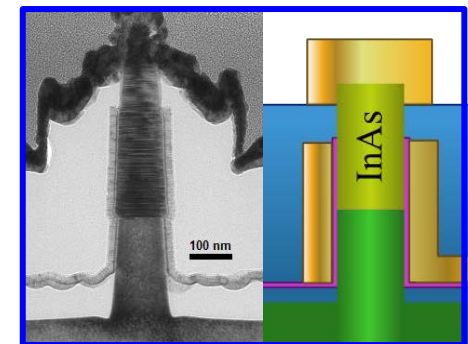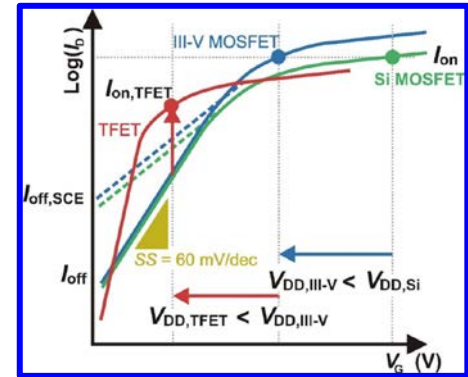IBM Research – Zurich   Kirsten Moselund, ICONN Canberra, 09.02.2016

Outline

- ## Motivation & background
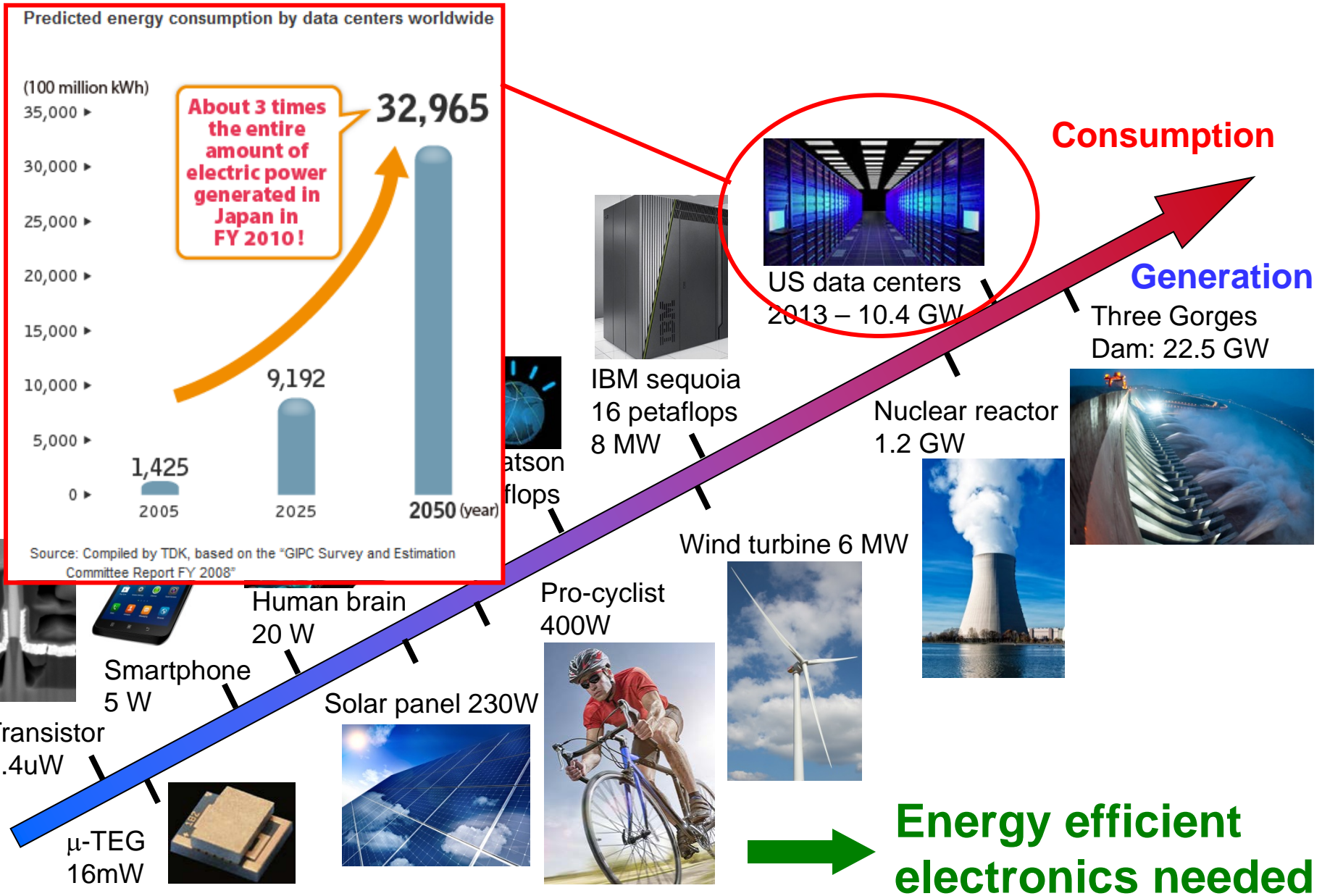 - Low power electronics
  - SOA Tunnel FETs

- ## InAs/Si NW tunnel FETs
  - Functionality
  - Template Assisted Selective Epitaxy
  - Device fabrication & characterization

- ## Analysing the results
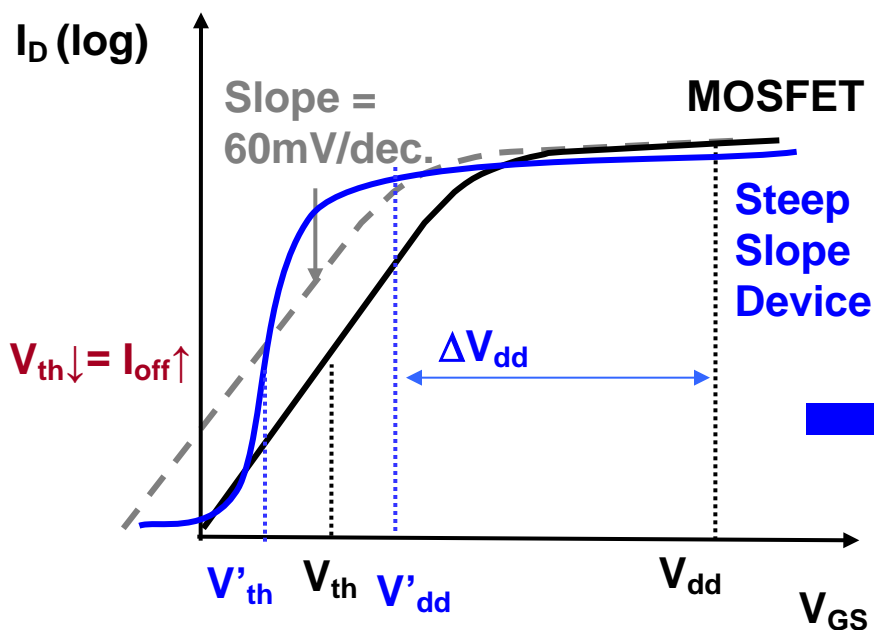 - TFET simulations
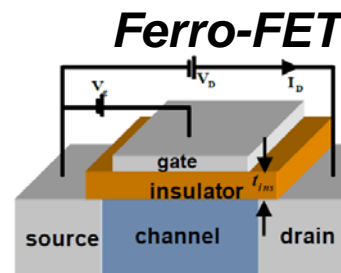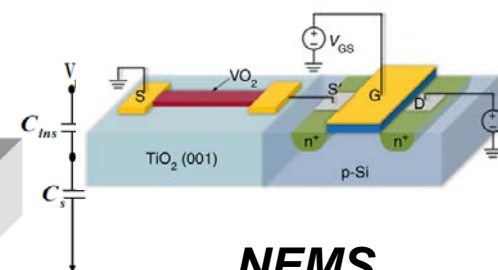 - Optimizing the device

- ## Outlook & Summary

The power challenge

IBM

Predicted energy consumption by data centers worldwide

(100 million kWh)

About 3 times the entire amount of electric power generated in Japan in FY 2010!

32,965

9,192

1,425

2005   2025   2050 (year)

Source: Compiled by TDK, based on the "GIPC Survey and Estimation Committee Report FY 2008"

Consumption

US data centers
2013 – 10.4 GW

Generation

IBM sequoia
16 petaflops
8 MW

Three Gorges
Dam: 22.5 GW

Nuclear reactor
1.2 GW

Wind turbine 6 MW

atson
flops

Human brain
20 W

Pro-cyclist
400W

Smartphone
5 W

Solar panel 230W

Transistor
0.4uW

μ-TEG
16mW

**Energy efficient
electronics needed**

3

Low power electronics

$$P_{tot} \approx \underbrace{C \cdot V_{dd}^2 \cdot f(V)}_{active} + \underbrace{I_{Leak} \cdot V_{dd}}_{leakage}$$

➡ Reduce I_{Leak}, Reduce V_{dd}

I_D (log)

Slope = 60mV/dec.

MOSFET

Steep Slope Device

$V_{th}\downarrow = I_{off}\uparrow$
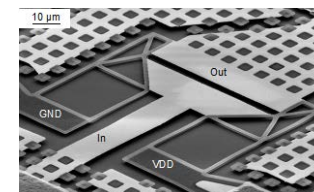
ΔV_{dd}
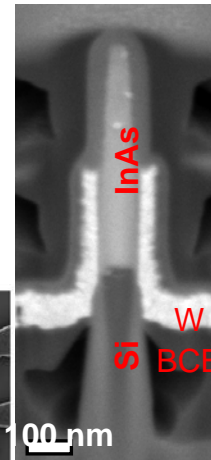
V'_{th} V_{th} V'_{dd}

V_{dd}

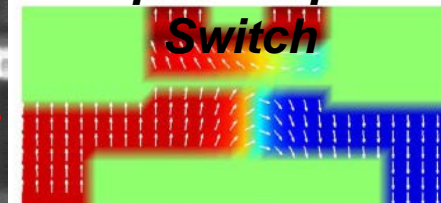V_{GS}

Steep subthreshold slope
➔ can decrease V_{th} to reduce V_{dd}

Phase transition

Ferro-FET

gate
insulator
source channel drain

C_{Ins}
C_s

V_{GS}

VO_2

TiO_2 (001)

n^+ n^+ p-Si

NEMS

10 μm

Out
GND
In
VDD

Tunnel FET

InAs

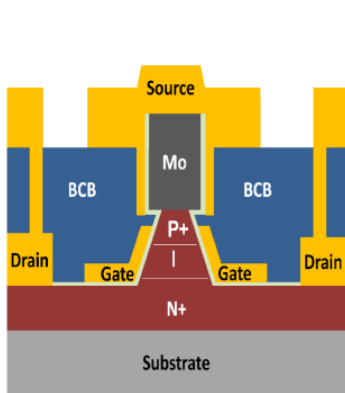W
Si BCB

100 nm

GNR FET
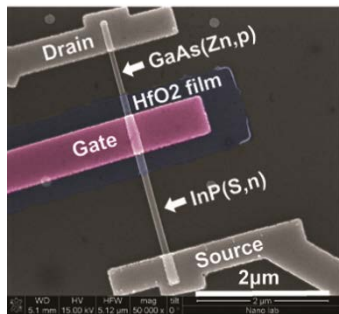
Spin Torque Switch

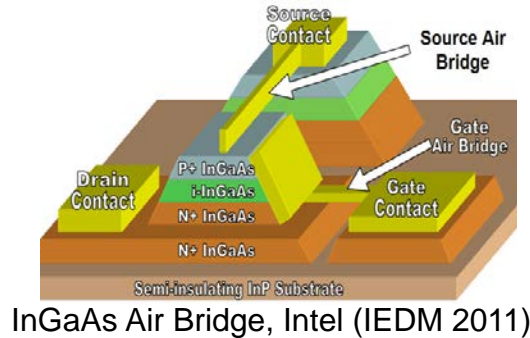Domain wall switching
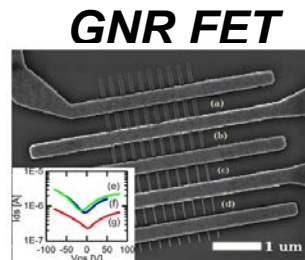
State of The Art Tunnel FETs

- Many different implementations (geometry, materials etc.) reported so far
- Varying potential for: High I_{on}, low SS, integration potential (Complementary C-TFET), scalability.
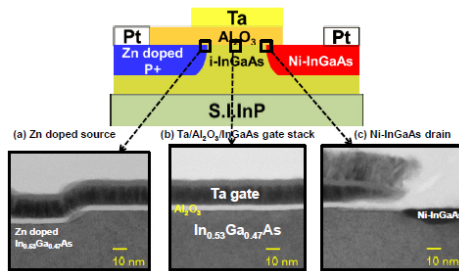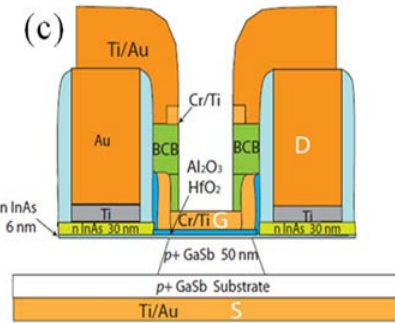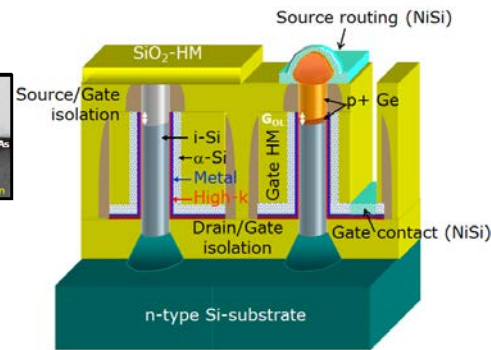

InGaAs mesa,
Penn state (DRC2011)

InGaAs Air Bridge, Intel (IEDM 2011)

InAs/GaSb mesa,
Notre Dame(IEDM 2012)

s-SiNW on SOI (inverters),
FZ Julich (IEDM 2013)

GaAs/InP NW Lund (ACS Nano 2012)

Planar Zn-diffused InGaAs,
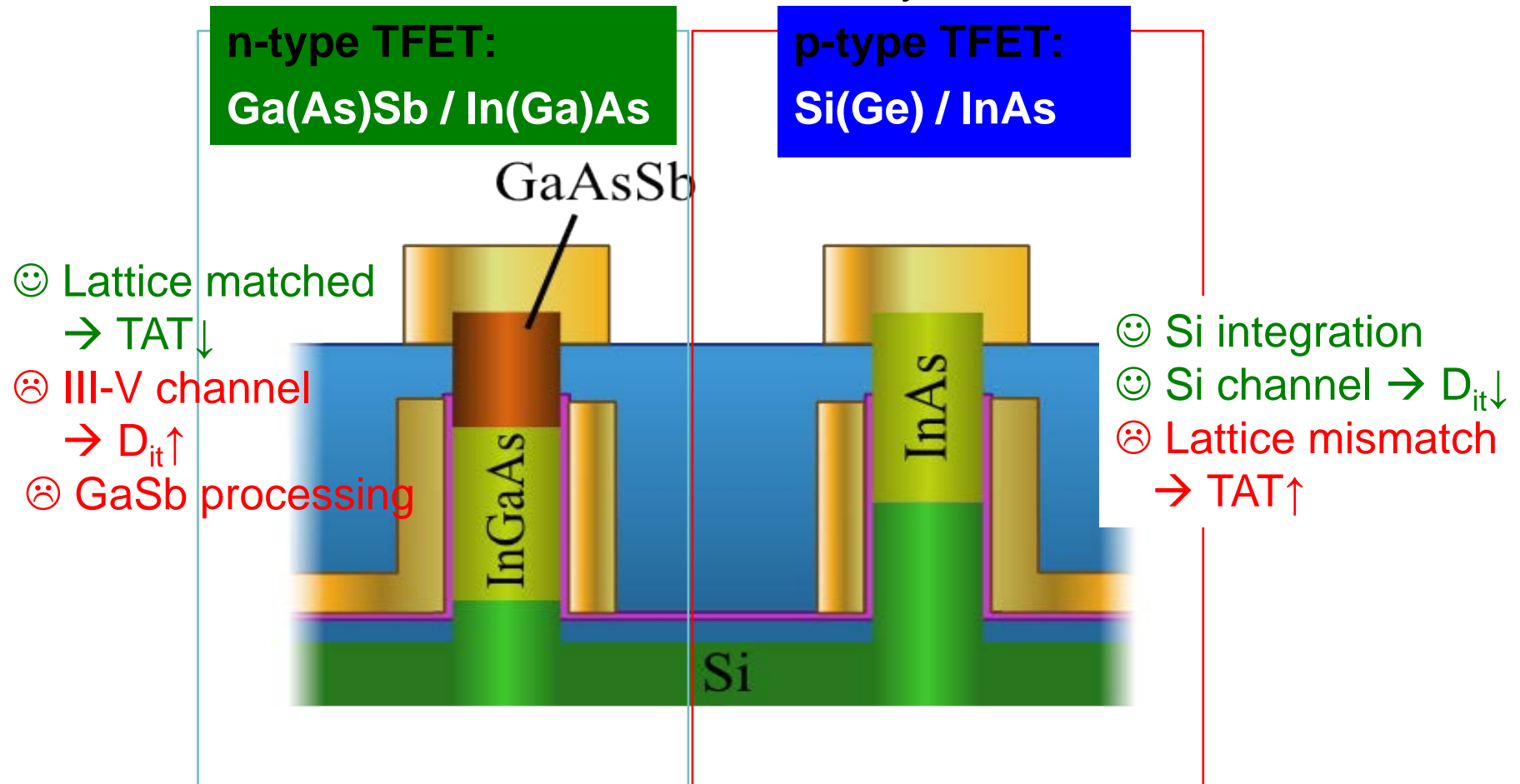Tokyo University(IEDM 2013)

Vertical Si-Ge NW,
IMEC (IEDM 2013)
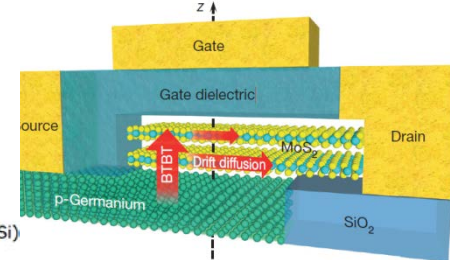
3D-2D TFET: MoS_2 & Ge,
UCSB (Nature 2015)
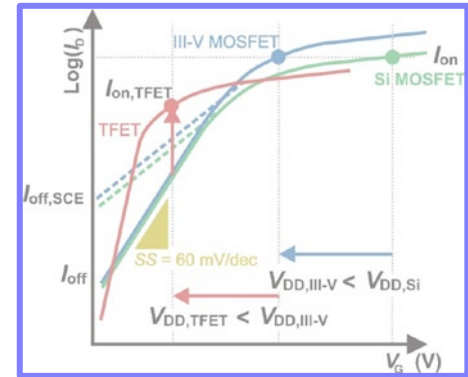
IBMs approach to TFETs

Develop a III-V device platform on Si

- **Complementary TFET technology** based on III-V NW heterostructures
- Goal: **high I_{on}** & **low I_{off}** & **steep slope** in one device
- Scalable – device dimensions and density

n-type TFET:
Ga(As)Sb / In(Ga)As

p-type TFET:
Si(Ge) / InAs

GaAsSb

InGaAs

InAs

Si

☺ Lattice matched
  → TAT↓
☹ III-V channel
  → D_{it}↑
☹ GaSb processing

☺ Si integration
☺ Si channel → D_{it}↓
☹ Lattice mismatch
  → TAT↑

Outline

- Motivation & background
  - Low power electronics
  - SOA Tunnel FETs

- InAs/Si NW tunnel FETs
  - Functionality
  - Template Assisted Selective Epitaxy
  - Device fabrication & characterization

- Analysing the results
  - TFET simulations
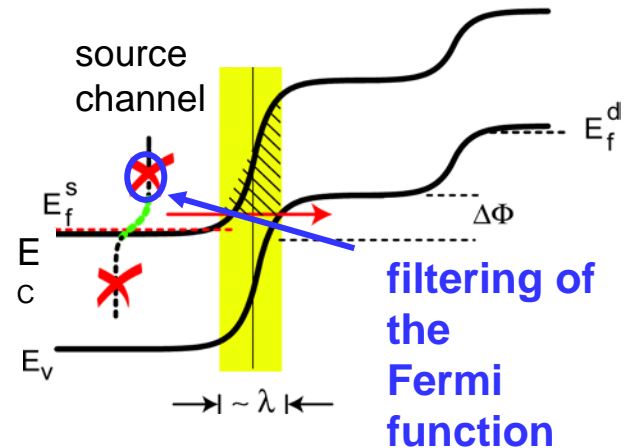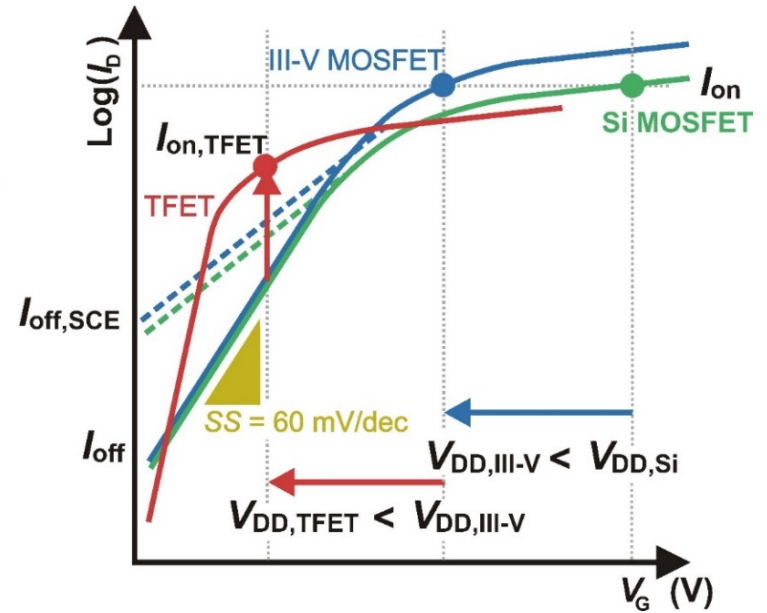 - Optimizing the device

- Outlook & Summary
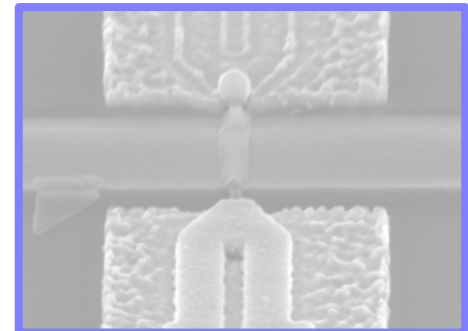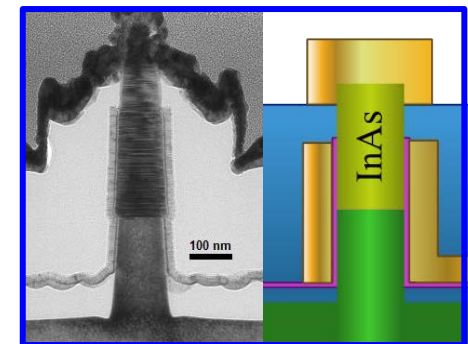
Tunnel FET functionality

- Steep slope ➔ V_{dd} scaling and low I_{off}
- Potential to achieve ultra-low power operation
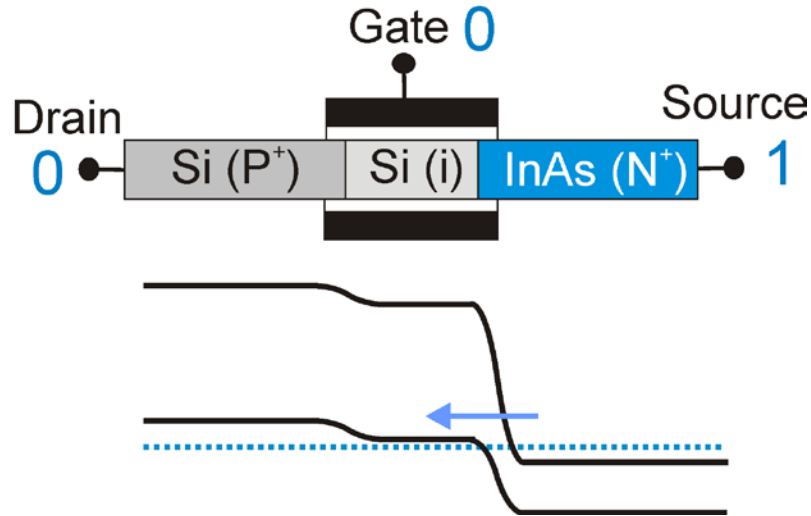
Band-to-band-tunneling (BTBT) acts as bandpass filter
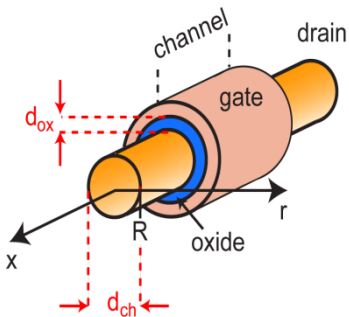cutting off the tails of the Fermi distribution
➔ **SS < 60 mV/dec possible**

$$I_{on} \sim T_{tunneling}^{WKB} = \exp\left(-\frac{4\lambda\sqrt{2m^*}\,E_G^{3/2}}{3qh(\Delta\Phi + E_G)}\right)$$
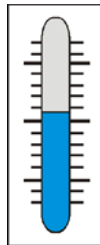
Increasing Ion

λ: Electrostatics $\rightarrow$ NW, high-k, doping profiles

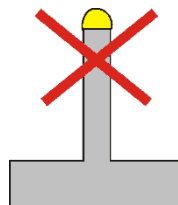E_g, m^*: materials based $\rightarrow$ Ge/InAs source on Si, III-V heterostructures
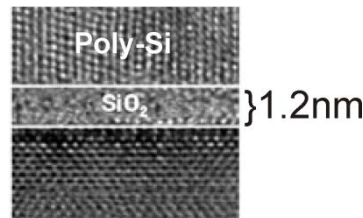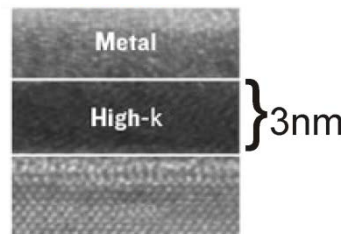
GAA

Abrupt doping

High-k

III-V

hetero-structures

Low thermal budget

No catalyst

Late 1990's

Poly-Si

SiO$_2$ }1.2nm

2003

Metal

High-k }3nm

InAs

Si

9

IBM
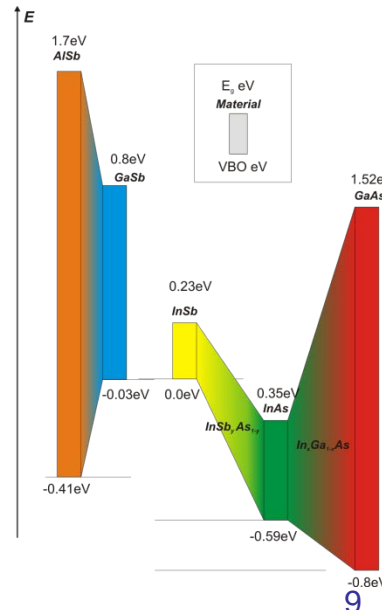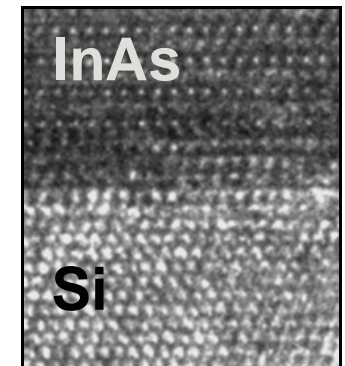
Growth on any crystalline orientation

a b c d 200 nm e 50 nm

III-V

Si(100) (110) (111) (112) nc-Si
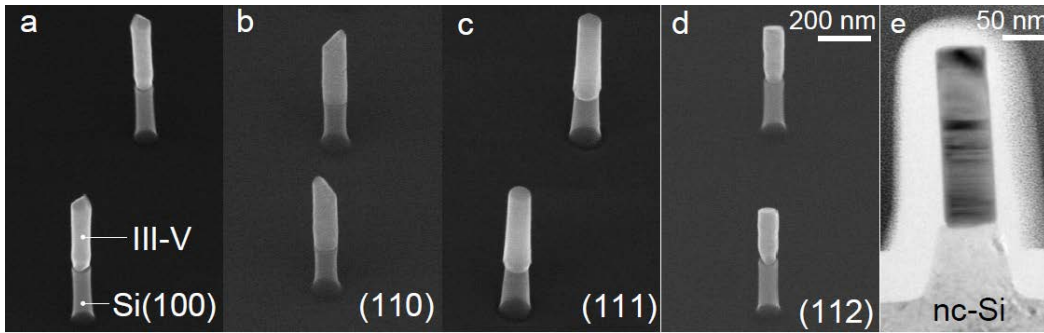
✓ **Enables VLSI integration**

Stacked nanowires

500 nm

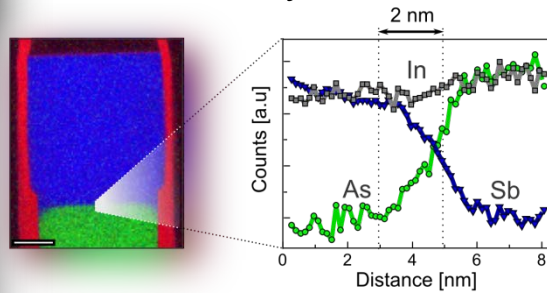Si III-V Si GaAs

100 nm
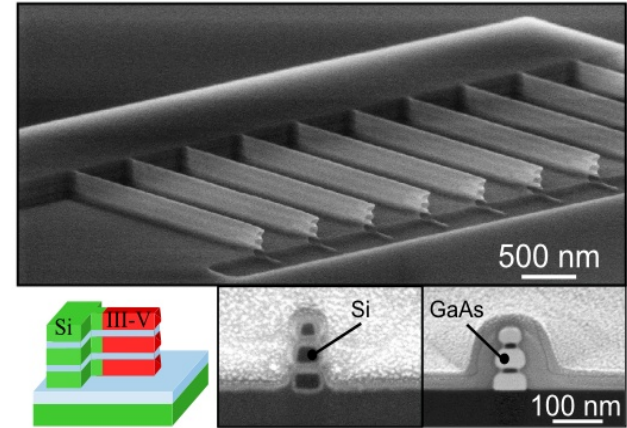
✓ **Scalable Technology**

Abrupt junctions
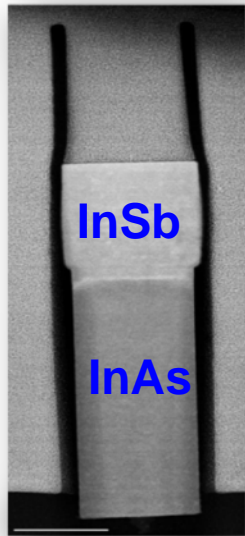
Chemical Analysis: EELS, EDX

InSb

InAs

2 nm

In

As Sb

Counts [a.u]

Distance [nm]
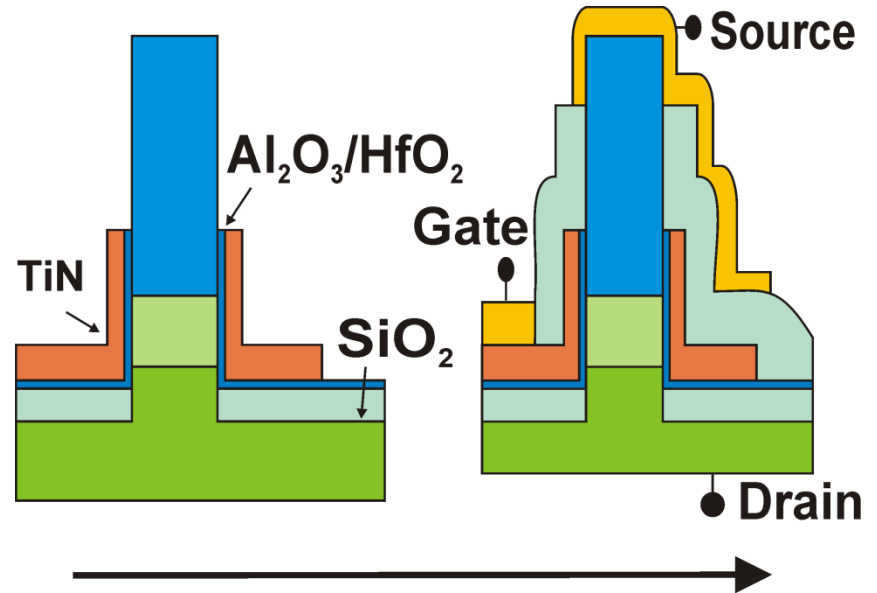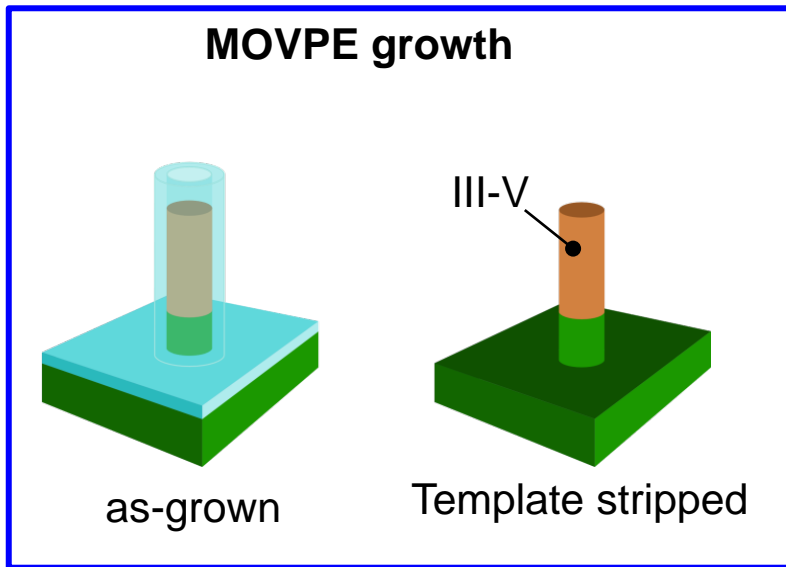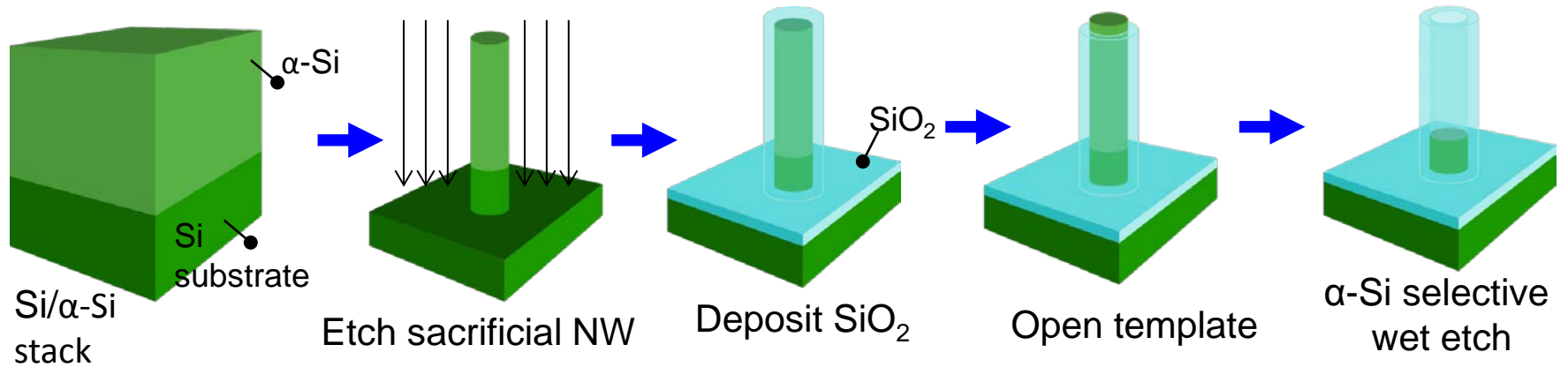
Courtesy of L. Gignac, IBM Yorktown.

✓ **Requirement for Steep slope**

Large arrays

GaAs

200 nm

P. D. Kanungo et al. Nanotechnology, 2013, M. Borg et al. Nanoletters, 2014. H. Schmid et al. APL 2015,
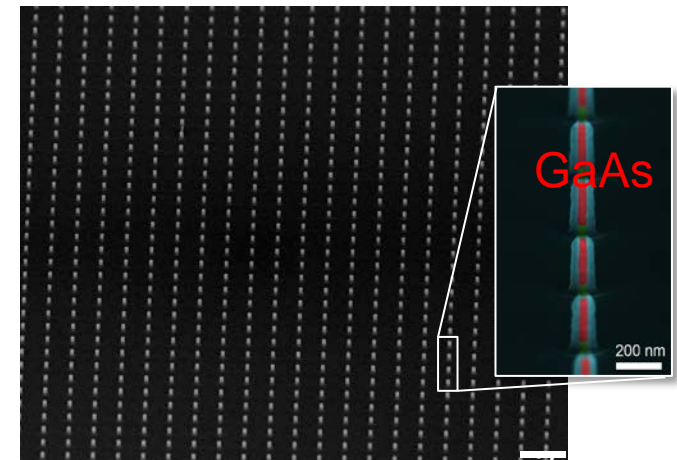
Vertical Implementation of TASE

Si/α-Si stack → Etch sacrificial NW → Deposit SiO$_2$ → Open template → α-Si selective wet etch

α-Si
Si substrate
SiO$_2$

MOVPE growth

as-grown   Template stripped

III-V

Al$_2$O$_3$/HfO$_2$
TiN
SiO$_2$
Source
Gate
Drain

Developing our InAs/Si TFET process

TEM: L. Gignac, J. Bruley, C. Breslin

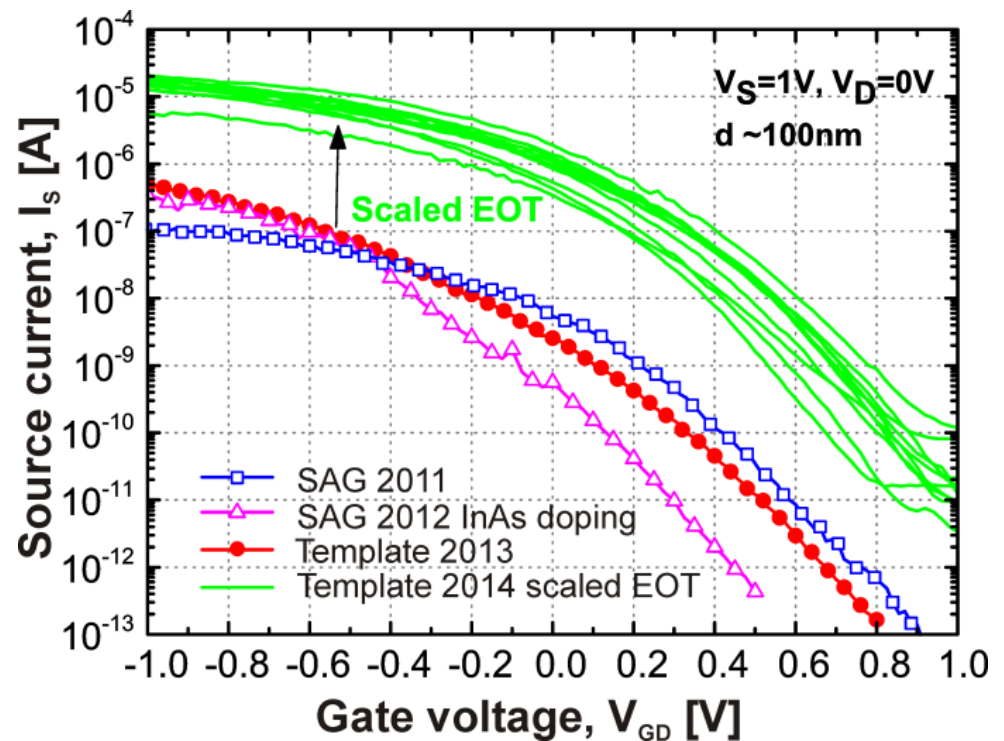SE-Process | Template-Process | Scaled Template

TASE
Scaled diameter
Metal ALD
Scaled EOT
TEOS
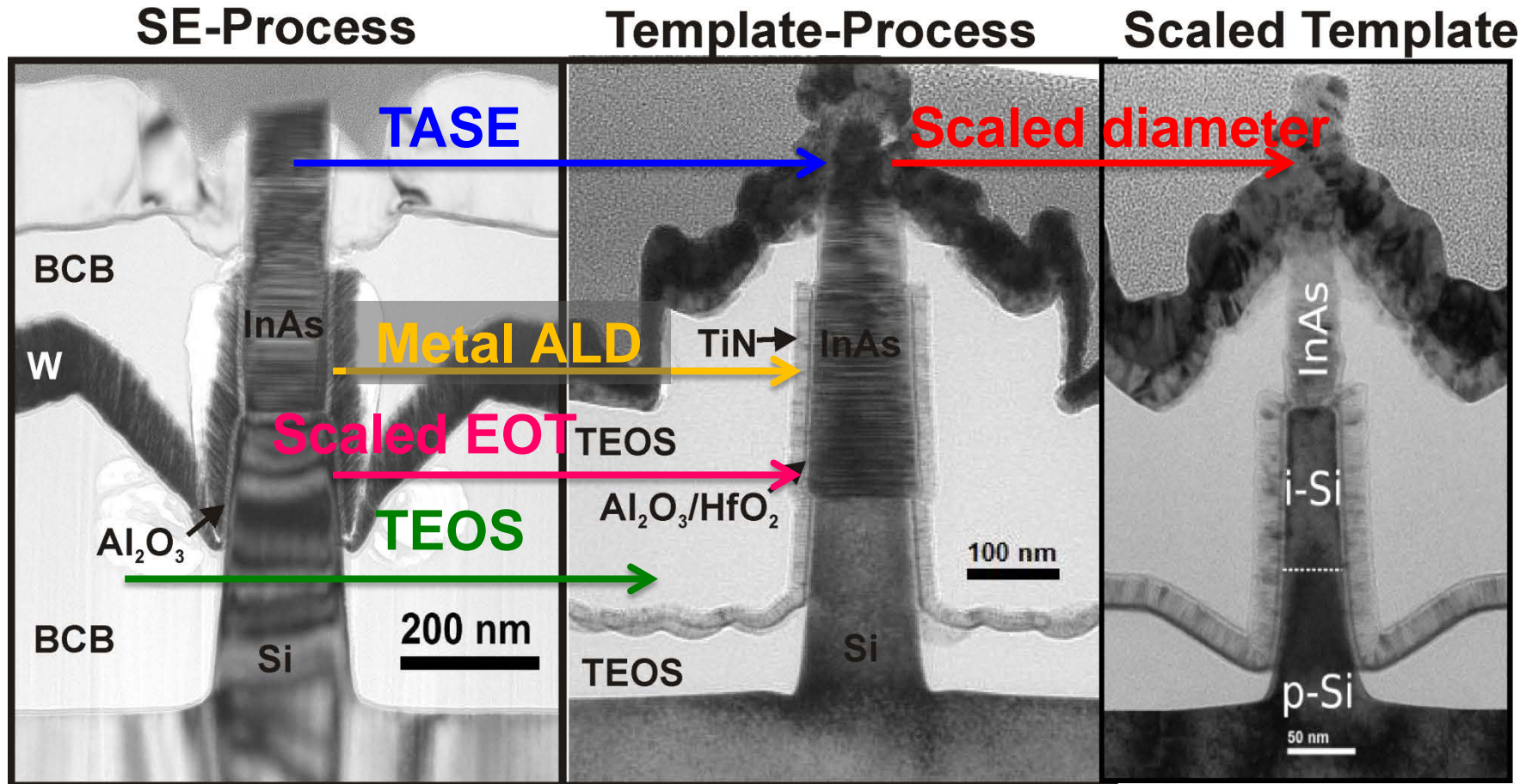
📖 K. Moselund, EDL 2012. H. Riel IEDM 2012. D. Cutaia, et al. J-EDS 2015, D. Cutaia, et al. ULIS 2015
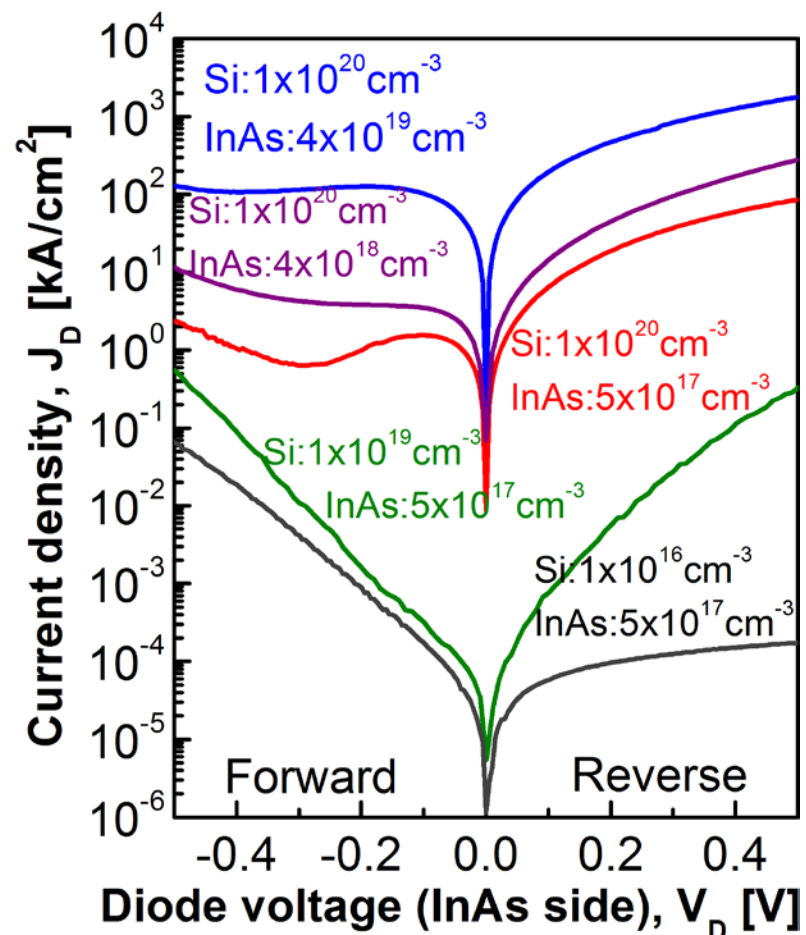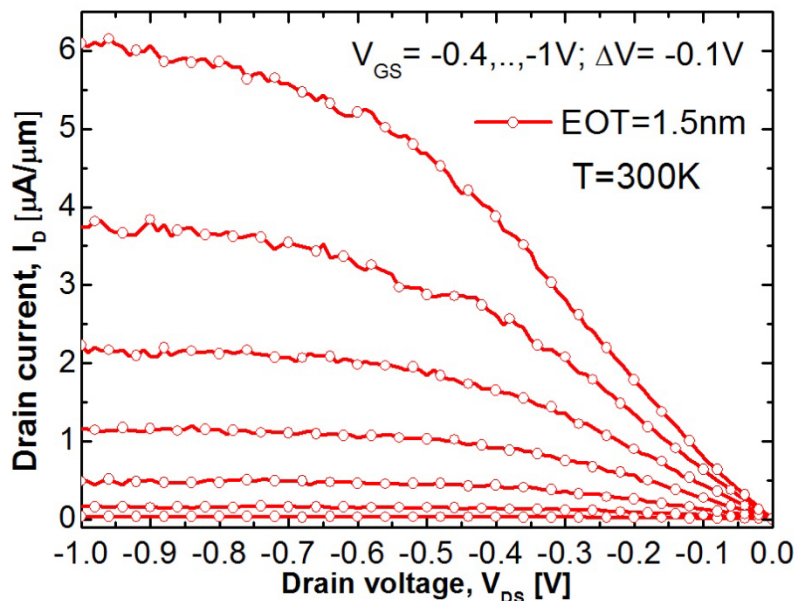
TFET transfer performance

- **TASE** →Improved device yield & reduced variability

- **EOT scaling** (2.7nm to 1.5nm)

  - I_{on} boosted by ~50x to 50 µA/µm

  - $I_{on}/I_{off} \approx 10^6$

  - SS_{ave}: 150–200 mV/dec
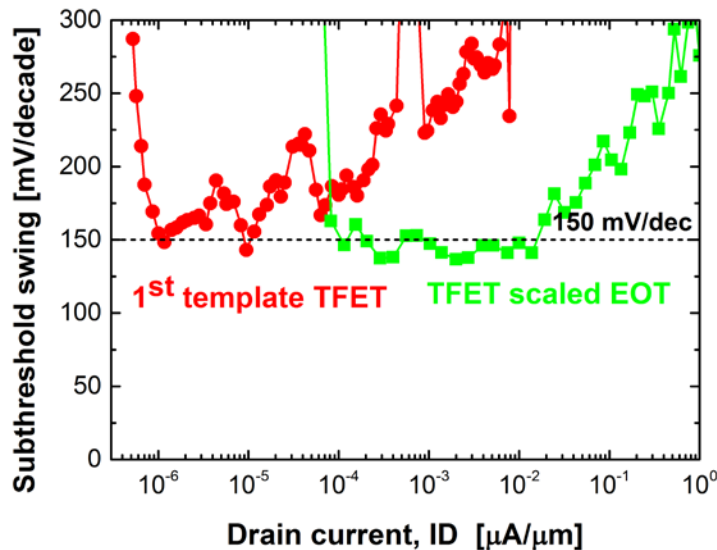
📖 D. Cutaia, ULIS & J-EDS2015

$I_D(V_{DS})$: Current saturation
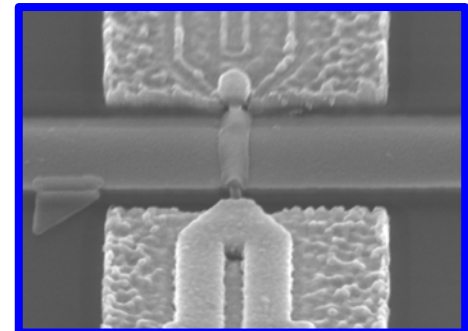
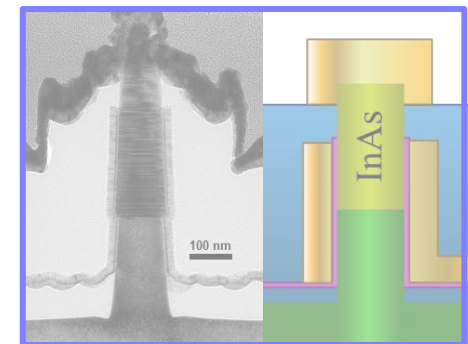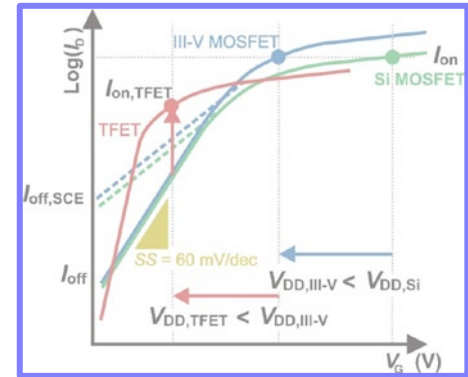- Good electrostatic control of i-Si/InAs heterojunction
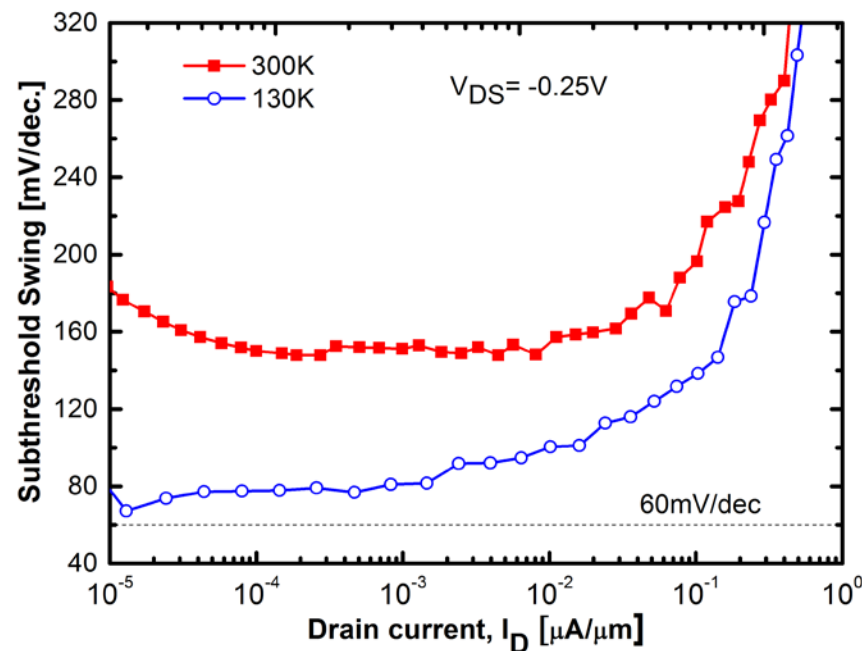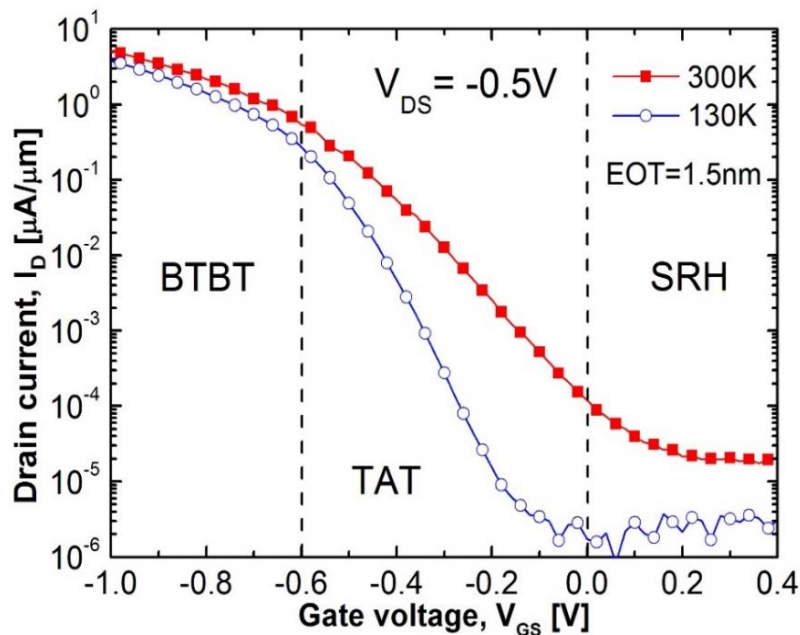
Outline

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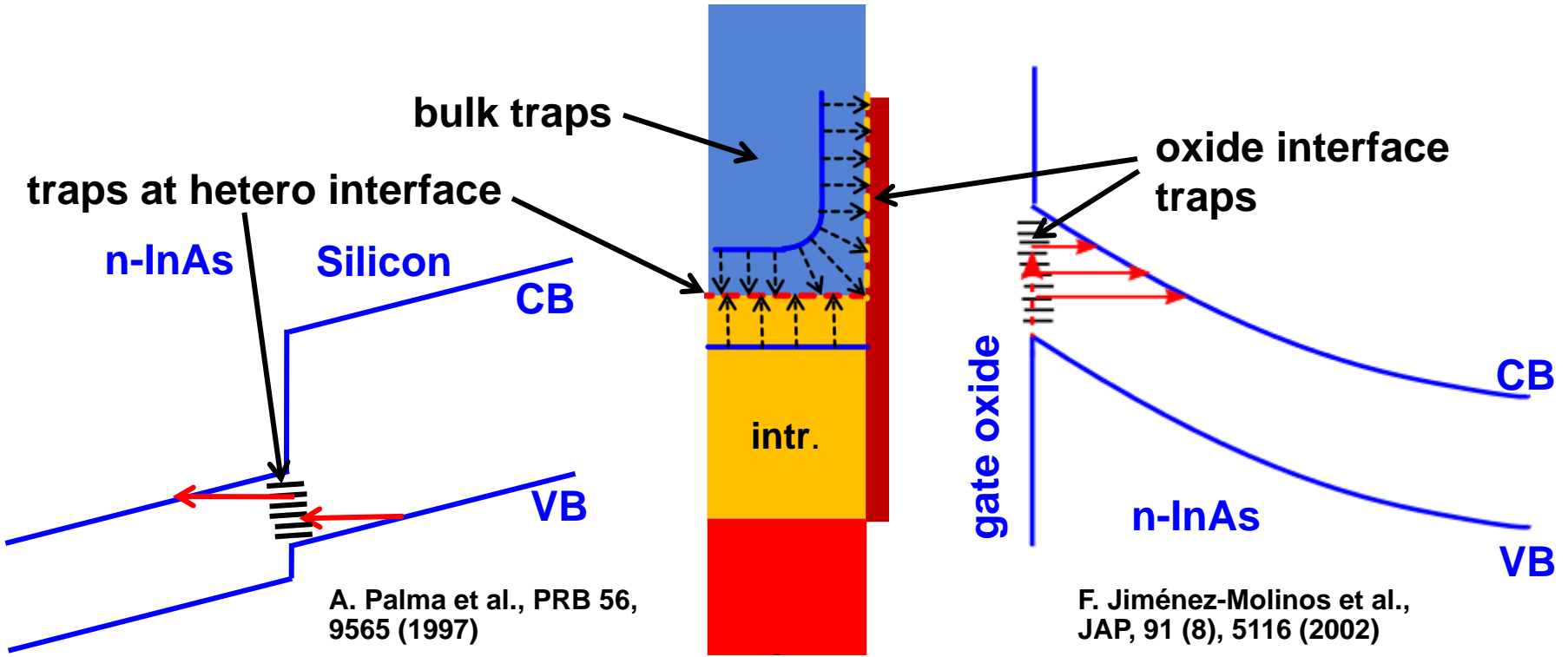- Analysing the results
  - TFET simulations
  - Optimizing the device

- Summary

- I_{on} maintained with decreasing temperature → expected TFET behaviour

- Activation energy analysis → BTBT dominates for V_{GS} < -0.6 V.

- SS reduced at low temperature

  → *SS* limited by traps: D_{it} at the dielectric interface & TAT heterojunction
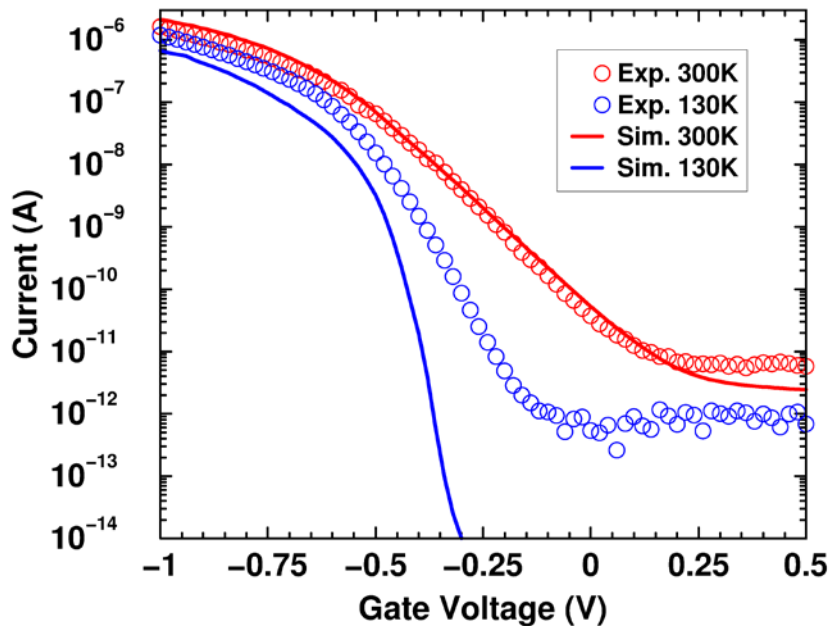
Effect of generation centers ("traps")

- Trap-assisted tunneling (TAT) can be seen as multi-phonon-assisted **trap-band tunneling** or as field-enhanced **multi-phonon generation**.

- Contribution from 3 kinds of traps: bulk, hetero interface, gate oxide interface
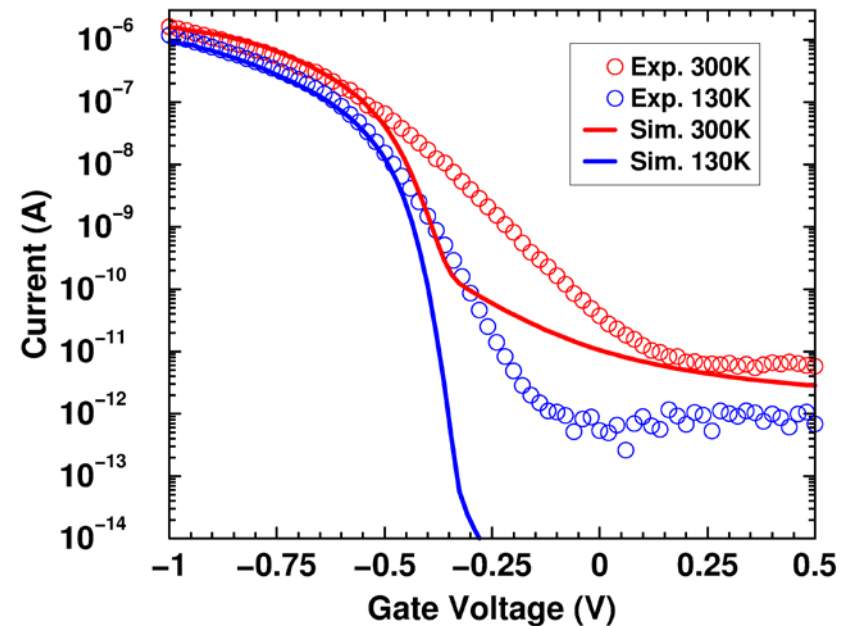

bulk traps

oxide interface traps

traps at hetero interface

n-InAs   Silicon

CB

VB

intr.

gate oxide

n-InAs

CB

VB

A. Palma et al., PRB 56, 9565 (1997)

F. Jiménez-Molinos et al., JAP, 91 (8), 5116 (2002)

📖 A. Schenk et al. ULIS 2015

oxide interface

**hetero interface**

📖 A. Schenk et al. ULIS 2015

- Two types of traps impact tunnel FETs

  - Oxide interface (like MOSFET) → D_{it}

  - Hetero interface, lattice mismatch → **TAT**

- Oxide interface traps dominant at 300K → need better gate stack

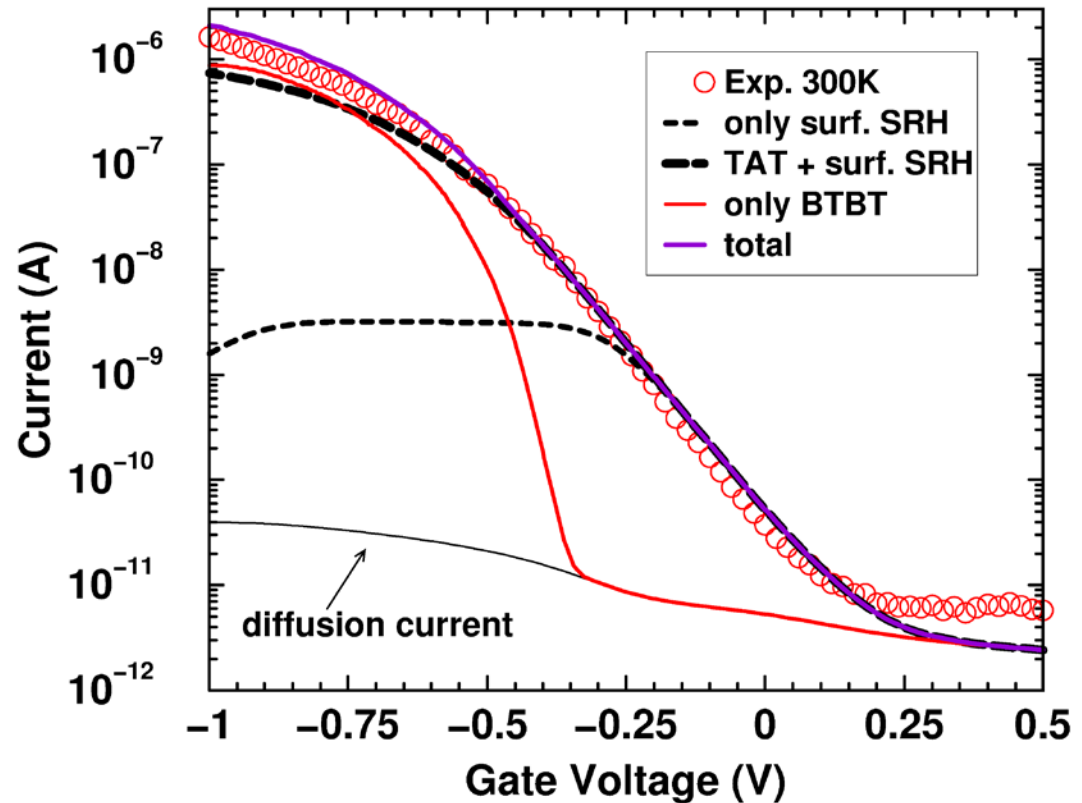- Hetero interface traps dominant at 130K → likely ultimate limitation

Predicting optimized TFET performance

Reproducing T-dependence:

- Oxide: D_{it} = 1e13 cm^{-2}eV^{-1}

- Junction: D_{it} = 7e12 cm^{-2}eV^{-1}
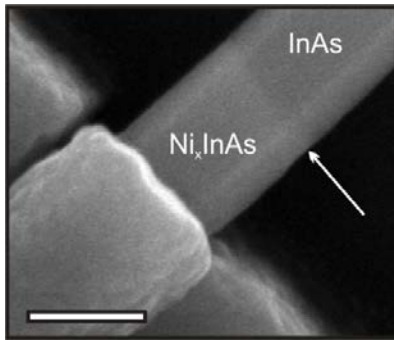
- Surface SRH generation + zero-phonon tunneling.
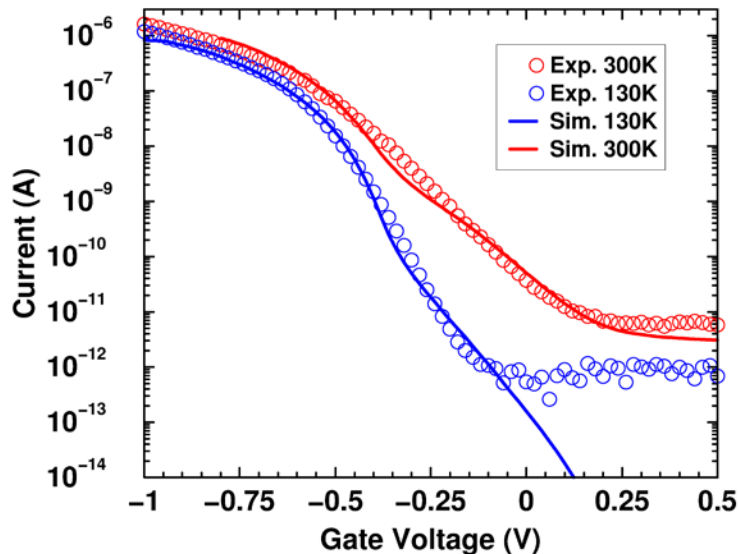
Without the contribution of traps a steep slope is achieved.

📖 A. Schenk et al. ULIS 2015
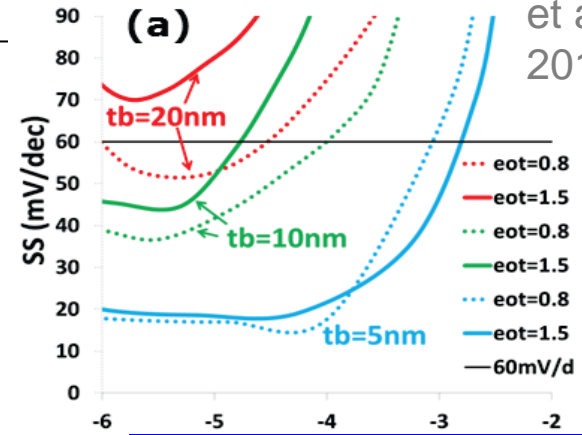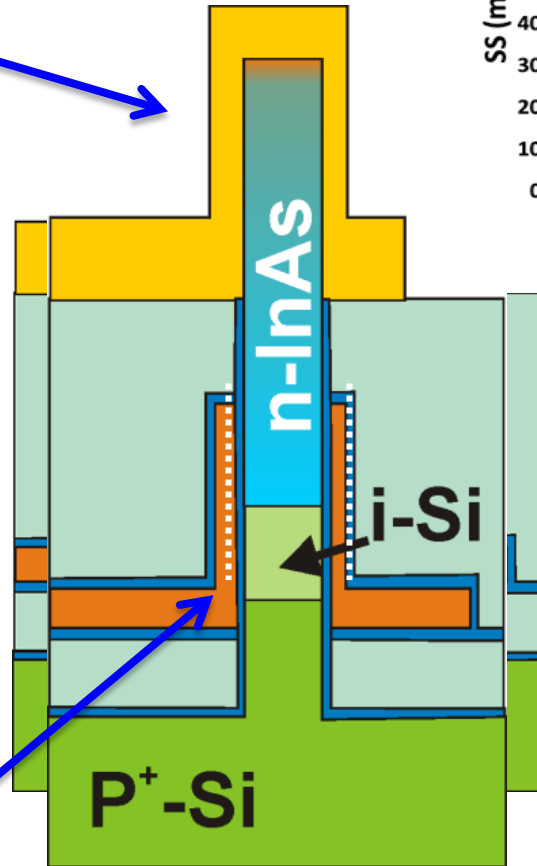
How to optimize the TFET

- Ni-alloying
  - → Decreases $R_{contact}$

✓ **Improve I_{on}**

Improved gate stack
- EOT scaling
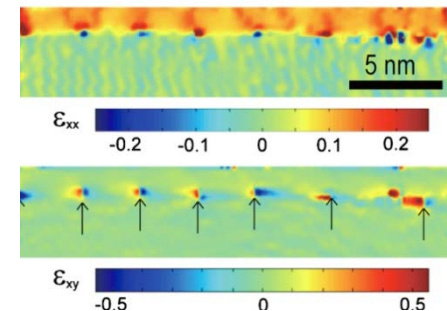- → improves I_{on}
- Reduce Dit by forming gas anneal

✓ **Steeper Slope**

✓ **Steeper Slope**

Scale down dimensions
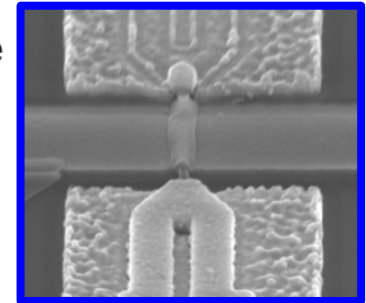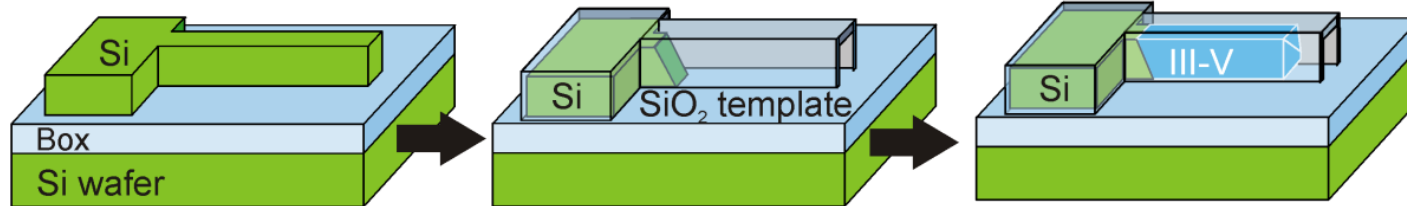- Electrostatics improve
- → Key to steep slope
- Defects caused by lattice mismatch should diminish with dimensional scaling

IBM Research – Zurich   Kirsten Moselund, ICONN Canberra, 09.02.2016

Implementing changes – lateral TASE TFET

lateral - Template Assisted Selective Epitaxy

1) Etch Si device layer 2) Oxide template & Si etch 3) III-V growth in template
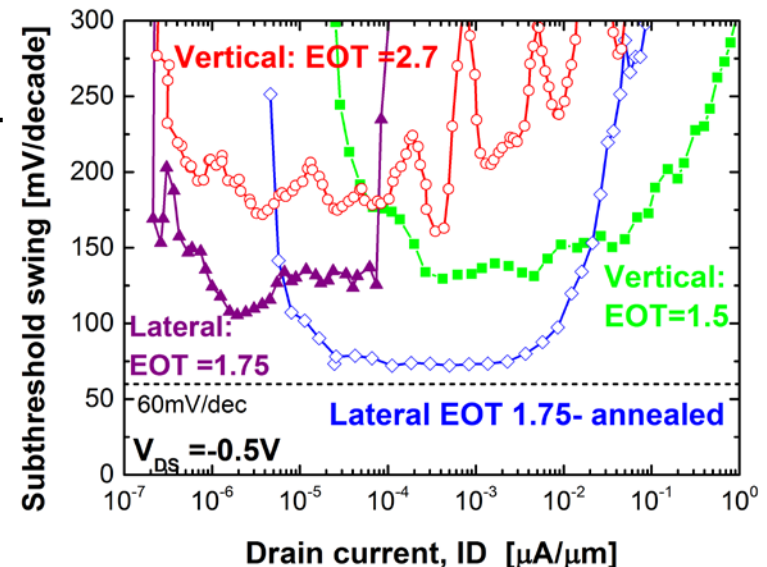

Advantages:
- Lateral → first step towards VLSI TFET
- Device parameters (L_G, L_i, W) may be varied freely in design.
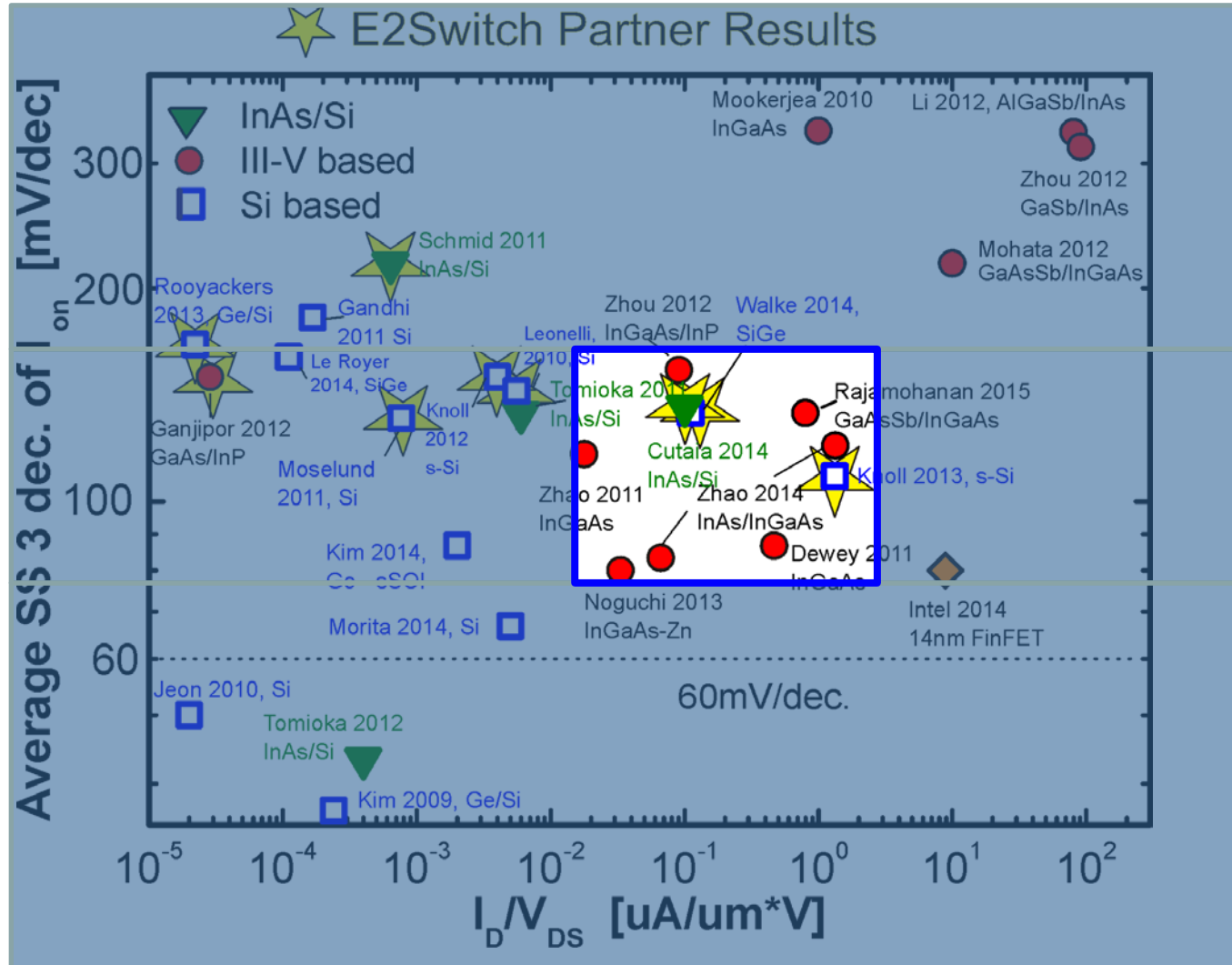- Scalability more easily achieved

Results:
- Substantial improvement achieved in SS_{ave} (~70mV/dec) due to **scaled geometry** (~30nm) & **improved gate stack.**

Submitted to VLSI symp. 2016
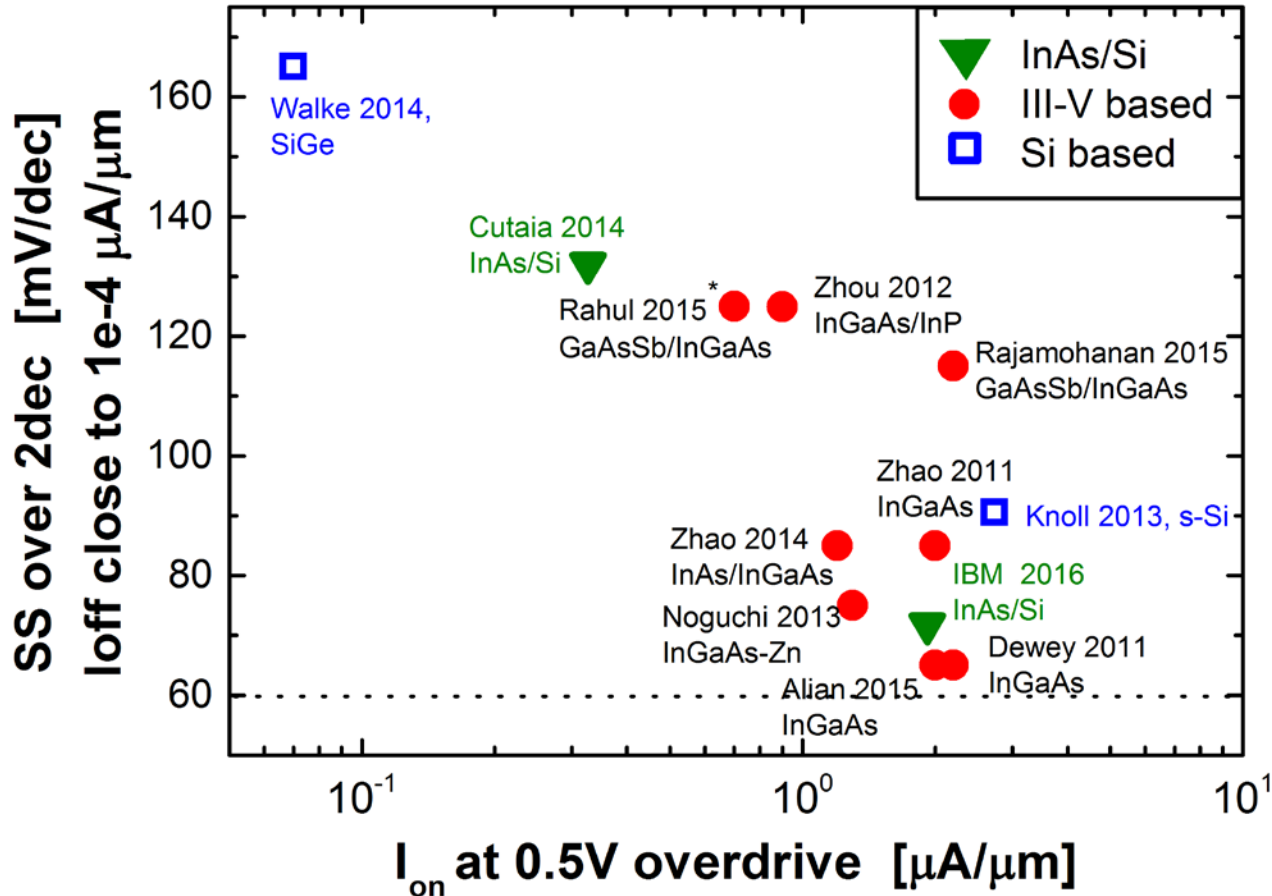
- Trade-off between high I_{on} and low SS.

- Minimum SS = meaningless number

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- Fixes I_{off} to 1e-4 μA/μm → steep slope at very low I_{on} not useful
- 0.5V overdrive measured from I_{off}
- CMOS has two order of magnitude higher current level → cannot compare
- Values of V_{DS} differs slightly: 0.2V(Alian), 0.3 or 0.5V

Summary

- Introduced tunnel FETs and low-power electronics

- Demonstrated TASE growth for TFETs and device fabrication.

- Traps at the oxide and hetero interface are currently limiting perfromance.

IBM Outlook

- Optimized InAs/Si p-TFETs fabricated using lateral TASE

- Working on the InAs/GaSb n-TFET

- Applications of TASE to new fields: photonics, sensors,…
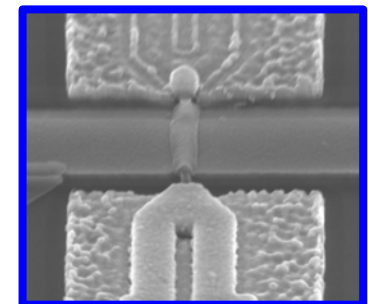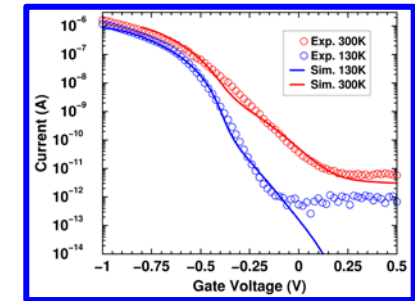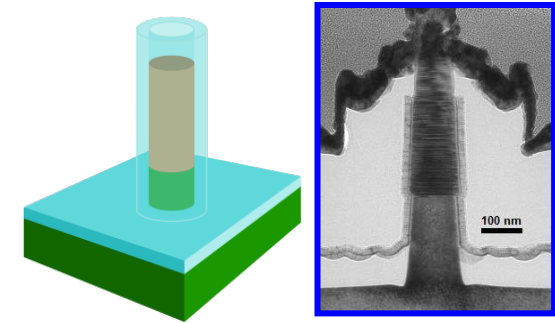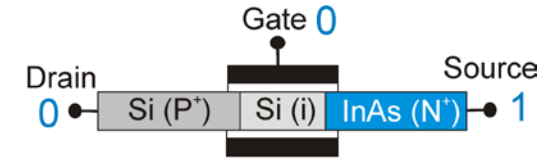
Thank you for your attention

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