GIDL Suppression by Optimization of Junction Profiles in 22nm DGSOI nFETs

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Abstract

It is shown by TCAD simulations how the gate-induced drain leakage which dominates the *OFF*-current in 22nm double-gate SOI nFETs with high-*K* gate stacks, can be minimized by proper variations of the junction profiles. Based on a microscopic, non-local model of band-to-band tunneling, transfer characteristics are computed after systematic changes in source/drain doping, body thickness, and HfO_2 layer thickness. This is done under the constraint of a minimal degradation of the *ON*-current. The ITRS target for LSTP devices (10 pA/µm) can be met.

Device description

The starting structure of the 22nm SOI nFET was defined in the EU project PULLNANO [1] as symmetrical double-gate architecture, see Fig. 1. The EOT is 1.1nm obtained with a 0.7nm interfacial layer and 2.4nm of HfO_2. The gate length is 22nm, the body thickness 10nm, and 4.6V are chosen for the gate work function. The channel is unstrained with <100> orientation, the source/drain extensions are 60nm long, and the contacts are placed vertically at the ends of them. The junction profiles were tuned to meet the *OFF*-current ITRS specification for LSTP devices (10 pA/µm) [2], assuming thermionic emission as leakage mechanism. Structure and doping information were translated into Sentaurus-Device [3] input files by the PULLNANO consortium [1]. When direct gate tunneling

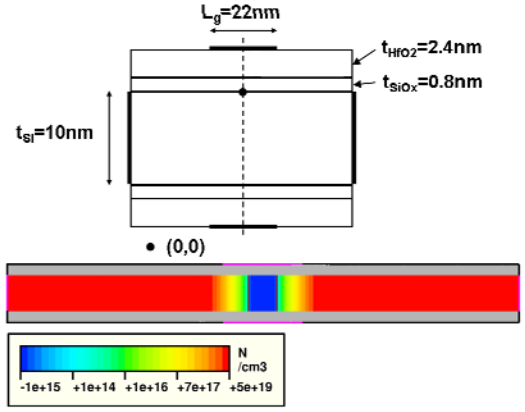

Fig.1: *Geometry and doping of the 22nm UTB DGSOI nFET.*

(GT) and non-local band-to-band tunneling (B2BT) are taken into account, the picture changes drastically, see Fig. 2. Whereas GT is only visible at low drain bias well below the ITRS limit, B2BT increases the *OFF*-current at 1V drain voltage by about 3 orders of magnitude. The GT assessment is based on the calibrated parameter set: $\varepsilon_{HfO2} = 23$, $\varepsilon_{SiO2} = 3.9$, $\chi_{HfO2} = 2.05$eV, $m_{HfO2} = 0.11m_0$, $\chi_{SiO2} = 0.9$eV, $m_{SiO2} = 0.5m_0$. The B2BT model will be described next.

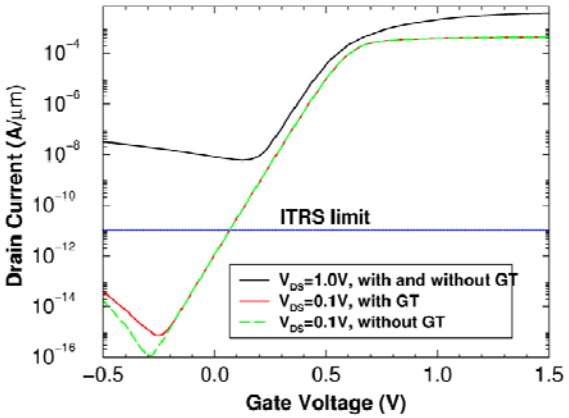

Fig.2: *Transfer characteristics showing the absence of gate leakage, but a strong GIDL due to B2BT.*

GIDL model

Phonon-assisted B2BT is a crucial leakage mechanism in strong electric fields of MOS structures. It must be turned on in TCAD simulations, if the field exceeds approximately $8\text{x}10^5$V/cm. The non-local B2BT rate is modeled according to the microscopic theory of [4,5] in [3]. Non-locality is crucial, as it e.g. prevents tunneling where no final states are available. In a MOSFET this usually happens close to the gate oxide interface, i.e. in a region where the electric field F in the semiconductor becomes maximal. In Fig. 3 this region is denoted as "dark space". The indirect B2BT transitions involve the emission/absorption of a transverse acoustic phonon with energy $\hbar\omega$. The tunnel barrier is given by an effective band gap which is modified by band gap narrowing and DOS tails. The B2BT model was validated using IV and CV data of special Si pn-junction diodes and their SIMS profiles, provided by P. M. Solomon, IBM Yorktown Heights [6].

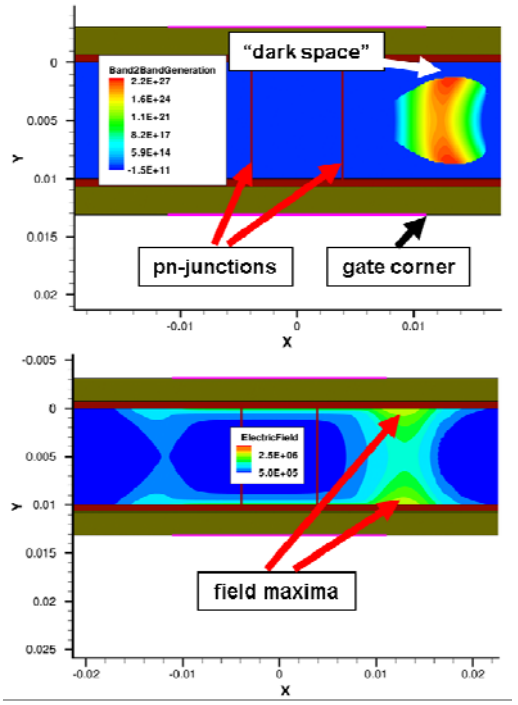

Fig.3: *Upper: B2BT rate location close to the gate corners. Lower: Spatial distribution of electric field.*

Technology variations for GIDL minimization

Increasing the decay length of the lateral Gaussian donor profile gives shallower junctions, but as expected, the effect on the *OFF*-current is practically zero, because the B2BT rate is not located in the pn-junction (see Fig. 3). The *ON*-current slightly degrades (~2%). Decreasing the plateau level of the donor profile results in shallower junctions which slightly shift outwards. A moderate decrease yields only a moderate improvement for the *OFF*-leakage, but also a moderate degradation of the *ON*-current. A significant reduction of the *OFF*-current can only be achieved with a strong decrease of the heavy S/D doping, at the price of a strongly reduced *ON*-current (lower S/D conductivity). If the Gaussian donor profiles are shifted outwards, the gate overlap becomes smaller and the sub-threshold swing improves markedly due to the stronger source-drain potential barrier. The *OFF*-current reduction is proportional to the size of this shift, see Fig. 4. The ITRS limit is almost reached with "PeakPos"=24nm which means that the decay of the profile starts 24nm from the centre of the device. The pn-junctions are then almost at the position of the gate corners (almost zero gate overlap). The ON-current decreases by only 6%. Decreasing the body thickness leads to a small reduction of the *OFF*-current only, but degrades the *ON*-current because of the lower mobility. A larger voltage drop across the gate oxide should reduce the voltage drop beneath the gate corners and thus reduce the B2BT rate. However, increasing the HfO_2 layer thickness from 2.4nm to 3.0nm gives only a very small reduction of the *OFF*-current.

Conclusions

The optimization of doping profile and geometry of the 22nm DGSOI nFET shows that a reduction of the *OFF*-current has to be paid with a degradation of the *ON*-current. In trying to find the best compromise it turned out that the only efficient measure is a shift of the lateral doping profiles such that the pn-junctions become very close to the gate corners. This brings I_{off} down to almost the ITRS limit while decreasing the *ON*-current by a few % only. All other variations studied have either a minor effect or are linked with an unacceptable degradation of I_{on}. These findings are restricted to the DG SOI architecture with lowly doped body, where the maximum of the B2BT rate is not located at the metallurgical junction, but close to the gate corner.

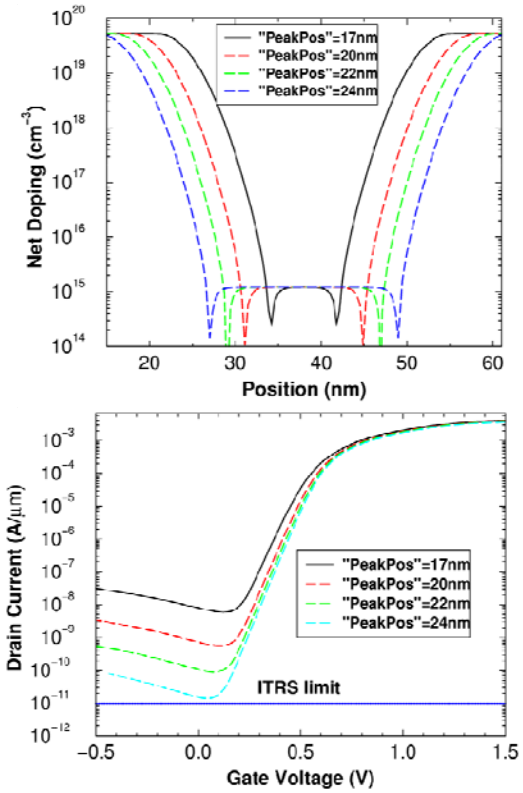

Fig.4: *Upper: Lateral shifts of the S/D doping profiles. Lower: Corresponding transfer characteristics.*

References

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