Complementary III-V heterostructure Tunnel FETs (invited)

K. E. Moselund, D. Cutaia, H. Schmid and H. Riel
Materials Integration and Nanoscale Devices Group
IBM Research Zurich
Rüschlikon, Switzerland
kmo@zurich.ibm.com

S. Sant and A. Schenk
Integrated Systems Laboratory
ETH Zürich
Zürich, Switzerland

***Abstract*—In the present work we will show our complementary TFET technology, which allows for the co-planar integration of InAs/Si p-TFETs and InAs/GaSb n-TFETs. We demonstrate both types of devices, show the results of the electrical characterization at room temperature and down to 125K. The p-TFETs exhibit excellent performance with I_{on} of a couple of μA/μm ($|V_{GS}| = |V_{DS}| = 0.5$V) combined with average subthreshold swing, *SS*, of 70-80mV/dec. The all III-V n-TFETs show about an order of magnitude higher I_{on}, but their SS is limited by the non-optimized gate stack and doping profiles.**

Thorough simulation studies of our devices show trap-assisted tunneling at the heterojunction to be the main limitation on SS. We will discuss the impact of different trap mechanisms and compare our results with other experimental data.

Keywords—tunnel FET, III-V, MOCVD growth, trap analysis

I. INTRODUCTION

Tunnel FETs, TFETs, are currently considered as the most promising steep slope devices for ultra-low power logic applications [1] [2], due to their ability to achieve sub-thermionic subthreshold swing, *SS*, referred to as the sub-60mV/dec limit at room temperature. To overcome this barrier, other types of devices have been investigated such as nanoelectromechanical switches (NEMS), ferro-electric FET and impact ionization devices. However, a very attractive feature of the TFET is that it resembles a MOSFET both in terms of device geometry as well as in circuit functionality, so that co-integration with CMOS is perceived as less challenging compared to other exotic devices, both from a technological point of view as well as with respect to circuit design. This may be true for Si-based devices, such as those reported in [3], which demonstrate fairly high level integration potential with the demonstration of a TFET inverter. However, III-V heterojunctions with smaller and tunable tunnel gaps are likely required to achieve the desired performance in terms of steep *SS* at reasonably high levels of I_{on} [4] [5] [6].

In the case of III-V TFETs, however, CMOS-like integration is far from straightforward. Either different material combinations are required for the n-type and p-type device, or even if using the same material system such as InGaAs/GaAsSb heterojunctions, different doping profiles would be required in the n- and p-channel device regions. As most III-V devices currently rely on in-situ doping, this would require separate growth runs for the different polarity devices.

To date, to the best of our knowledge, only two paths towards complementary III-V tunnel FET technologies have been demonstrated. The first work is that of Pandey et al. [7], where they employ a common metamorphic buffer technology on InP to grow separate molecular beam epitaxy stacks for p-TFET and n-TFET. Separate gate stacks are used for the two types of devices. Although this allows for the integration on the same wafer, the use of the InP substrate is not CMOS compatible and the scalability of this approach is ultimately limited by the growth process.

The second work, from our group, was just recently revealed [8] and is based on a novel technique for the local monolithic integration of III-V material on Si, which allows us to co-integrate InAs/Si p-channel devices with InAs/GaSb n-channel devices in a co-planar fashion. In the present work the details of our complementary TFET technology will be explained.

In addition, recent progress on experimental tunnel FETs indicates that when device geometries are optimized (scaled EOT and t_{body}, doping profiles etc.), we seem to be hitting a barrier where traps are limiting device performance in terms of achieving the ideal sub-thermionic slopes predicted by theory. Here we have carried out an extensive trap analysis for the p-channel InAs/Si TFETs, the impact of heterojunction traps on device performance will be highlighted.

II. DEVICE FABRICATION

The device fabrication is detailed in Fig. 1, which shows a simplified schematic of the process flow for the two different polarity devices. For the III-V materials integration we rely on our recently developed Template-Assisted-Selective-Epitaxy (TASE) technique [9], which was used for the demonstration of InAs NW MOSFETs and Hall-structures [10] and for the dense integration of high-performance InGaAs MOSFETs [11].

In this technique, the III-V material is grown within an oxide tube with a single Si nucleation seed at one extremity. In this fashion, high-quality III-V material can be integrated locally and densely. The growth step is very selective so that only opened templates will be filled with III-V material, this makes it possible to carry out independent growth runs by consecutively opening up neighboring templates, as illustrated in Fig. 2.

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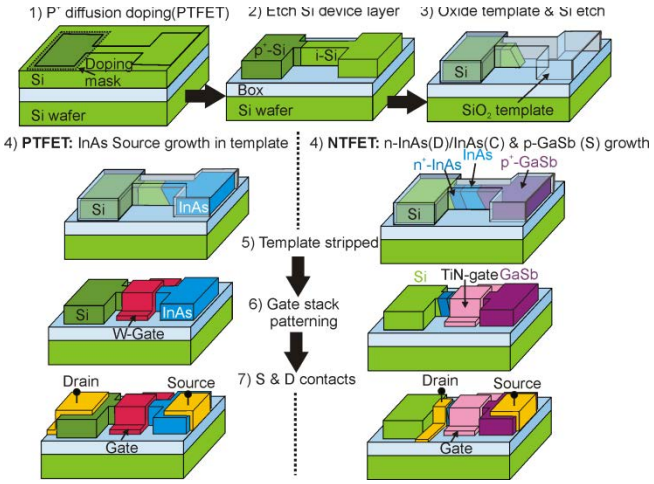

Fig. 1 Schematic showing the process flow for p-channel InAs/Si TFETs and n-channel InAs/GaSb TFETs. The template fabrication is identical for the two cases, except for the doping of the p^+-Si drain region for the p-TFETs (1). (2) The future device structure is etched out, for the p-TFET Si is part of the device, whereas in the case of the n-TFET it only serves as nucleation site. (3) Template is opened and Si etched back to a desired depth. (4) III-V material or materials are grown. (5) The template is stripped in BHF (not shown). (6) Gate stack is deposited and patterned, and (7) contacts are defined and patterned using E-beam lithography and lift-off.

In the case of the p-TFET only the InAs source is regrown, whereas the p+-drain, and i-channel are implemented in the Si SOI layer. The advantage of this approach is that the Si likely presents less interface traps, D_{it}, in the gate stack, compared to the III-Vs, on the other hand the lattice mismatch of about 11% between InAs/Si is expected to create defects at the heterojunction. In the case of the n-TFET the entire device structure n+-InAs drain, n-InAs channel, and p-GaSb source is grown in a single growth run. The system is almost lattice matched with about 0.65% mismatch, and if introducing ternary compounds one might completely remove the mismatch.

Top-view scanning electron micrograph (SEM) images as well as cross-sections of devices are shown in Fig. 3. A diluted HF dip right before growth slightly expands the oxide nanotube, making the III-V segments slightly larger than the Si. Dimensions are around 30nm. For both devices we use a conservative normalization of W_{eff} = 100nm for the electrical characteristics.

The present devices are fabricated on two separate wafers as this simplifies the growth and fabrication process, but the process flow is the same, so in principle there is no barrier to co-integrating the two types of devices on the same substrate. The gate dielectric deposition procedure and composition of the stack is the same in the two cases, although not optimized for GaSb. The only difference in terms of the device implementation is the use of a different gate metal in the two cases. However, W and TiN have similar work functions and we have not observed any significant impact on device performance in the past. In both cases a gate stack anneal (10 min, 300°C, 25%H_2 in Ar) is carried out. In addition for the InAs/Si p-TFETS we found the performance to be much improved by a final contact annealing step (5min, 300°C, Ar). This allows for a Ni-silicidation to be formed at the p^+ Si drain contact. Fig. 4 illustrates the effect of this anneal on the SS of our devices, and also compares with previously fabricated devices [12] [13] in the vertical geometry.

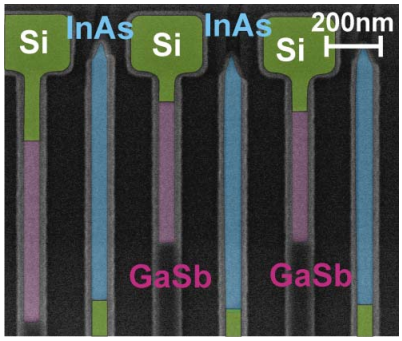

Fig. 2 SEM image of a template array which has been filled with different III-V materials. First the InAs containing templates were grown, and in the second growth step these were sealed off, while GaSb was grown in the neighboring tubes.

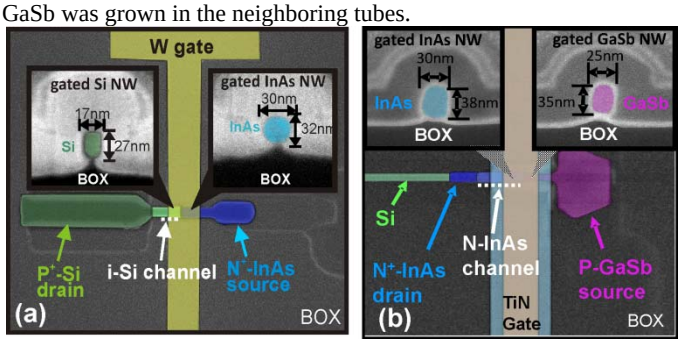

Fig. 3 Top view SEM images of the fabricated a) p-TFET and b) n-TFET before isolation and contacting so that the III-V regions are clearly visible. Insets show cross-sections in the different regions: cross sections as small as 17x27 nm^2 and 25x35 nm^2 are achieved for p- and n-type devices respectively.

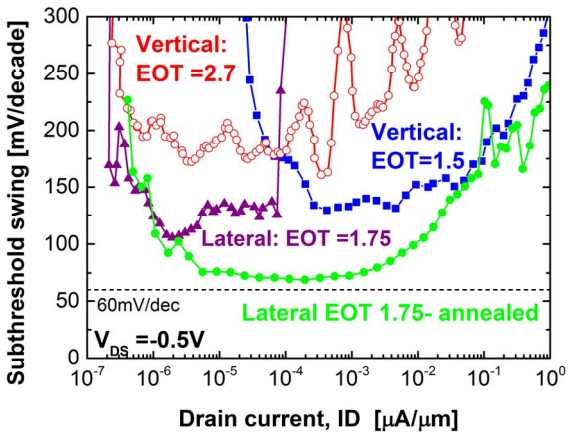

Fig. 4 Comparison of lateral InAs/Si p-TFETs presented in this work before and after anneal with previously demonstrated reported vertical TFETs in the same material combination.

Physical gate lengths of devices measured are about 900nm for the p-TFET, where about 200-250 nm overlap the InAs source. For the n-TFET the physical gate length is 150nm, with about 100nm on top of the InAs channel and 50nm on the GaSb source.

III. Electrical Characterization

Transfer characteristics of both p-TFET and n-TFET are shown in Fig. 5 for different V_{DS} bias levels. The I_{on} of the p-TFET is 4μA/μm, whereas for the all III-V n-TFET it is about an order of magnitude larger. We have been optimizing the InAs/Si TFET through several generations, which is evidenced in the excellent average slope and good turn-on characteristics. On the other hand, this is the first TASE implementation of an InAs/GaSb TFET, hence the gate stack and doping profiles are not optimized which results in a poor slope. The drop-off in I_{on} at large V_{GS} is a result of the on-set of GaSb depletion.

As it can be seen Fig. 4 SS performance is markedly improved compared to our previously shown vertical devices. We believe the main improvement is a result of geometry scaling, present device diameters are about 30 nm, whereas the vertical devices had diameters of around 100 nm.

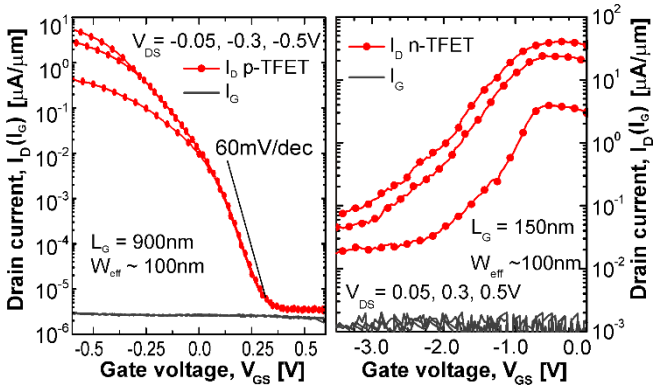

Fig. 5 Room temperature and DC transfer characteristics of p-TFET and n-TFET devices for different $|V_{DS}|$ = 50 mV, 0.3 & 0.5 V. Black curves represent the gate leakage, which is negligible in both cases.

Diode characteristics $I_D(V_{DS})$ measured on the TFETs are shown in Fig. 6. The reverse branch corresponds to the output characteristic of the tunnel FETs. Previously, we have observed negative-differential resistance (NDR) regions in our tunnel diodes [14] [15], but not in the TFETs. The explanation for this different behavior is as follows: In the case of the InAs/Si junction, high carrier concentrations on both sides of the junction are required to observe the NDR. Simulation shows that this condition is only met for gate voltages above ~1V, i.e. outside of the present measurement range.

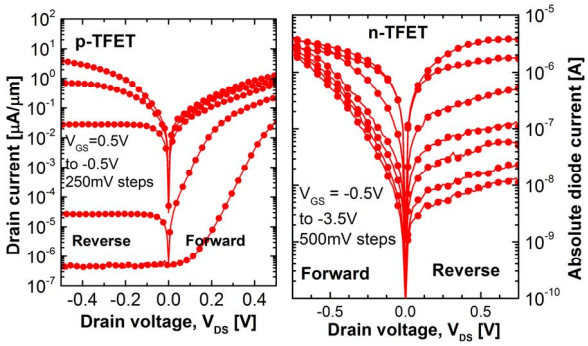

Fig. 6 Diode characteristics of p-TFET and n-TFET at 300K, the reverse branches correspond to the output characteristic of the TFET.

The lack of NDR observed in n-TFETs, as opposed to pin diodes fabricated on the same chip (not shown here), is attributed due to the presence of D_{it} in the gate stack which effectively suppresses the NDR.

IV. Low-Temperature Characterization

We carried out temperature sweeps for both devices down to 125 K and corresponding transfer characteristics are shown in Fig. 7. In both cases only a fairly small I_{on} dependence is shown, in the case of the n-TFET dominated by GaSb depletion as previously mentioned. The subthreshold swing, however, show a very strong temperature dependence, indicating the presence of traps.

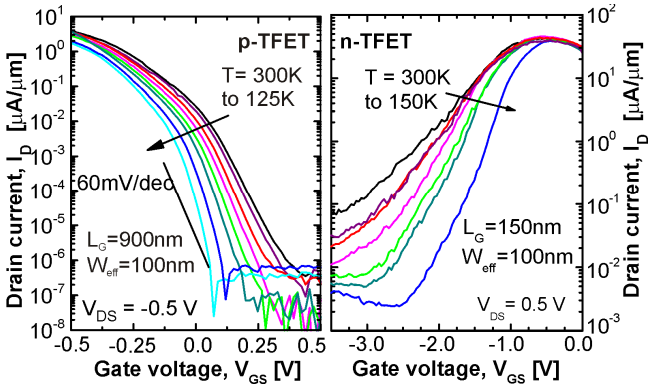

Fig. 7 Transfer characteristics for p-TFET and n-TFET as a function of temperature from room temperature down to 125 (150) K, for a V_{DS} bias of 0.5V.

Traps have been identified as the main impediment of TFETs when it comes to achieving sub-thermionic slopes [16]. The nature of the traps is likely very different depending on device geometry and dimensions. For example, in the present case we believe the SS of the InAs/GaSb n-TFET to be dominated by D_{it} from the non-optimized gate stack. In the InAs/Si p-TFET, however, the majority of the gate overlaps the Si channel, which is expected to have relatively low oxide D_{it}, whereas the large lattice mismatch of 11% is expected to contribute significant trap densities at the heterojunction.

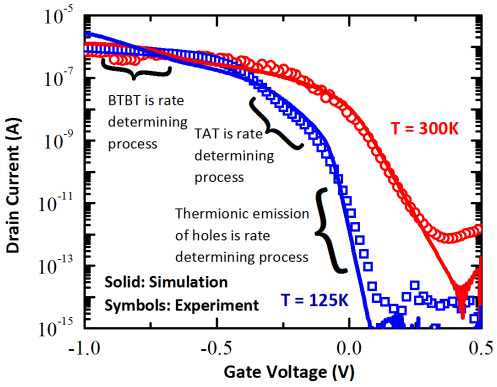

Fig. 8 Comparison of experimental and simulated transfer characteristics of an InAs/Si p-TFET at 125K and 300K. The dominating mechanisms in the different intervals are indicated.

We have carried out extensive TCAD simulation of our InAs/Si devices [17], using simulation parameters carefully calibrated to first tunnel diodes and then full TFETs. As seen in Fig. 8 this results in excellent matching of experiment and simulation at both room- and low-temperature. The combination of a high trap density and a fairly long gated i-Si region means that the TAT process acts as a current source generating electron-hole pairs, whose passage through the channel is controlled by a thermionic barrier, hence for low gate bias levels the device effectively works as a MOSFET (in terms of functionality, not because there is a parasitic MOSFET in the physical structure), this is the region indicated as thermionic emission in Fig. 8. This results in a slope similar to the 60mV/dec. governed by the device electrostatics. At medium gate bias levels trap-assisted tunneling determines the slope, and only at high bias levels does BTBT dominate.

In Fig. 9 the different contributions to the current are displayed for the 300K case. By turning on- and –off various trap mechanisms we can observe that although band-to-band-tunneling is responsible for the I_{on} at high V_{GS}, the entire transient is dominated by traps, which in our case originate at the InAs/Si heterojunction, oxide D_{it} only plays a minor role. If no traps were present the transient at the higher current levels relevant for transport would be steeper, whereas since the on-set of BTBT is more gradual at the lower current levels SS in this case would actually be less abrupt. In [17] the operation principle and specific device optimizations to improve performance are investigated in more detail.

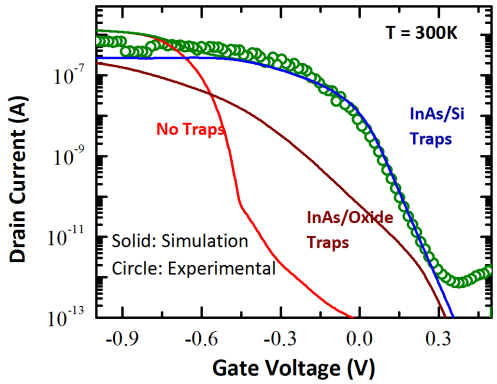

Fig. 9 Individual contributions of BTBT and the two trap-assisted processes at 300K in the simulated transfer characteristics of an InAs/Si p-TFE.

I. Discussion

In Fig. 10 we compare the SS vs. I_D for the present work with that extracted from a number of experimental references. A few other good experimental devices are not included because they either did not include an SS vs. I_D plot or I_D values were not normalized to effective width. The purpose is not to discuss the merits of each one; those are all among the very best experimental TFETs, the majority of fabricated devices lie outside of this chart because slopes are too large or current levels way too low. These devices possess different advantages and challenges when it comes to future promise and integration capability. However, when comparing with

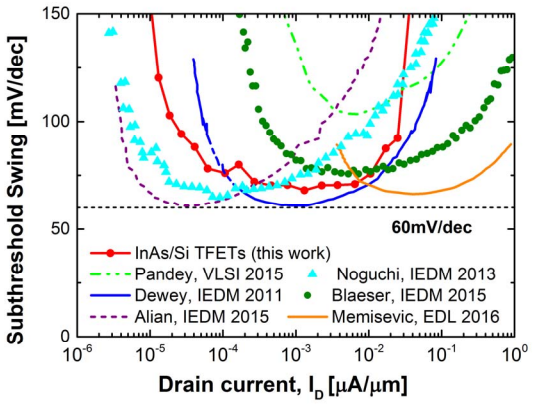

Fig. 10 Subthreshold swing as a function of drain current, extracted from a number of published TFET works **[7] [6] [4] [18] [19] [5]**. Values are adapted from .pdf data so minor variations might appear. In all cases we have chosen values close to 0.3 or 0.5V.

these references, they all seem to converge towards similar values which are suspiciously close to this same limit, and none achieve sub-thermionic slopes. Naturally, we cannot discuss the limitations of other works, but based on our own experience and recent conclusions of others [16] we may conclude that once device geometries have been fine-tuned and sufficiently scaled, trap mechanisms (D_{it}, heterojunction, doping, material defects) are responsible for the performance limitations. Hence, to experimentally realize the promises of TFETs which we know from simulation studies, we have first to establish the nature of the traps and then find appropriate solutions to deal with these.

II. Conclusion

We have demonstrated a process which allows for the co-integration of n- and p-channel TFETs on silicon and in a planar geometry compatible with conventional CMOS processing. We have demonstrated dense material integration in a CMOS-compatible approach for TFETs, which can be integrated with MOSFETs and other devices on the same wafer. The p-TFETs show excellent device performance with I_{on} around 4 μA/μm (V_{GS} = V_{DS} = -0.5V) range and average *SS* around 70-80 mV/dec. Yet, the turn-on is limited by trap-assisted generation processes. Conversely, the n-TFETs suffer from an immature gate-stack processing, but exhibit higher tunneling probability and thus I_{on}. Also, we have discussed the contribution of traps, which we believe to be the biggest barrier for TFETs in general, when it comes to fulfilling the promise of steep slopes.

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REFERENCES

[1] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, pp. 329-337, 2011.

[2] H. Lu and A. Seabaugh, " Tunnel Field-Effect Transistors: State-of-the-Art," *Journal of the EDS*, vol. 2, pp. 44-49, 2014.

[3] L. Knoll, Q. Zhao, A. Nichau, S. Richter, G. Luong, S. Trellenkamp, A. Schafer, L. Selmi, K. Bourdelle and S. Mantl, "Demonstration of improved transient response of inverters with steep slope strained Si NW TFETs by reduction of TAT with pulsed I-V and NW scaling," *IEEE International Electron Devices Meeting (IEDM)*, p. 4.4, 2013.

[4] G. Dewey, B. Chu-Kung, J. Boardman, J. M. Fastenau, J. Kavalieros, R. Kotlyar, W. K. Liu, D. Lubyshev, M. Metz, N. Mukherjee, P. Oakey, R. Pillarisetty, M. Radosavljevic, H. W. Then and R. Chau, "Fabrication, Characterization, and Physics of III-V Heterojunction Tunneling Field Effect Transistors (H-TFET) for Steep Sub-Threshold Swing," *Proc. International Electron Device Meeting, IEDM*, p. 33.6, 2011.

[5] M. Noguchi, S. Kim, M. Yokoyama, S. Ji, O. Ichikawa, T. Osada, M. Hata, M. Takenaka and S. Takagi, "High Ion/Ioff and low subthreshold slope planar-type InGaAs tunnel FETs with Zn-diffused source junctions," *Tech. Dig IEDM*, p. 28.1, 2013.

[6] A. Alian, J. Franco, A. Vandooren, Y. Mols, A. Verhulst, S. E. Kazzi, R. Rooyackers, D. Verreck, Q. Smets, A. Mocuta, N. Collaert, D. Lin and A. Thean, "Record performance InGaAs homo-junction TFET with superior SS reliability over MOSFET," *Tech. Dig. IEDM*, p. 37.1, 2015.

[7] R. Pandey, H. Madan, H. Liu, V. Chobpattana, M. Barth, B. Rajamohanan, M. J. Hollander, T. Clark, K. Wang, J.-H. Kim, D. Gundlach, K. P. Cheung, J. Suehle, R. Engel-Herbert, S. Stemmer and S. Datta, "Demonstration of p-type In0.7Ga0.3As/GaAs0.35Sb0.65 and n-type GaAs0.4Sb0.6/In0.65Ga0.35As Complimentary Heterojunction Vertical Tunnel FETs for Ultra-Low Power Logic," *Symp. on VLSI Technology*, pp. 15-3, 2015.

[8] D. Cutaia, K. E. Moselund, H. Schmid, M. Borg and A. &. R. H. Olziersky, "Complementary III-V Heterojunction Lateral NW Tunnel FET Technology on Si," *accepted for Symp. on VLSI Technology*, 2016.

[9] M. Borg, H. Schmid, K. E. Moselund, G. Signorello, L. Gignac, J. Bruley, C. Breslin, P. D. Kanungo, P. Werner and H. Riel, "Vertical III-V Nanowire Device Integration on Si(100)," *Nano Letters*, vol. 14, pp. 1914-1920, 2014.

[10] H. Schmid, M. Borg, K. Moselund, L. Gignac, C. M. Breslin, J. Bruley, D. Cutaia and H. Riel, "Template-assisted selective epitaxy of III-V nanoscale devices for co-planar heterogeneous integration with Si," *Applied Physics Letters*, vol. 106, p. 233101, 2015.

[11] L. Czornomaz, E. Uccelli, M. Sousa, V. Deshpande, V. Djara, D. Caimi, M. Rossel, R. Erni and J. Fompeyrine, "Confined Epitaxial Lateral Overgrowth (CELO): A novel concept for scalable integration of CMOS-compatible InGaAs-on-insulator MOSFETs on large-area Si substrates," *VLSI Technology (VLSI Technology), 2015 Symposium on*, pp. T172 - T173, 2015.

[12] D. Cutaia, K. E. Moselund, M. Borg., H. Schmid, Gignac, C. Breslin, S.Karg, E. Uccelli and H. Riel, "Vertical InAs-Si Gate-All-Around Tunnel FETs Integrated on Si using Selective Epitaxy in Nanotube Templates," *Journal of the EDS*, vol. 3, no. 3, pp. 176-183, 2015.

[13] K. E. Moselund, H. Schmid, C. Bessire, M. T. Björk, H. Ghoneim and H. Riel, "InAs–Si Nanowire Heterojunction Tunnel FETs," *IEEE Electron Device Letters, ,* vol. 33, pp. 1453-1455, 2012.

[14] H. Schmid, C. Bessire, M. T. Bjoerk, A. Schenk and H. Riel, "Silicon Nanowire Esaki Diodes," *Nano Letters,*, vol. 12, pp. 699-703, 2012.

[15] D. Cutaia, M. Borg, H. Schmid, K. Moselund, N. Bologna, A. Ionescu and H. Riel, "Temperature dependent conductance slope analysis of InAs-GaSb nanowire junctions fabricated on Si," *In preparation.*

[16] U. E. Avci, B. Chu-Kung, A. Agrawal, G. Dewey, V. Le, R. Rios, D. H. Morris, S. Hasan, R. Kotlyar, J. Kavalieros and I. A. Young, "Study of TFET Non-ideality Effects for Determination of Geometry and Defect Density Requirements for Sub-60mV/dec Ge TFET," *tech. Digest IEDM*, p. 34.5, 2015.

[17] S. Sant, K. E. Moselund, D. Cutaia, H. Schmid, M. Borg, H. Riel and A. Schenk, "Lateral InAs/Si p-type Tunnel FETs integrated on Si - Part 2: Simulation Study of the Impact of," *IEEE Transactions on Electron Devices*, p. To be submitted., 2016.

[18] S. Blaeser, S. Glass, C. S.-B. K. Narimani, N. v. d. Driesch, S. Wirths, A. T. Tiedemann, S. Trellenkamp, D. Buca, Q. T. Zhao and S. Mantl, "Novel SiGe/Si line tunneling TFET with high Ion at low VDD and constant SS," *International Electron Devices Meeting (IEDM)*, p. 22.3, 2015.

[19] E. Memisevic, J. Svensson, M. Hellenbrand, E. Lind and L.-E. Wernersson, "Scaling of Vertical InAs-GaSb nanowire Tunneling Field-Effect Transistors on Si," *Electon Device Letters*, vol. 37, pp. 549 -552, 2016.

[20] K. Tomioka and T. Fukui, "Tunnel field-effect transistor using InAs nanowire/Si heterojunction," *Applied Physics Letters*, vol. 98, p. 083114, 2011.

[21] G. Zhou, Y. Lu, R. Li, Q. Zhang, Q. Liu, T. Vasen, H. Zhu, J. M. Kuo, T. Kosel, M. Wistey, P. Fay, A. Seabaugh and H. Xing, "InGaAs/InP Tunnel FETs With a Subthreshold Swing of 93 mV/dec and ION/IOFF Ratio Near 1E6," *IEEE Electron Device Letters*, vol. 33, pp. 782-784, 2012.