Effect of Surface Roughness and Phonon Scattering on Extremely Narrow InAs-Si Nanowire TFETs

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***Abstract*—The impact of surface roughness (SR) and phonon scattering on extremely narrow InAs-Si Nanowire TFETs is studied in this paper. The rough surface of the nanowire is generated by randomly distributing the atoms at the InAs-Si/Oxide interface according to an Ando-like exponential auto-correlation function. Phonons are atomistically treated by means of the valence-force-field method. A full-band and atomistic quantum transport simulator based on the $sp^3d^5s^*$ tight-binding model and the non-equilibrium Green's function formalism is used to solve the quantum transport problem where the electron-phonon interactions are tackled within the self-consistent Born approximation. Phonon scattering is found to have no major effect on the device ON-state, while in the OFF-state the current is significantly increased. SR scattering has a detrimental impact on the TFET performance with a ON-current reduction by almost two orders of magnitude, but it induces limited variability. A direct comparison of both scattering mechanisms reveals the dominant behavior of SR over phonon scattering.**

I. Introduction

Band-to-band tunneling (BTBT) transistors (TFETs) are expected to give rise to a new generation of low-power consumption logical switches [1]. During the last decade both theoretical and experimental efforts have been launched to realize a TFET that could challenge the current metal-oxide-semiconductor field-effect transistors (MOSFETs) [2]–[5]. From a theoretical point of view, in ideal conditions, TFETs achieve lower subthreshold swings (SS) than MOSFETs reach at room temperature, i.e. $SS = 60$ mV/dec. However, to date, there has been no experimental demonstration of a bulk-like TFET with a high ON-current and low SS at the same time. In order to boost the TFET ON-current, staggered-gap (InAs-Si) [3] and broken-gap (InAs-GaSb) [4] heterojunctions have been proposed. Although the latter has been shown to be a possible solution for the ON-state current issue, its SS is significantly higher than in MOSFETs with values around 100 mV/dec. This deterioration can be attributed to the presence of trap-assisted tunneling (TAT) in the OFF-state caused by imperfections at the material interface.

At the nanometer scale, quantum phenomena, especially geometrical confinement, and scattering mechanisms, such as surface roughness (SR) and electron-phonon interactions, start to play an important role and strongly affect the device performance. This has been clearly shown in MOSFETs [6]. In the case of TFETs, however, the influence of scattering has received much less attention and only few papers can be found in the literature [7] on this subject.

In this work, we present for the first time, the impact of SR and phonon scattering on (extremely narrow) gate-all-around InAs-Si nanowire TFETs as schematized in Fig. 1. The nanowire is oriented along the $\langle 111 \rangle$ crystallographic direction. The source (n^+-type InAs region) and drain (p^+-type Si region) are highly doped, whereas the gate contact is only placed around the intrinsic-Si channel region. A full-band and atomistic device simulator called OMEN [8] and based on the $sp^3d^5s^*$ tight-binding model and the non-equilibrium Green's function formalism is used to perform the required quantum transport calculations self-consistently with Poisson's equation. The rough surface of the nanowire is

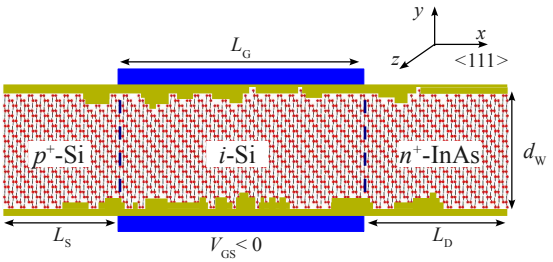

Fig. 1. Schematic of a InAs-Si nanowire TFET with a rough surface. For all devices, the drain-length is $L_d = 10$ nm (p^+-type Si region), the channel-length $L_G = 15$ nm, and the source-length $L_s = 25$ nm (n^+-type InAs region) with $d_w = 2.5$ nm. The doping concentrations are $N_D = 2 \times 10^{20}$ cm^{-3} and $N_A = 10^{19}$ cm^{-3}, whereas the effective oxide thickness under the gate region is EOT $= 0.43$ nm. The temperature in the devices is assumed to be 300 K.

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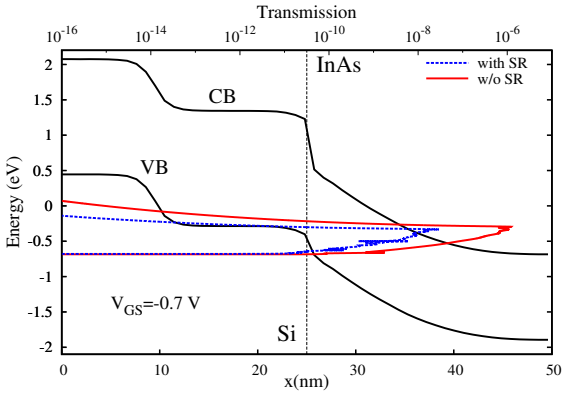

Fig. 2. Comparison of the BTBT probability between InAs-Si nanowire TFETs with s perfect (red line) and rough (blue dashed-line) surface. The band diagram (black line) is also shown. The peak BTBT probability corresponding to a perfect nanowire is two orders of magnitude higher than the one with SR.

modeled by randomly distributing the atoms at the InAs-Si/Oxide interface according to an Ando-like exponential auto-correlation function [9]. The phonons propertities are represented with a valence-force-field model [10], while the electron-phonon interactions are taken into account via the self-consistent Born approximation. As convergence criteria it is ensured that the current does not vary by more than 1% all along the device. The effect of both scattering mechanisms on the InAs-Si TFET are analyzed by compering the obtained performance with the ideal devices. The main findings are presented in details in the following sections.

II. Results

Figure 1 sketches the InAs-Si heterojunction nanowire TFET considered in this work. The transport direction is along the $\langle 111 \rangle$ crystallographic direction (x-axis). The gate all-round contact surround an intrinsic channel of length $L_{\mathrm{G}} = 15$ nm, whereas the source (n^+-type InAs) and drain (p^+-type Si) regions are 25 nm and 10 nm long, respectively. The nanowire diameter is set to 2.5 nm. The device is highly doped with $N_{\mathrm{D}} = 2{\times}10^{20}\,\mathrm{cm}^{-3}$ and $N_{\mathrm{A}} = 10^{19}\,\mathrm{cm}^{-3}$. The oxide is 1 nm thick with a dielectric constant $\epsilon_{\mathrm{high}-\kappa} = 9$. The applied drain-to-source bias is $V_{\mathrm{DS}} = -1$ V and all simulations were performed at room temperature, i.e. 300 K.

A. Surface roughness scattering

Surface roughness scattering is modeled by randomly distributing the atoms at the InAs-Si/oxide interface according to an Ando-like exponential auto-correlation function $\Gamma_s(x) = \Delta_m^2 \exp\left(-|x|/L_m\right)$ characterized by a

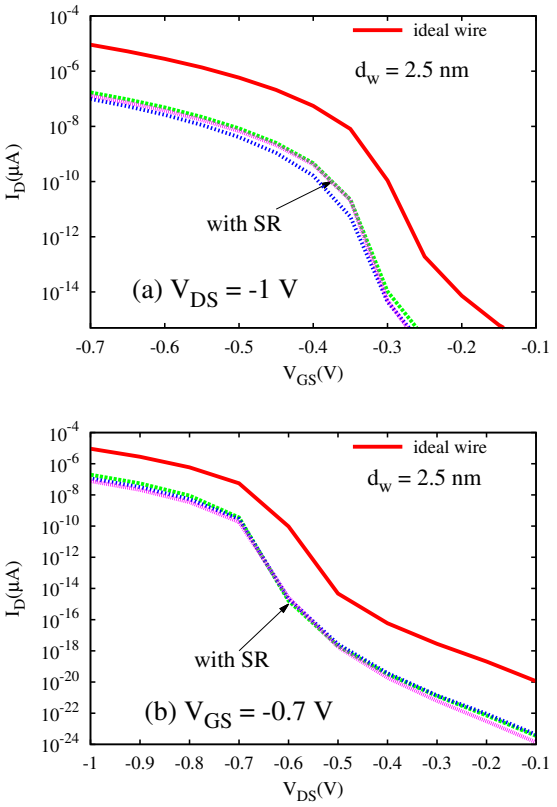

Fig. 3. I_{D}-V_{GS} transfer (a) and I_{D}-V_{DS} output (b) characteristics of three different InAs-Si nanowire TFETs with rough surfaces and of their ideal counterpart (red solid-line) are compared.

rough surface mean square Δ_m and a correlation length L_m. We defined $\Delta_m = 0.14$ nm and $L_m = 0.7$ nm [9]. Simulations of InAs-Si nanowire TFETs with rough surface have been carried out using OMEN [8], based on the $sp^3d^5s^*$ tight-binding model and the non-equilibrium Green's function formalism.

Figure 2 shows the BTBT of a InAs-Si nanowire TFET with a perfect (red line) and rough (blue dashed-line) surface. As a consequence of SR, the BTBT probability decreases by two orders of magnitude due to a modification of the quantized energy levels. Each realization of the rough surface might lead to a different BTBT probability. However, we have observed that they remain qualitatively and quantitatively the same.

The I_{D}-V_{GS} transfer and I_{D}-V_{DS} output characteristics of three different InAs-Si nanowire TFETs with rough surfaces and of their ideal counterpart are reported in Fig. 3(a) and Fig. 3(b), respectively. When SR scattering is present the current is reduced by about two orders of magnitude as compared to its ideal value at $V_{\mathrm{GS}} = -0.7$ V with $V_{\mathrm{DS}} = -1$ V. For thicker

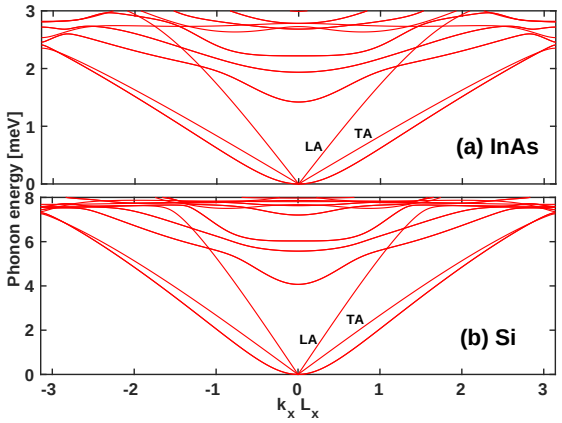

Fig. 4. Phonon bandstructure of (a) InAs and (b) Si nanowires with diameter $d_{\mathrm{w}} = 2.5$ nm. The longitudinal (LA) and transverse acoustic (TA) branches are pointed out in their corresponding figure.

devices this different would be much less. The rough surface not only suppress the tunneling paths close to the InAs-Si/oxide interface, but also effectively reduces the nanowire diameter causing an increment of band-gap. This effect can be observed at higher gate biases, where the SR scattering shifts the onset gate voltage by -0.1 V. Also, notice that in both I_{D}-V_{GS} (Fig. 3(a)) and I_{D}-V_{DS} (Fig. 3(b)) characteristics the variability due to different representations of the rough surface is very low.

B. Phonon scattering

The oscillations of atoms around their equilibrium position induce electron-phonon interactions, i.e. the electronic system is perturbed by lattice vibrations. Electron-phonon interactions have been widely investigated in nano-MOSFETs using the effective-mass approximation (EMA). Less often with a full-band model as required in TFETs where an accurate representation of the conduction and valence sub-bands is necessary. Similarly, the bulk phonon properties are generally used in nanostructures although confinement also affects the lattice vibrations. Hence, a more accurate description of phonons is needed at the nanometer scale. For that purpose, we employ again OMEN, which implements a valence-force-field (VFF) model to atomistically treat the lattice vibration or phonons of a given semiconductor. The VFF method provides an expression for the total potential energy as a function of the ion positions including different harmonic interactions [11]. By taking the second derivatice of this potential the dynamical matrix of the system can be constructed. By solving the resulting eigenvalue problem one obtains the phonon bandstructure. For instance, the phonon bandstructure of an InAs and Si nanowire with transport direction along the $\langle 111 \rangle$-direction and $d_{\mathrm{W}} = 2.5$ nm is plotted in Fig. 4(a) and Fig. 4(b), respectively. The group velocity of the longitudinal (LA) and transverse (TA) acoustic modes can be extracted from Fig. 4. In case of InAs, it is found to be 2572 m/s and 1200 m/s for the LA and TA modes, respectively. For the Si nanowire, the group velocity is equal to 7820 m/s for the LA and 3870 m/s for the TA modes.

The full derivation of the electron-phonon interaction Hamiltonian can be found in Ref. [11]. Here, the main expressions are summarized. The perturbation Hamiltonian that describes the electron-phonon interactions is given in second quantization as [11]

$$H_{\mathrm{ep}} = \sum_{n,\,m} \nabla H_{nm} \left(\hat{u}_n - \hat{u}_m \right) c_m^{\dagger} c_n, \tag{1}$$

where the $\hat{u}_m$ is the quantized lattice displacement and the operator c_m ($c_m^{\dagger}$) annihilates (creates) an electron at a position $\mathbf{R}_m$. The electron-phonon coupling $\nabla \mathbf{H}$ is obtained by derivating the tight-binding Hamiltonian $\mathbf{H}$. Then, within the NEGF formalism and applying perturbation theory, the electron-phonon interactions can be cast into a scattering self-energy [11]:

$$\Sigma_{nn}^{\lessgtr} = \sum_{l,\mathbf{q}} \tilde{I}_{nlln}(\mathbf{q}) \nabla H_{nl} \Big(\nu_{\mathbf{q}} G_{ll}^{\lessgtr}(E \pm \hbar\omega_{\mathbf{q}}) + (\nu_{\mathbf{q}} + 1) G_{ll}^{\lessgtr}(E \mp \hbar\omega_{\mathbf{q}}) \Big) \nabla H_{ln}. \tag{2}$$

The indices l and n refer to atomic positions, whereas $\nu_{\mathbf{q}}$ and $\tilde{I}_{nlln}(\mathbf{q})$ are the Bose-Einstein distribution and a form-factor, respectively. They both depend on the phonon wave-vector $\mathbf{q}$. From Eq. (2) one can see that the lesser/greater scattering self-energy $\Sigma^{\lessgtr}$ is a function of the Green's function $G^{\lessgtr}$. Both equations must therefore be solved in a self-consistent way till convergence is achieved. This procedure is known as self-consistent Born approximation. It stops when the current is conserved within 1% along the entire device.

Electron-phonon interactions have been only considered in the case of a nanowire with a perfect InAs-Si/oxide interface. Due to its high computational intensity, such interactions could only be investigated at three different gate voltages corresponding to the ON-state ($V_{\mathrm{GS}} = -0.7$ V) , OFF-state ($V_{\mathrm{GS}} = -0.15$ V), and at a middle gate voltage ($V_{\mathrm{GS}} = -0.35$ V). The results are reported in Fig. 5. From left to right, one sees that the influence of phonon scattering on the ON-state is negligible, while at lower gate voltages its impact

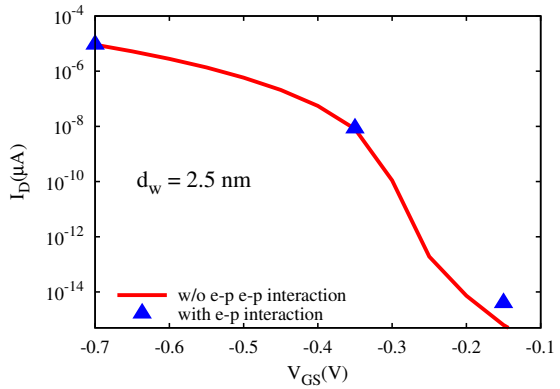

Fig. 5. Comparison of the I_D-V_{GS} transfer characteristics of an InAs-Si nanowire TFET with (triangle point) and without (red solid-line) electron-phonon scattering.

becomes more pronounced. In the OFF-state, the current is enhanced by about one order of magnitude, thus deteriorating the SS when electron-phonon scattering is turned on. Although in this material configuration the BTBT is direct, states below the conduction and above the valence band are connected, by the emission and absorption of phonons, which increases the leakage OFF-state current.

The simultaneous presence of SR and phonon scattering should even more affect the TFET performance, i.e. SR reduces not only the ON-state current but also the OFF-state one, as observed in Fig. 3. However, the OFF current will increase due to phonon scattering, this leads to a higher SS. The impact of SR scattering is expected to be dominant in extremely narrow nanowire TFETs.

III. Conclusion

Surface roughness and phonon scattering have been included in the simulation of on extremely narrow InAs-Si nanowire TFETs. A full-band and atomistic quantum transport simulator based on the $sp^3d^5s^*$ tight-binding model, the valence-force-field method, and the non-equilibrium Green's function formalism was used to estimate the performance degradations caused by these non-ideal effects. Phonon scattering was found to have no influence on the ON-state of the device, while it significantly increased the OFF-state current. SR scattering did not induce a strong variability of the transistors characteristics, although it reduced the transistor ON-current by almost two orders of magnitude. It is expected that in extremely narrow InAs-Si nanowire TFETs, SR scattering plays a more important role than phonon scattering.

Acknowledgment

The research leading to these results has received funding from the European Community's Seventh Framework Programme under grant agreements No. 619509 (Project E^{2}SWITCH) and No. 604416 (Project DEEPEN).

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