Modeling of Leakage Currents in Ultra Shallow Junctions

A. Schenk and A. Scheinemann
Integrated Systems Laboratory, ETH Zurich

Recent developments in CMOS technology introduce process steps inflicting higher damage to the silicon lattice. Amorphising implants and simultaneous reduction of thermal budgets to gain better control of the formation of Ultra Shallow Junctions (USJs) render the presence of extended defects in active regions unavoidable. Therefore, a better understanding of the electrical properties of extended defects i.e. Dislocation Loops (DLs) and {311}-defects is mandatory.

We evaluate electrical characterization data for dedicated samples with controlled introduction of defects by non-amorphising Si implants and amorphising Ge-implants. Commercial process (Sentaurus-Process) and device (Sentaurus-Device) simulation tools are used to test the plausibility of applied defect models and test basic assumptions about the electrical activity of the defects. Experimentally found correlations between defect concentration and leakage currents are interpreted based on different defect models. The commercial simulators are also used as analytical tools to extract defect parameters from measured DLTS (Deep Level Transient Spectroscopy) signals S(T) and capacitance transients C(t).