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How Non-ideality Effects Deteriorate the Performance of Tunnel FETs

Andreas Schenk[1], Saurabh Sant[1], Kirsten Moselund[2], and Heike Riel[2]

[1]Integrated Systems Laboratory, ETH Zurich, CH-8092 Zürich, Switzerland, schenk@iis.ee.ethz.ch

[2]IBM Research-Zurich, Säumerstrasse 4, CH-8803 Rüschlikon, Switzerland

Abstract

Physics-based TCAD simulations of measured vertical and lateral InAs/Si hetero nanowire tunnel FETs are presented to demonstrate the effect of major non-idealities on slope and ON-current. The D_{it} limit for sub-thermal TFET operation is predicted, and it is shown that a high defect density at the InAs/Si interface can result in a slope close to 60 mV/dec due to thermionic emission in an arising MOSFET with the intrinsic Si region as gated channel.

(Keywords: TFETs, steep slope, non-idealities)

Introduction

Non-ideality effects as trap-assisted tunneling (TAT) at interface and bulk traps, roughness of material interfaces, channel quantization, and density-of-state (DOS) tails degrade the performance of TFETs [1]. It is shown by physics-based TCAD simulations how sub-threshold swing (SS) and ON-current are influenced by crucial physical parameters like D_{it}, capture cross sections, relaxation energies, and roughness amplitude. Temperature-dependent measurements of hetero nanowire (NW) TFETs (Fig. 1) provide the input for a quantitative assessment of the D_{it} limit which still guarantees a sub-60 mV/dec slope averaged over 3-4 decades. A new model for the combined effect of channel quantization and interface roughness on line tunneling quantifies the expected smoothening of the sharp onset of tunneling, which otherwise is typical for the 2D-3D DOS matching.

Effect of trap-assisted tunneling

Fig. 2 compares the theoretical band-to-band tunneling (BTBT) current with TAT currents due to generation centers at the InAs/oxide interface (measured parameters used) and at the InAs/Si hetero interface (D_{it} fitted) in one of the lateral devices shown in Fig. 1. The latter current matches the experimental curve at 300 K which has a SS ~ 60 mV/dec [2]. The band diagram in Fig. 3 reveals that the strong TAT generation at the hetero-interface acts like a current source in an internal MOSFET that arises from self-consistent electrostatics where the interface charges in conjunction with the gate voltage create a thermionic barrier to the flow of holes towards the drain. The intrinsic Si channel provides an almost perfect gate control which explains the measured slope. The comparison for two temperatures in Fig. 4 shows three distinct segments of the transfer curve - thermionic emission, TAT, and BTBT – being the bottleneck at low, intermediate, and high V_{GS}, respectively. It is found that $D_{it} < 5e11cm^{-2}eV^{-1}$ at both interfaces is required to reach sub-thermal SS (still caused by TAT) [3].

Effect of surface roughness

Line tunneling (vertical tunnel paths under the gate) is affected by surface roughness because of the effective smoothening of the 2D DOS in the TFET channel. Within Ando's perturbation approach one can model the combined effect of channel quantization and roughness [1]. Fig. 5 presents a test device with predominant line tunneling used to quantify the roughness effect. Simulations performed with different roughness amplitudes Δ and an auto-correlation length L = 1.9 nm are shown in Fig. 6. The DOS smoothening degrades the SS with rising Δ and decreasing L (not shown).

Conclusion

Low defect densities, in particular at interfaces, and smooth semiconductor-oxide interfaces are necessary to achieve sub-thermal slope in InAs/Si NW TFETs. By combining defect characterization, temperature-dependent IV-measurements, and physics-based TCAD simulations one can predict the size of both effects.

Acknowledgments

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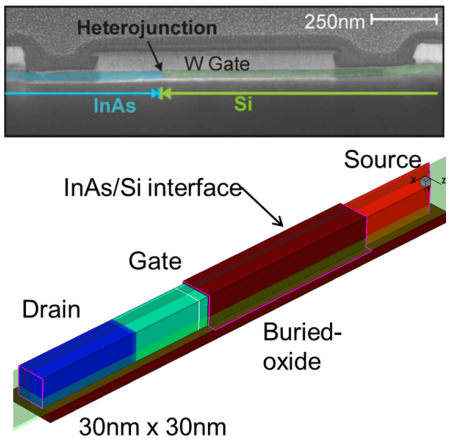

Fig. 1: SEM image of the lateral InAs/Si NW TFET with inclined hetero-interface (top) and 3D simulation domain (bottom).

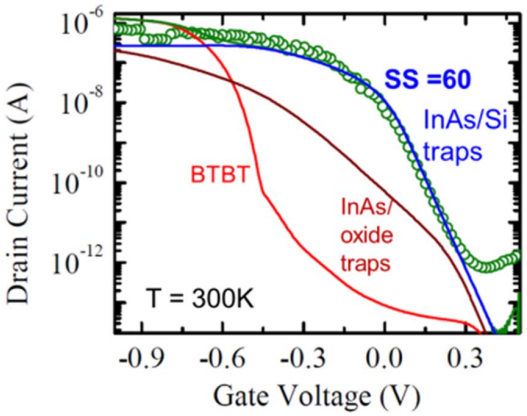

Fig. 2: Individual contributions of BTBT and the two TAT processes to the transfer characteristics of the lateral InAs/Si NW TFET at 300 K. Solid lines: simulation, circles: measurement.

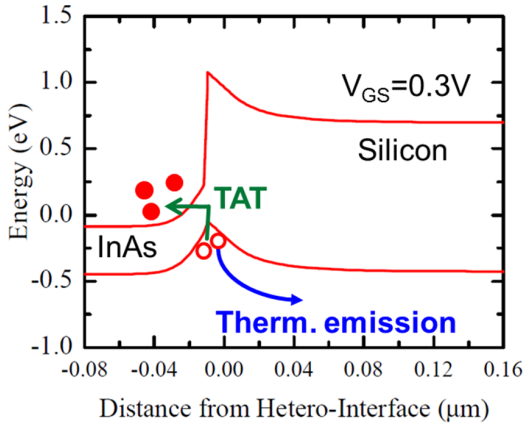

Fig. 3: Band diagram along the channel for three different gate voltages near the onset of the TFET. In case of a high defect density at the InAs/Si interface, transport of carriers happens via two subsequent steps, viz., TAT and subsequent thermionic emission.

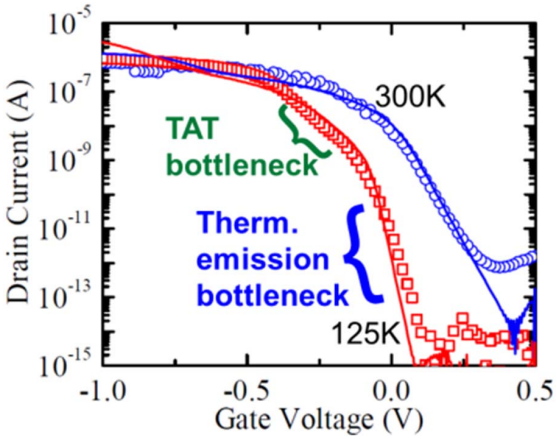

Fig. 4: Transfer characteristics at two different temperatures reveal three distinct intervals of the transfer curve, where the current originates from thermionic emission, TAT, or BTBT, respectively.

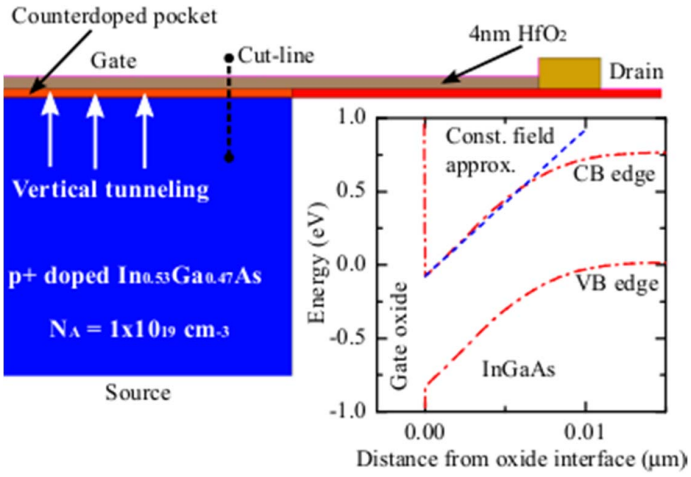

Fig. 5: Left: Simulation domain of an InGaAs vertical TFET with counter-doped pocket. The special geometry suppresses point tunneling and is used to study the combined effect of channel quantization and surface roughness. Right: Band edge diagram at V_{GS} = 0.625V along the cut line perpendicular to the channel.

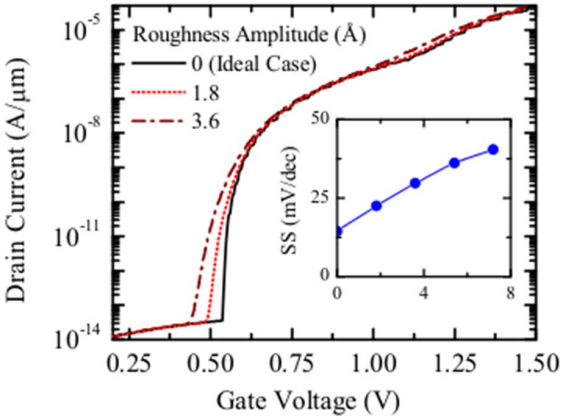

Fig. 6: Transfer characteristics of the vertical TFET in Fig. 5 for different values of the roughness amplitude Δ. Increasing Δ degrades the SS which is plotted in the inset.