Trap-Tolerant Device Geometry for InAs/Si pTFETs

Saurabh Sant and Andreas Schenk

***Abstract*— The influence of channel quantization and interface traps on the performance of InAs/Si pTFETs is analyzed, and a device geometry is predicted which is least sensitive to trap-assisted tunneling (TAT). The good agreement between simulated and measured transfer characteristics validates the reliability of the simulation setup. Simulations show that TAT degrades the sub-threshold swing (SS) of the tunnel field effect transistor (TFET) and that channel quantization reduces its ON-current. The same simulation setup is used to find the device geometry which is least susceptible to interface traps. Scaling down the nanowire diameter below 20 nm inhibits TAT at the oxide/InAs interface. Furthermore, aligning the gate edge with the InAs/Si hetero-junction reduces the degradation of the SS caused by TAT at the hetero-interface. In this way, a gate-aligned InAs/Si nanowire TFET with diameter ∼20 nm can deliver sub-thermal sub-threshold swing even in the unavoidable presence of oxide- and hetero-interface traps.**

***Index Terms*— Channel quantization, interface traps, trap-tolerance, tunnel FETs.**

I. INTRODUCTION

TUNNEL Field Effect Transistors (TFETs), which work on the principle of gate-induced modulation of the band-to-band tunneling (BTBT) process, can overcome the physical limit of the thermal sub-threshold swing (SS) inherent in MOSFETs. Although simulations confirm that ideal hetero-TFETs can achieve sub-thermal SS [1], the fabrication of such switches with sufficient on-current and sub-thermal SS over a few decades of drain current is difficult although not impossible [2]. Simulations have shown that field-induced quantum confinement (also called channel quantization) severely degrades the on-current [3], [4]. On the other hand, non-idealities such as interface traps, interface roughness, and band tails are known to increase the SS. Interface and bulk traps are most detrimental in this respect [5]. The large lattice mismatch between InAs (lattice constant $a_0 = 6.032$ Å) and Si ($a_0 = 5.43$ Å) makes strain relaxation by defect formation at the interface more favorable than gradual strain relaxation. Additionally, the growth of InAs on Si creates antiphase domains in InAs [6]. The result is a high density of states (D_{it}) which could only be avoided by growing extremely narrow InAs nanowires [7]. The lack of a native oxide on InAs causes a large D_{it} also at the InAs/oxide interface [8], [9], although InAs channel MOSFETs with low D_{it} have been reported [10]. Due to a high D_{it} at the InAs/Si hetero-interface, thermionic emission can even become the dominant mechanism in InAs/Si pTFETs thus effectively converting them to MOSFETs [11], [12]. Simulations of these TFETs showed that the D_{it} at *both* InAs/Si and InAs/oxide interfaces must come below 5×10^{11} cm^{-2}eV^{-1} to ensure sub-thermal swing [12] which is tough to achieve. Hence, it is necessary to find a device geometry which is least sensitive to the interface traps.

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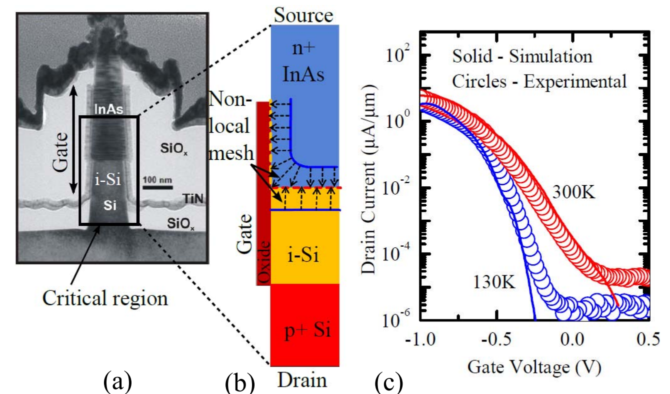

Fig. 1. (a) TEM image of the InAs/Si vertical nanowire TFET (taken from [13]). (b) Radial cross section of the critical region for TCAD simulation. (c) Comparison of experimental and simulated transfer characteristics [25].

In this work, the role of interface traps and channel quantization in the degradation of, respectively, the SS and the on-current of InAs/Si pTFETs is analyzed. Results are compared with measured transfer characteristics, and the simulation set-up is employed to determine the device geometry which is least susceptible to TAT, i.e. *trap-tolerant*.

The fabricated InAs/Si vertical nanowire (diameter ≈ 100 nm) TFETs used for the parameter validation consist of p+ doped Si drain ($N_A = 3 \times 10^{19}$ cm^{-3}), 100 nm long intrinsic Si channel, and 500 nm long n+ doped InAs ($N_D = 2 \times 10^{18}$ cm^{-3}) as shown by the TEM image in Fig. 1(a) [13]. The gate stack is Al_2O_3/HfO_2 with an EOT of 1.3 nm. The critical region of the device is simulated with the semi-classical TCAD package Sentaurus device by Synopsys Inc. [14] (see. Fig. 1(b)). Band gaps in Si and InAs were set to 1.1 eV and 0.36 eV, respectively, and the valence band (VB) offset at the InAs/Si hetero-junction to 130 meV. The latter was extracted from the analysis of

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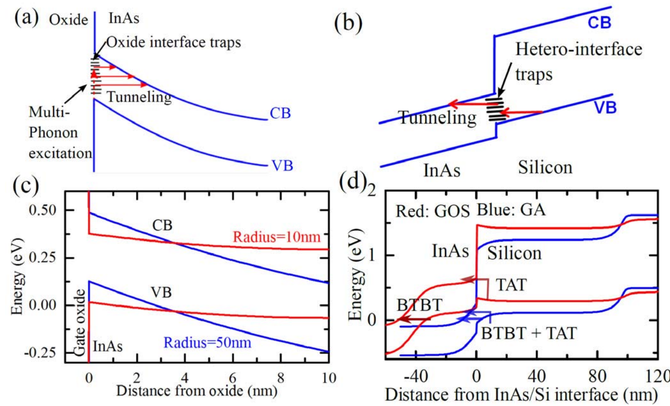

Fig. 2. Schematic band edge diagrams showing TAT at (a) the oxide/InAs interface and (b) Si/InAs interface. (c) Extracted band edge diagrams normal to the oxide/InAs interface at the on-state $V_{GS} = -0.75$ V. A triangular well is absent in the NW with $d = 20$ nm suppressing TAT. (d) Extracted band edge diagrams along the axis of the $d = 20$nm InAs/Si NW pTFET with gate-overlapped-source (GOS) and gate-aligned (GA) geometries at $V_{GS} = -0.5$ V.

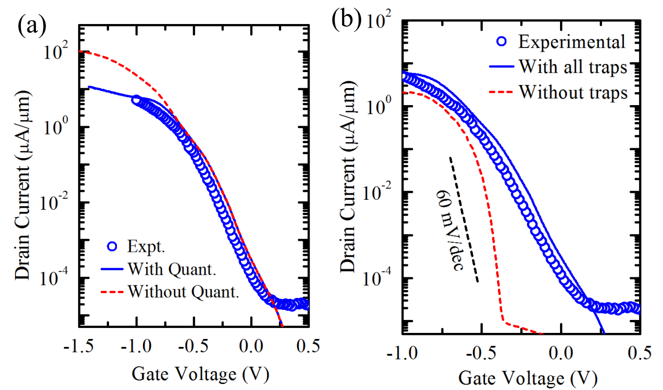

Fig. 3. Comparison of the simulated transfer characteristics (a) with and without channel quantization, and (b) with and without interface traps. Channel quantization lowers the on-current, whereas interface traps degrade the sub-threshold swing in TFETs.

measured InAs/Si tunnel diode characteristics [15]. The gate metal work function was set to 4.8 eV. To account for the effect of quantization in a triangular potential well in the channel on tunneling, a new band-to-band tunneling (BTBT) model based on the path rejection method [4], [16] was implemented using the external Physical Model Interface in the simulator. In this model, a tunnel path is accepted if its energy is above the first sub-band level, but is rejected otherwise. The default dynamic nonlocal path BTBT model was used for the narrow TFET with $d = 20$ nm where the triangular potential well is absent in the channel. Here, electronic states in InAs nanowire ($d = 20$ nm) are quantized due to confinement in a circular quantum well. Calculation of the energy of the first sub-band relative to the bottom of the well gives a value of 85 meV. This energy is added to the CB edge of InAs to mimic the effect of geometrical confinement which is otherwise ignored by Sentaurus device. Size quantization is ignored in Si due to the large effective mass. Both BTBT models require electron and hole effective masses as input parameters. They were set to their values in bulk – $m_e = 0.023\ m_0$, $m_{lh} = 0.026m_0$ for InAs [17] and $m_e = 0.19m_0$, $m_{lh} = 0.15m_0$ for Silicon. This is justified because size quantization notably changes the effective mass only if $d < 15$ nm [18]. Since the CB of InAs is at the Γ-point, direct tunneling is expected to be the dominant tunneling mechanism between the CB of InAs and the VB of Si at moderate electric field [19]. Thus, phonon-assisted tunneling is not considered. The drain current was scaled by the circumference of the nanowire to compare the *IV*-plots at various diameters.

As shown in Fig. 2(a), TAT at the InAs/oxide interface involves multi-phonon excitation of electrons from the VB to the traps and subsequent tunneling to the CB. At the InAs/Si interface, traps can mediate a direct or phonon-assisted tunneling process between the Si VB and the InAs CB as shown in Fig. 2(b). Steady-state occupation of traps results by the principle of detailed balance and affects the electrostatics self-consistently. TAT at interface traps is modeled with the nonlocal model [20]. In its TCAD implementation, the tunnel rate is calculated in WKB approximation with numerical integration over the imaginary dispersion. Traps at the InAs/Oxide interface are assumed to be uniformly distributed in the band gap. A maximum D_{it} of $1\times10^{13}\text{cm}^{-2}\text{eV}^{-1}$ is considered in accordance with [13]. The trap interaction volume which is a measure of the strength of the off-diagonal coupling in the transition probability and acts as a scaling parameter for the generation rate in the nonlocal TAT model is set to 10Å^3. Traps at the InAs/Si hetero interface are located close to the VB edge [12]. The energetic distribution of D_{it} at the InAs/Si interface is assumed to be Gaussian with its peak at the VB edge. A field-induced shift in the trap energy level [21]–[23] is ignored in the analysis. The peak value is set to $1\times10^{13}\text{cm}^{-2}\text{eV}^{-1}$ and the FWHM to 220 meV which, on integration over energy, gives a trap density of 2.7×10^{12} cm^{-2}. This corresponds to approximately one trap per circular disk with a radius of 3.4 nm. Transmission Electron Microscopy (TEM) analysis of the InAs/Si interface reported by Tomioka *et al.* [24] reveals a periodic arrangement of dislocations with ∼3 nm spacing. If each dislocation contributes one trap level, the calculated D_{it} agrees well with the value used here. The trap interaction volume is fitted to 50Å^3.

The comparison of simulated and measured transfer characteristics of the fabricated TFET is shown in Fig. 1(c). Fig. 3(a) presents the effect of channel quantization, revealing a severe lowering of the on-current. Only this can attune simulated and measured curves, which provides some confidence that the quantization effect is indeed present in these devices. The reduction of the on-current in the presence of channel quantization is due to the rejection of shorter tunnel paths which leads to an increase of the average tunnel length and reduces the BTBT rate. Fig. 3(b) depicts the impact of TAT on the swing at 300 K. In the sub-threshold region, the drain current is entirely dominated by TAT with negligible contribution from BTBT. The $I_D - V_{GS}$ curve at a lower gate bias is solely degraded by surface SRH generation. With increasing voltage, i.e. sufficient band bending, tunneling from trap levels into the CB (Fig. 2(a)) starts to become effective. Since the tunnel rate between trap and CB states is much larger, multi-phonon excitation becomes the bottleneck. As multi-phonon excitation exhibits a small field enhancement compared to

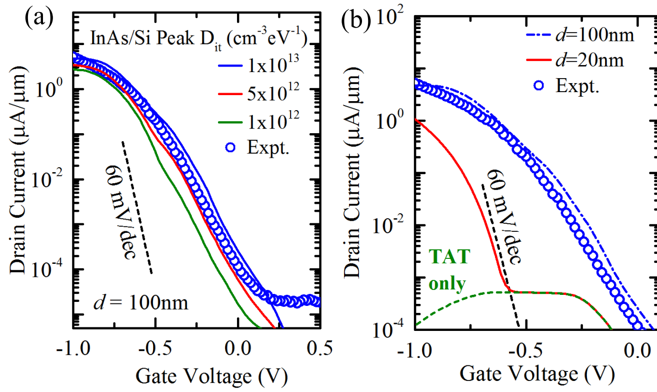

Fig. 4. (a) Effect of passivating the InAs/Si hetero-interface in the InAs/Si pTFET ($d = 100$ nm). The SS remains large despite reducing the D_{it} at the InAs/Si interface. (b) Simulated transfer characteristics of the InAs/Si pTFET with $d = 100$ nm and 20 nm. Contribution of hetero-junction TAT ($d = 20$ nm) is plotted in dashed green.

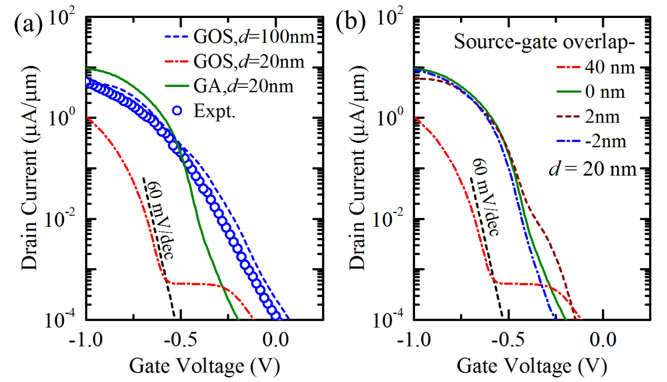

Fig. 5. (a) Simulated transfer characteristics of the GOS and GA TFETs. The leakage floor disappears in case of the GA TFET. (b) Effect of a gate-source misalignment of $+/-2$ nm in the GA TFET.

zero-phonon trap-to-band tunneling, the drain current increases sluggishly resulting in a strong SS degradation. At 300 K, the contributions of InAs/Si and InAs/oxide TAT to the total sub-threshold drain current are of similar magnitude. On the other hand, at 130K the contribution of InAs/oxide traps becomes negligibly small due to the suppression of multi-phonon excitation of electrons from the VB. As a result, hetero-interface TAT is dominant in the sub-threshold region which reduces the SS at lower temperatures. Since both the InAs/oxide and InAs/Si traps contribute to the total current at 300 K, the D_{it} at both interfaces must be suppressed to achieve a sub-thermal swing.

Simulation of the NW TFETs using different D_{it} at the InAs/Si interface confirms that, passivation of the InAs/Si interface alone would not yield a sub-thermal SS (see Fig. 4(a)). Therefore, other techniques to suppress TAT must be explored. Although traps at the InAs/oxide interface cannot be passivated, their contribution to the drain current via TAT can be reduced by decreasing the NW diameter d to 20 nm. This results in the steep $I_D - V_{GS}$ plots shown in Fig. 4(b). The NW TFET with $d = 100$ nm undergoes surface inversion (see Fig. 2(c)) which creates a triangular-like potential well at the InAs/oxide interface. TAT is significantly enhanced at such a well due to tunneling between traps and the CB edge. On the other hand, the TFET with $d = 20$ nm undergoes volume inversion resulting in flat band conditions at the InAs/oxide interface (see Fig. 2(c) for comparison). In the latter case, only multi-phonon excitation can take place, TAT is inhibited due to insufficient band bending. Note that, due to the nearly flat bands at the InAs/oxide interface, the effect of channel quantization is absent in the TFET with $d = 20$ nm. Therefore, the default BTBT model is used instead, and the energy of the first sub-band is added to the CB edge. Electrostatic screening of the channel by the oxide interface traps [26] is still present. However, it does not degrade the SS as strongly as TAT. In this way, diameter scaling can bring down the minimum point swing from 157 mV/dec ($d = 100$ nm) to 68mV/dec ($d = 20$ nm).

Although the diameter scaling suppresses TAT at the oxide interface, TAT at the InAs/Si hetero-junction continues to happen creating a leakage basin of the TAT current at the onset of BTBT in the pTFET. Since the lateral electric field at the hetero-interface saturates in the GOS TFET when volume inversion begins, the hetero-TAT current also saturates at 10 nA/μm (see Fig. 4(b)). This high value makes the TFET incapable for low-power application. To overcome this drawback, the gate must be aligned with the InAs/Si hetero-interface. Simulation results for the NW TFET ($d = 20$nm) with gate alignment (GA) and with gate-overlapped-source (GOS) geometry are compared in Fig. 5(a). It may be inferred from the IV-plots that the gate alignment advances the onset of BTBT in the TFET. As seen from the band edge diagram along the axis of the two TFETs in Fig. 2(d), BTBT takes place at the source end of the gate in the GOS TFET, but at the InAs/Si hetero-interface in the GA TFET. Therefore, in the GOS geometry, BTBT begins only when the entire GOS region undergoes volume inversion which happens at a higher gate bias. This results in a delayed onset of BTBT relative to TAT which causes the leakage basin. On the contrary, in the GA geometry, BTBT begins as soon as accumulation starts in the i-Si channel. Hence, the onset of hetero-junction TAT coincides with the onset of BTBT (see Fig. 2(d)). The simultaneous onset of TAT and BTBT in GA TFETs improves the point SS to ~59 mV/dec (from 69 mV/dec in GOS geometry). More importantly, it results in a lower leakage floor. Additionally, the GA geometry yields a higher on-current compared to the GOS geometry. In the former, BTBT takes place at the hetero-interface which offers a lower tunnel barrier due to the staggered band alignment at the interface. The transfer characteristics in Fig. 5(b) imply that already a small gate-source overlap degrades the SS. The SS is almost unaffected if an underlap is present between gate and source.

In conclusion, since the suppression of oxide- and hetero-interface traps is difficult, "trap-tolerant" TFET geometries need to be explored. In the case of an InAs/Si nanowire TFET, diameter scaling down to 20 nm would minimize TAT at the oxide-interface and gate alignment would avoid the leakage basin arising from the hetero-TAT when the defects are confined at the hetero-interface. The above approach may also be applicable to TFETs with other material systems.

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