Comparative Simulation Study of InAs/Si and All-III-V Hetero Tunnel FETs

A. Schenk[a], S. Sant[a], K. Moselund[b], and H. Riel[b]

[a] Integrated Systems Laboratory, ETH Zürich, Gloriastr. 35, 8092 Zürich, Switzerland
[b] IBM Research-Zurich, Säumerstrasse 4, 8803 Rüschlikon, Switzerland

Two different nanowire tunnel FETs, based either on the InAs/Si or the $In_{0.53}Ga_{0.47}As$/InP hetero-system, are investigated by device simulation. Variations of radius, equivalent oxide thickness, local doping, valence band offset, temperature, and the effect of trap-assisted tunneling on the sub-threshold slope and the on-current of the transistors are demonstrated.

Introduction

The Tunnel Field Effect Transistor (TFET) which utilizes the band-to-band-tunneling (BTBT) generation current of a gated pin-diode is regarded as promising candidate for ultra-low power circuits due to its potential sub-thermal slope which could enable a strongly reduced supply voltage (1). III-V/Si hetero junctions have been proposed for an improved on-current as compared to Si TFETs (2). Using small-gap semiconductors like InAs or $In_{0.53}Ga_{0.47}As$ as source material increases the tunnel rate, while the wide band gap of the channel/drain materials Si or InP reduces ambipolar leakage. Nanowires (NWs) enable a good electrostatic control due to the surrounding gate and result in an efficient strain relaxation when the diameter is scaled down (3). Tomioka et al. and Björk et al. successfully integrated InAs NWs on Si by nanometer-scale hetero epitaxy based on selective area growth within patterned oxide films (4,5,6,7,8). Recently, Borg et al. demonstrated a new approach to integrate individual InAs/Si hetero-structure NW TFETs onto Si using selective epitaxy in nanotube templates. This approach allows to start with Si substrates of any crystalline orientation and to scale the diameter of the NWs down to reasonable limits (9). First p-type TFETs fabricated by this technology showed an overall performance with on-currents, I_{on} of $6\,\mu A/\mu m$ ($|V_{GS}| = |V_{DS}| = 1\,V$) and a room-temperature subthreshold swing (SS) of ~160 mV/dec over at least three orders of magnitude in current (10). Temperature-dependent measurements indicated that the SS is limited by traps (10). The present simulation study is based on the geometry (see Figure 1), the measured IV-characteristics, and the limited electrical characterization of these devices.

Mesa-like InGaAs n- and p-type TFETs were fabricated by a couple of groups (11,12). Zhao et al. pointed out three factors that degrade the SS: (i) a too high source doping level which screens the gate field and weakens the coupling between the semiconductor and the gate, (ii) a poor III-V/oxide interface with a mid-gap interface trap concentration of $\sim 4 \times 10^{12}/eV/cm^2$, and (iii) the dopant diffusion at the tunneling junction interface which has the same consequence as (i). Below, these issues will be picked up in detail by device simulation. An n-type $In_{0.53}Ga_{0.47}As$/InP hetero-junction TFET with mesa-like fabrication process was reported by Zhou et al. (13). As the $In_{0.53}Ga_{0.47}As$/InP hetero-

system is perfectly lattice-matched, a much smaller interface trap concentration can be expected compared to InAs/Si where the 11% mismatch leads to the formation of dislocation pattern (6,14). However, a drawback of the $In_{0.53}Ga_{0.47}As/InP$ hetero-system is given by the thermionic barrier due to the band offsets which degrades the SS at intermediate gate bias. This drawback must be overcome by introducing a layer of InGaAsP alloy graded from $In_{0.53}Ga_{0.47}As$ on one end to InP on the other end.

Technology-computer-aided design (TCAD) can help to understand the behavior of hetero nanowire Esaki diodes and TFETs, and can give guidelines to improve their performance by optimization of geometry, doping, composition, gating, and biasing. The best approach is to use an atomistic, 3D quantum transport tool (15,16,17,14). Unfortunately, the dimensions of real TFETs prohibit the application of such tools. Instead, drift-diffusion transport codes are widely used. In this paper, all simulations are performed with the commercial device simulator Sentaurus-Device (S-Device) which is equipped with various local and non-local BTBT models (18). Although certain aspects (e.g. size and channel quantization, band gap narrowing, DOS tails) cannot be modelled adequately, predictive trend simulations are possible after careful calibration of the parameters of the tunnel model by comparison with experimental data or with results of pseudo-potential calculations (19).
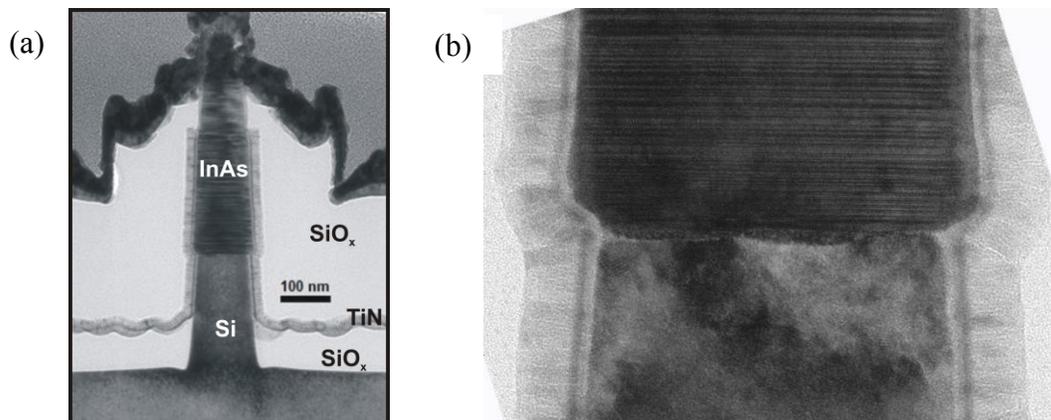
Figure 1: TEM image of an InAs/Si nanowire p-TFET also showing the geometrical dimensions (a). Close-up of the InAs/Si interface which is not smooth across the entire junction area and has a high density of defects (b). Also visible are stacking faults caused by the change in crystal structure of InAs between wurtzite and zincblende.

The remainder of the paper is organized as follows: After introducing the device and the TCAD model, comparisons between simulated and measured $I_D V_{GS}$-characteristics of p-type InAs/Si hetero NW TFETs are shown for different temperatures. The impact of trap-assisted tunneling and the effect of dopant diffusion at the interface are then discussed. Finally, using identical geometries and the optimum source doping, a detailed comparative analysis of $In_{0.53}Ga_{0.47}As/InP$ versus InAs/Si hetero NW TFETs is presented. Key parameters like NW radius and equivalent oxide thickness are varied for this.

Simulation Set-up and TCAD Model

The hetero-structure p-TFETs with nanowire geometry were simulated using the commercial TCAD simulator S-Device (18). The InAs/Si hetero-junction TFETs consist

of InAs as source material and Si as intrinsic layer and drain material. Similarly, InGaAs/InP TFETs have InGaAs as source material and InP as intrinsic-layer and drain material. The source is n+ doped to $2x10^{18}$ cm^{-3} in the case of InAs and $8x10^{18}$ cm^{-3} in the case of InGaAs. These doping levels minimize the SS of the TFETs with respective materials. The drain region is p+ doped to $3x10^{19}$ cm^{-3} in both TFETs. A 100 nm long section of the source is overlapped to the gate. Therefore, the TFET can be categorically called a Gate-overlapped-Source p-TFET. The radial cross section of the simulated nanowire TFET is shown in Figure 2 along with the dimensions. In order to avoid a thermionic barrier at the InGaAs/InP interface, a graded layer of InGaAsP is introduced. The mole fraction of the constituents in this layer is graded from InGaAs at one end to InP at the other end. The device is simulated in the cylindrical coordinate system which essentially converts the radial cross section in Figure 3 to a nanowire by horizontally rotating the structure around the left edge.

The BTBT in semiconductors is modeled using the "Dynamic nonlocal path BTBT model" which is an implementation of Kane's theory of BTBT. In this model, tunnel paths are created which start from the valence band edge in the direction of the electric field and connect the conduction band edge at the same energy. The BTBT rate of electrons is calculated by using the WKB approximation and integrating over imaginary bands along the tunnel paths. The BTBT model can accurately reproduce the transfer characteristics of the TFETs in the subthreshold region. BTBT can take place between heavy hole (HH) band and conduction band (CB) or between light hole (LH) band and CB. As the effective mass of holes in the HH band is much larger compared to that in the LH band, tunneling from the HH band is completely suppressed. Therefore, it is neglected in the simulations.

Figure 2: Device geometry of the simulated hetero-junction TFET.

The BTBT model requires the direct and indirect band gaps of the semiconductors along with their effective electron and hole masses. The direct and indirect band gaps, electron and hole effective masses of InAs, InGaAs and InP at 300K were taken from Ref. (20). All these values as well as the values of other parameters are provided in Table I. The band diagrams at the InGaAs/InP and InAs/Si hetero-interfaces are schematically shown in Figure 3. The InGaAs/InP material system has been extensively studied experimentally, and measured CB offsets were found to range from 0.21 eV to 0.3 eV (21,22,23). In this work, the CB offset is set to 0.27 eV following Ref. (24) which reports ab-initio calculations of the material system. The VB offset of the InGaAs/InP hetero-system is fixed to 0.33 eV. For the InAs/Si material system no experimental band offsets are available to date. Anderson's rule (25) gives a VB offset of 80 meV. Preliminary ab-initio DFT calculations of the InAs/Si band offset yielded a value of ~210 meV (26). For the comparative simulation study both values are used.

In addition to the BTBT model, Shockley-Read-Hall (SRH) generation was activated to account for the thermal generation current ("leakage") in the off-state. Lifetimes of 1 ns are used for InAs. These values yielded the best fit to the temperature dependence of reverse characteristics of unintentionally doped InAs/Si hetero NW diodes measured in Ref. (27). The same values are taken for InGaAs and InP. As the TFET turns on, an inversion layer is formed under the gate overlapped with the source region. A semi-classical model - modified local density approximation (MLDA) - is used to mimic the quantum-mechanical charge redistribution under the gate (28).

TABLE I. Parameters required for BTBT model and typical parameters used for interface traps.

Parameters	InGaAs/InP		InAs/Si	
	InGaAs	InP	InAs	Si
m_C	0.043	0.079	0.023	0.15
m_V	0.052	0.12	0.026	0.19
Degeneracy	2	2	2	2
Huang-Rhys factor	0.4	0.4	0.4	3.5
Phonon energy	0.03	0.03	0.03	0.068
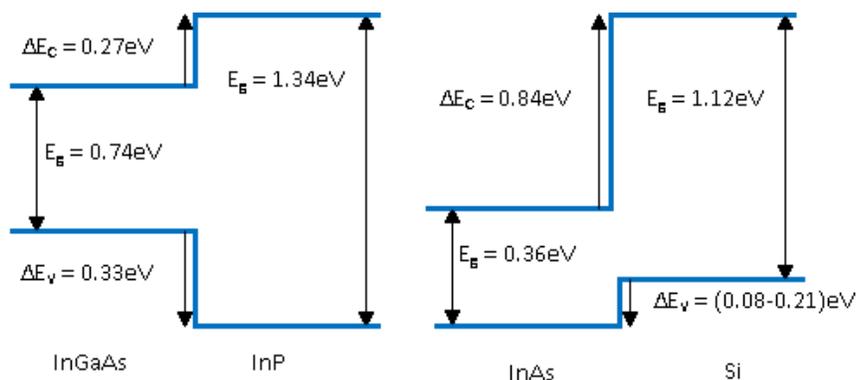
Figure 3: Band alignment at the hetero-interface.

A source-drain bias of -0.5 V is used in all the simulations targeting application with a supply voltage of 0.5 V. As long as this bias is applied at the drain contact (source grounded), the $I_D V_{GS}$ currents are practically independent of it. Slight changes are only observed at the highest current levels. The off-voltage is defined as the voltage at which the drain current exceeds 2×10^{-14} A. The average SS is calculated by averaging the SS over four decades above the off-current. The on-current is calculated at the gate voltage which is by 0.5 V larger than the off-voltage.

Comparison with Experimental Data

$I_D V_{GS}$-characteristics

The measured and simulated transfer characteristics, $I_D V_{GS}$, for the InAs/Si hetero-junction TFET are shown in Fig. 4 for two different temperatures. The measured RT on-current is 1.62 μA (~ 5.2 μA/μm) at $|V_{GS}| = 1.0$ V, $|V_{DS}| = 0.5$ V and the Ion/Ioff ratio is ~10^6. The steeper SS obtained at 130 K clearly proves the presence of traps, which limit sub-60mV/decade operation. The measured average SS at RT is 157 mV/dec, in contrast

to the simulated value of ~32 mV/dec for Δ_{VB} = 80 meV (averaged over 3 decades). One problem in comparing simulated and measured transfer characteristics is the unknown work function. One could fit it (including the neglected effect of channel quantization) if the thermal generation current would be lower than the BTBT current over the entire V_{GS}-range, by using the position of the minimum of the ambipolar IV curve. In reality, the SRH generation current which becomes field-assisted for $|V_{GS}|$ > 0.1 V obscures this minimum and prevents a fit of the work function. This also prevents a clear assessment of the ratio of simulated and measured on-currents. In Figure 4 the work function was set to 4.55 eV which is an arbitrary value. Nevertheless, the simulated on-current seems to be higher than the measured one, although a series resistance effect due to the low mobility in InAs (μ_n = 400 cm²/Vs used) is already included in the simulation. The mobility in comparable InAs NWs has been measured in Ref. (29) and the effect on the on-current of InAs/Si NW Esaki diodes was shown in (30). The simulation for RT reveals a transition from dominating point tunneling to dominating line tunneling visible as shallow buckle at about -0.95 V. The temperature effect on the line tunneling current is determined by the change of the InAs band gap with temperature. It agrees well with the measured temperature effect at V_{GS} = -1 V. Different valence band offsets result in largely different IV curves. A larger valence band offset facilitates an earlier onset of BTBT, i.e. at a lower $|V_{GS}|$ and hence at a lower field, which also leads to a steeper slope. In contrast, a smaller valence band offset delays the opening of the tunnel window, and as band alignment requires a higher field here, the slope at the onset is weaker.

Simulated Effects of Bulk Traps and Dopant Diffusion

The strong temperature dependence of the drain current at low and intermediate gate voltages hints to a field-enhanced thermal generation process which is conventionally called "trap-assisted tunneling (TAT)" in literature. Figure 5 shows results obtained with a physics-based TAT model based on the theory of multi-phonon transitions at deep centers in an electric field (31). The model implementation in S-Device assumes single mid-gap levels and requires a minimum set of parameters: Huang-Rhys factor S, effective phonon energy $\hbar\omega_{ph}$ (lattice relaxation energy ε_{rel} = $S\hbar\omega_{ph}$), and two tunnel masses. The interplay between tunneling and thermal generation enhances the field effect for weak electron-phonon (el-ph) coupling (small ε_{rel}) whereas increasing el-ph coupling shrinks the field enhancement. This is demonstrated in Figure 5 using homogeneous lifetimes $\tau_{n,p}$ =1 ns. For weak el-ph coupling (ε_{rel} = 12 meV) TAT dominates the $I_D V_{GS}$-curve up to $|V_{GS}|$ = 1 V. The SS increases with increasing el-ph coupling.

Another cause for the discrepancy between measured and simulated slope could be the out-diffusion of Si atoms during processing. In the InAs source the Si atoms would act as donors when incorporated on regular lattice sites. Even if the highly doped layer formed at the interface is thin, it has a pronounced effect on the electrostatics. The gate field in the region of the pn-junction becomes strongly screened which degrades the gate control of BTBT and, hence, the transconductance. The circles in Figure 5 were obtained with a 6 nm thin layer of $5 \times 10^{19} cm^{-3}$ n-doping. Inspection of the BTBT rate reveals that line tunneling under the gate is delayed and only turns on at very high $|V_{GS}|$. A fit to the measured data would require a substantial increase of the work function used in the simulation.
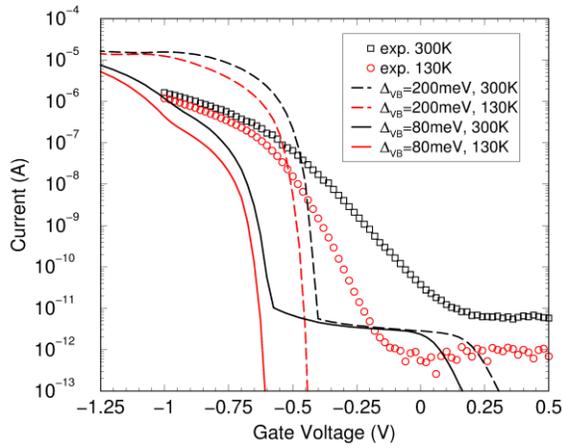
Figure 4: Measured and simulated $I_D V_{GS}$-characteristics of the InAs/Si hetero-junction TFET shown in Fig. 2 for two different temperatures and two different values of the valence band offset Δ_{VB}. The metal work function was set to 4.55 eV.
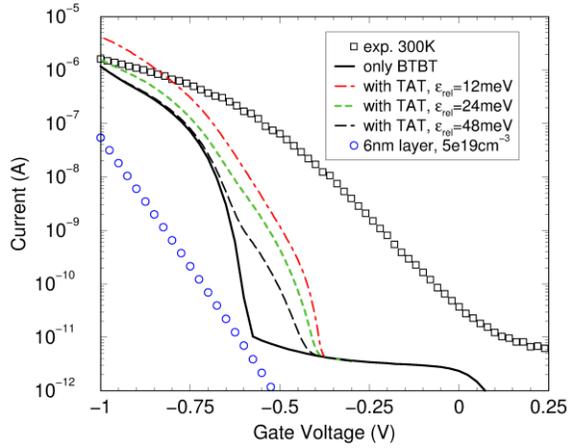
Figure 5: Simulated TAT currents at 300 K due to bulk traps in InAs for different values of the lattice relaxation energy (broken lines). Effect of a highly doped layer with 6 nm thickness at the interface (circles).

Performance Analysis: InAs/Si TFET versus In$_{0.53}$Ga$_{0.47}$As/InP TFET

Line Tunneling versus Point Tunneling

The radial cross section of the gate-overlapped-source region of the TFET is shown in Figure 6 along with a color-mapped diagram of BTBT rate of both electrons and holes in the device. In the InGaAs/InP TFET, the tunnel direction of the electrons is perpendicular to the gate and the tunneling electrons do not cross the pn-junction. In contrast, electrons in the InAs/Si TFET tunnel predominantly parallel or inclined to the gate and BTBT mostly happens across the pn-junction. This difference in the prominent tunnel direction in different hetero-structures is a consequence of the different band alignments at the interface of the materials as shown in Figure 3. It is explained below.
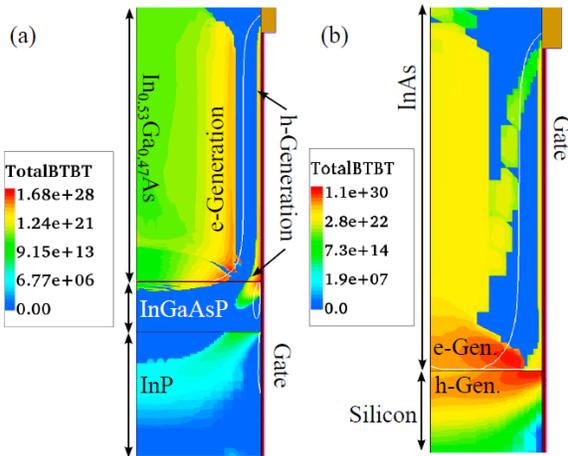
Figure 6: Color-mapped diagrams of the radial cross sections of (a) InGaAs/InP TFET and (b) InAs/Si TFET showing the BTBT rates of electron and hole generation. At the onset of line tunneling (normal to the gate), the inter-material point tunneling is absent in the InGaAs/InP TFET, while it is already dominant in the InAs/Si TFET.

Under applied drain bias, the device acts as a reverse-biased diode when the gate is floating. As the (negative) gate voltage is ramped up, an inversion layer of holes begins to form in the heavily n-type source region adjacent to the gate. Similarly, the band edges of the intrinsic Si layer bend upwards due to the negative potential at the gate. For sufficiently negative gate bias, the VB edge of Si in the intrinsic region energetically aligns with the CB edge of InAs in the source. As a result, tunneling of electrons begins from the VB edge of Si to the CB edge of InAs (often called "point tunneling" in the literature). If the bias is further increased, the rate of point tunneling enhances as the tunnel window widens. At the same time, as a result of the MOS effect, the band bending under the entire gate region increases to the extent that the VB edge of InAs adjacent to the gate energetically aligns with the CB edge of InAs in the bulk. This induces vertical tunneling of electrons from the channel to the bulk InAs (often called "line tunneling" in the literature). In short, since the tunnel gap (the difference between CB edge of InAs and VB edge of Si) at InAs/Si interface is smaller than the InAs gap, point tunneling begins earlier than line tunneling in the InAs/Si TFET and is the dominant mechanism. On the contrary, at the InGaAs/InP interface the tunnel gap (the difference between CB edge of InGaAs and VB edge of InP) is larger than the band gap of InGaAs which delays and suppresses point tunneling in InGaAs/InP TFETs. Therefore, line tunneling is the dominant tunneling mechanism in InGaAs/InP TFETs.

In conclusion, the type-II band alignment at the InAs/Si interface makes point tunneling dominant, whereas the type-I band alignment at the InGaAs/InP favors line tunneling. The dominance of point tunneling grows with shrinking tunnel gap at the InAs/Si interface. Similarly, the wider the tunnel gap at the InGaAs/InP interface, i.e. the larger the VB offset, the more dominant the line tunneling. The different tunnel directions in the two hetero-structures affect the impact of gate oxide scaling as well as diameter scaling on the performance of NW p-TFETs.

Effect of Gate Oxide Scaling

Scaling the gate oxide thickness increases the oxide capacitance and improves the gate control. A better gate control results in a sharper switching of the device, i.e. it improves the SS. A limitation to gate oxide scaling is set by gate tunneling leakage which prevents to use oxides with an Equivalent Oxide Thickness (EOT) significantly smaller than 1nm. Hence, high-k dielectrics are suitable for aggressive EOT scaling, as they deliver high gate-capacitance with thicker oxide compared to SiO_2. In this paper, all gate oxide thicknesses are referred to EOT, and SiO_2 with a given EOT in the range from 0.5 nm to 2.0 nm is used in the simulation. Gate tunneling is disregarded.

The effect of oxide thickness on the device characteristics is shown in Figure 7 demonstrating the improvement of SS with EOT scaling because of the enhanced gate control. This effect is observed irrespective of the materials of the hetero-structure, but is much stronger for InGaAs/InP TFETs than for InAs/Si TFETs. Line tunnel paths which start at the gate are most sensitive to the gate-induced electric field. The described effect also results in a strong increase of the on-current of the InGaAs/InP TFET, whereas the on-current of the InAs/Si TFET remains more or less unaffected. The weak sensitivity of the InAs/Si TFETs to gate oxide scaling could possibly due to the saturation of the BTBT rate.

Effect of Nanowire Diameter Scaling

Reducing the diameter improves the gate control of the NW. As explained above, this effect should result in an improvement of the SS. However, the different dominant tunnel directions in the two TFETs give birth to a variety of effects which impact the trends for the SS.

NW diameter scaling covers the range from 30 nm to 130 nm in this study, which avoids extremely narrow NWs where size quantization has a strong effect on the TFET performance. In the case of InAs/Si, shrinking the diameter indeed slightly improves the SS as shown in Figure 8. Shrinking the diameter reduces the circumference of the nanowire as well as its cross-sectional area. This offers less area for tunneling of electrons and reduces the on-state current of InAs/Si TFETs. For all diameter values down to 30 nm, tunneling mainly happens via point tunnel paths at the InAs/Si interface. For diameters greater than 40 nm, point tunneling is followed by line tunneling in the source region normal to the gate as explained earlier. This is shown in Figure 9(a) for a diameter of 100 nm. It is the result of surface inversion in which a depletion layer forms under the gate with increasing gate bias. This is followed by the formation of a hole inversion layer close to the gate. Due to the strong band bending, valence electrons tunnel from the inversion layer to the bulk and holes are generated in the inversion layer as shown in Figure 9(a). However, at a diameter of ~40 nm volume inversion takes place and line tunneling in the channel is no longer possible. Instead, BTBT begins at the upper edge of the gate as shown in Figure 9(b).
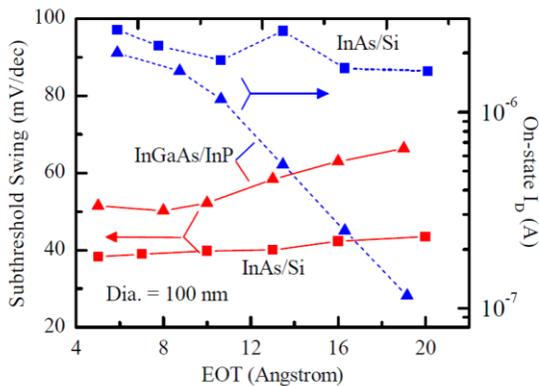
Figure 7: Variation of SS (solid lines) and on-state current (dotted-lines) with EOT. A decreasing EOT improves the gate control of the device resulting in better SS and on-current.
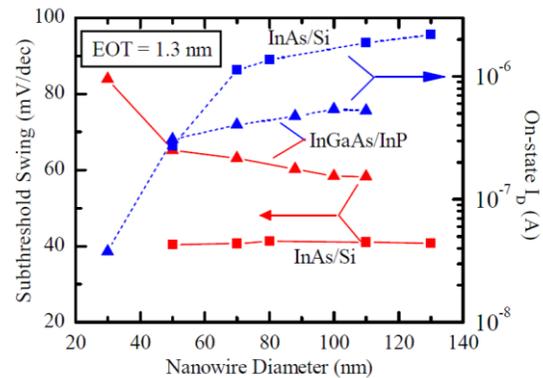
Figure 8: Impact of nanowire diameter scaling on SS (solid lines) and on-current (dotted-lines). Diameter scaling slightly improves the SS of InAs/Si TFETs while it degrades the SS of InGaAs/InP TFETs.
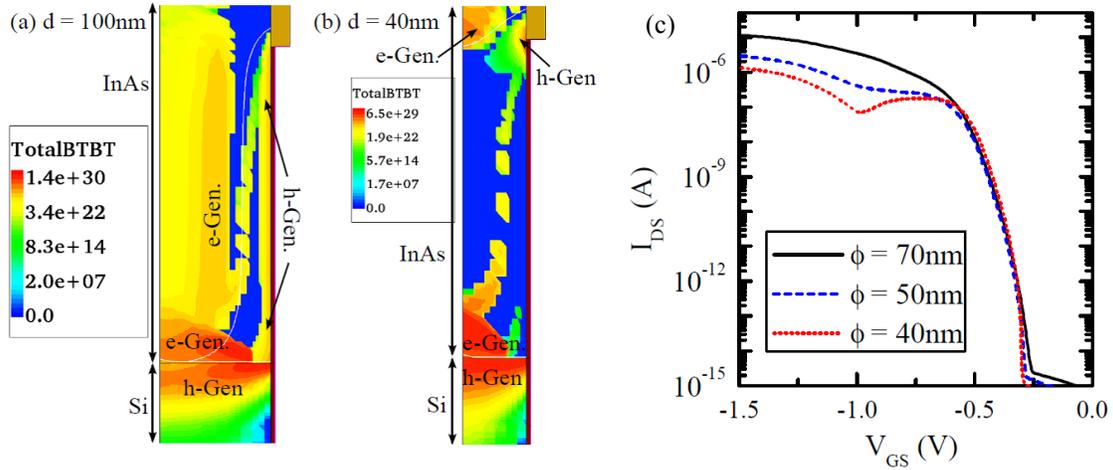
Figure 9: BTB electron and hole generation rate in InAs/Si TFETs for a diameter of (a) 100 nm and (b) 40 nm. Line tunneling takes place in the 100 nm thick nanowire due to surface inversion. For d = 40 nm, volume inversion occurs and the BTBT rate is located at the hetero-interface as well as at the upper gate edge. (c) Transfer characteristics of the TFETs for some peculiar diameters. The pronounced buckle in the case of d = 40 nm is caused by the onset of volume inversion.

For a deeper understanding of the above-described effect, color-mapped diagrams of the BTBT rate in the NW with 30 nm diameter are shown in Figure 10. At small gate bias (Figure 10(a)) only point tunneling at the InAs/Si interface sets in because of the small tunnel gap at the interface. At an intermediate gate bias (Figure 10(b)), volume inversion takes place and strong BTBT starts at the upper gate edge. Note that point tunneling at the InAs/Si interface has not yet ceased. Further increase in the gate bias flattens the bands along the diameter which suppresses point tunneling at the InAs/Si interface as shown in Figure 10(c). The drain current drops sharply, similar as for the InGaAs/InP NW TFET in Figure 11(d).

In the case of InGaAs/InP TFETs, in spite of the improved gate control, the SS slightly worsens by shrinking the diameter down to 50 nm. This seems to be a consequence of the gradual shift from surface inversion to volume inversion. At the diameter of 30 nm, the nanowire is so narrow that volume inversion starts without initial surface inversion and BTBT only occurs at the upper gate edge. This degrades not only the SS but also the magnitude of the on-current as shown by the transfer characteristics in Figure 11(d).
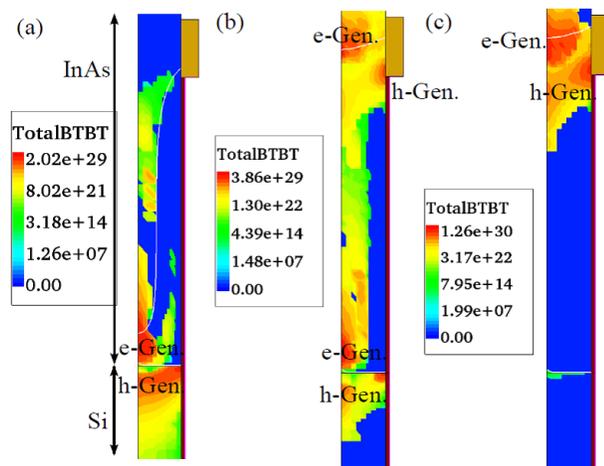
Figure 10: BTB electron and hole generation rates in a NW with d = 30 nm (a) after the onset of tunneling (b) at an intermediate gate bias, and (c) under high gate bias.
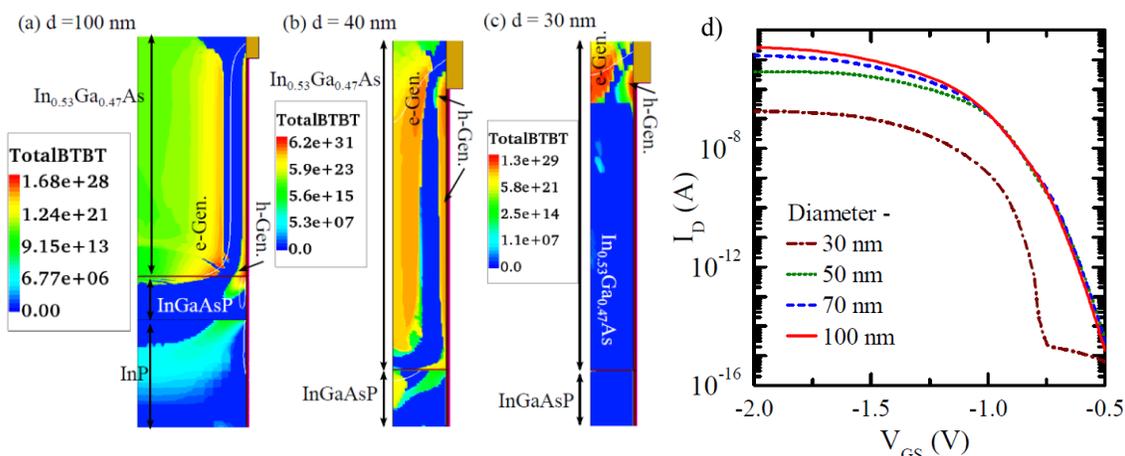
Figure 11: BTB generation rates in InGaAs/InP nanowire TFETs with diameters of (a) 100 nm, (b) 40 nm, and (c) 30 nm. In a 100 nm thick NW, the BTB generation rate is evenly spread over the channel region with some maximum at the interface while that in a 40 nm thick NW is concentrated along the upper part of the channel. The distributed line tunneling under the gate completely vanishes in the 30 nm thick NW TFET due to volume inversion. The corresponding $I_D V_{GS}$-characteristics are shown in (d).

Effect of Traps at the Material Interface

The interface of two semiconducting materials often gives rise to a large trap concentration. This could be attributed to the presence of irregular bonds between the atoms of the two materials. If the two semiconductors are lattice-mismatched, the trap concentration can increase by orders of magnitude. Among the two hetero-structures under consideration, the InAs/Si hetero-structure with relaxed InAs ($a_0 = 0.605$ nm) and Si ($a_0 = 0.543$ nm) is highly mismatched while the $In_{0.53}Ga_{0.47}As$ alloy is lattice-matched to InP ($a_0 = 0.586$ nm). The InAs/Si interface is, therefore, expected to have a much larger interface trap density compared to the InGaAs/InP interface. In addition to that, both material sets can have electrically active bulk traps distributed throughout the material as discussed above. In particular, the stacking faults found in the InAs NW might be responsible for low lifetimes.

Simulations were performed to test the sensitivity of the TFET transfer characteristics to interface traps. A density-of-states of interface traps (D_{it}) of 2×10^{13} cm^{-2}eV^{-1} was used for both interfaces, although the InAs/Si interface is expected to suffer from a much higher defect density than the InGaAs/InP interface. The energetic trap distribution in the band gap was assumed to be uniform. The "Dynamic nonlocal path TAT model" in S-Device was activated in the simulations. Details of the model can be found in (18). TAT acts as an additional electron-hole pair generation mechanism in TFETs which sets in prior to BTBT due to the lower tunnel barrier. As discussed above, the large inter-material tunnel gap at the InGaAs/InP interface suppresses the inter-material "point tunneling", whereas the small tunnel gap at the InAs/Si interface favors "point tunneling". Therefore, it is obvious that point tunneling (in which the tunnel paths cross the interface) is more sensitive to interface traps than line tunneling. This is observed in the simulation

of the two TFETs. The transfer characteristics of the TFETs with and without TAT are shown in Figure 12. The leakage current is higher for the InAs/Si TFET than for the InGaAs/InP TFET which suggests that InGaAs/InP hetero-structure based TFETs are less sensitive to interface traps. A much smaller D_{it} in the case of InGaAs/InP would practically remove the effect of TAT.
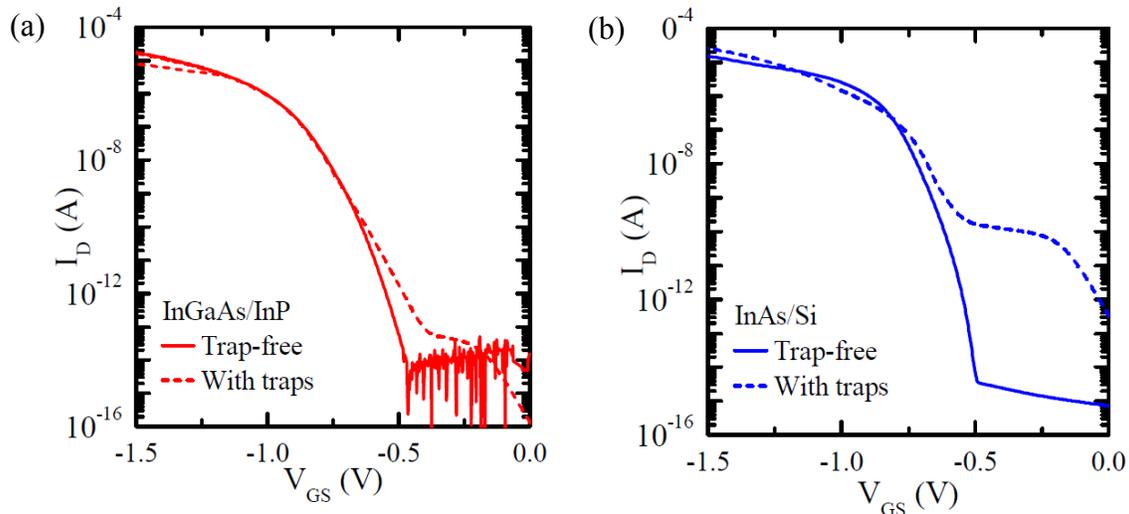
Figure 12: Transfer characteristics of (a) InGaAs/InP and (b) InAs/Si pTFETs with and without traps at the semiconductor interface. A uniform trap distribution was assumed in the band gap of InGaAs (or InAs) and the D_{it} was set to 2×10^{13} cm^{-2}eV^{-1}.

Conclusion

Large discrepancies between measured and simulated transfer characteristics of p-type InAs/Si NW TFETs can be attributed to the unknown work function, the dominance of electrically active traps, and possibly to a thin doping layer at the interface. Despite neglecting a number of effects, as DOS tails, band gap narrowing, channel quantization, and residual stress, calibrated TCAD can provide predictive trends for SS and on-current under variation of certain design parameters. This has been demonstrated for gate oxide and diameter scaling in InAs/Si and In$_{0.53}$Ga$_{0.47}$As/InP hetero NW TFETs. While gate oxide scaling improves the SS in In$_{0.53}$Ga$_{0.47}$As /InP TFETs because of the dominance of line tunneling, it has much less impact on the SS in InAs/Si TFETs where point tunneling determines the SS and where the BTBT rate has possibly already saturated in the considered thickness range. In General, the type-II band alignment at the InAs/Si interface makes point tunneling dominant, whereas the type-I band alignment at the In$_{0.53}$Ga$_{0.47}$As /InP favors line tunneling. Therefore, gate oxide scaling also results in a strong increase of the on-current of the In$_{0.53}$Ga$_{0.47}$As/InP TFETs. The on-current of the InAs/Si TFET remains more or less unaffected since the BTBT rate as function of oxide thickness is already in the regime of quasi-saturation. Gate oxide scaling is a more efficient method to improve the SS than diameter scaling. In the case of InAs/Si TFETs, diameter scaling hardly improves the SS, but reduces the on-current due to the loss of volume for the BTBT rate. At diameters less than ~40 nm, volume inversion takes place preventing line tunneling in the channel which leads to a sharp drop of the on-current. In the case of In$_{0.53}$Ga$_{0.47}$As/InP TFETs, both the SS and the on-current worsen because of

the increasing impact of volume inversion. Interface traps mainly affect point tunneling. Thus interface traps severely degrade the performance of InAs/Si TFETs but hardly ever that of $In_{0.53}Ga_{0.47}As$/InP TFETs.

Acknowledgments

References

1. A. M. Ionescu and H. Riel, Nature, **479**, 329 (2011).
2. A. S. Verhulst W. G. Vandenberghe, K. Maex, S. D. Gendt, M. M. Heyns, and G. Groeseneken, IEEE Electron Device Lett., **29**, 1398 (2008).
3. M. T. Björk, B. J. Ohlsson, T. Sass, A. I. Persson, C. Thelander, M. H. Magnusson, K. Deppert, L. R. Wallenberg, and L. Samuelson, Appl. Phys. Lett., **80**, 1058 (2002).
4. K. Tomioka, J. Motohisa, S. Hara, and T. Fukui, Nano Lett., **8**, 3475 (2008).
5. K. Tomioka, Y. Kobayashi, J. Motohisa, S. Hara, and T. Fukui, Nanotechnology, **20**, 145302 (2000).
6. K. Tomioka et al., Appl. Phys. Lett., **98**, 083114 (2011).
7. M. T. Björk, H. Schmid, C. D. Bessire, K. E. Moselund, H. Ghoneim, E. Lörtscher, and H. Riel, Appl. Phys. Lett., **97**, 163501 (2010).
8. K. E. Moselund, H. Schmid, C. Bessire, M. T. Björk, H. Ghoneim, and H. Riel, IEEE Electron Device Lett., **33**, 1453 (2012).
9. M. Borg, H. Schmid, K. E. Moselund, G. Signorello, L. Gignac, J. Bruley, C. Breslin, P. Das Kanungo, P. Werner, and H. Riel, Nano Letters, **14**(4), 1914 (2014).
10. D. Cutaia, K. E. Moselund, M. B. Borg, H. Schmid, L. M. Gignac, C. M. Breslin, S. Karg, E. Uccelli, and H. Riel, IEEE Journal of the Electron Devices Society, 2015, DOI 10.1109/JEDS.2015.2388793.
11. S. Mookerjea, D. Mohata, T. Mayer, V. Narayanan, and S. Datta, IEEE Electron Device Lett., **31**(6), 564 (2010).
12. H. Zhao, Y.-T. Chen, Y. Wang, F. Zhou, F. Xue, and J. C. Lee, Appl. Phys. Lett., **98**, 193501 (2011).
13. H. Zhu, J. Kuo, T. Kosel, M. Wistey, A. Seabaugh, and H. Xing, IEEE Electron Device Lett., **33**(6), 782 (2012).
14. A. Schenk, R. Rhyner, M. Luisier, and C. Bessire, Proc. 70th Device Research Conference (DRC), 201 (2012).
15. M. Luisier and G. Klimeck, IEEE Electron Device Lett., **30**, 602 (2009).
16. M. Luisier and G. Klimeck, J. Appl. Phys., **107,** 084507 (2010).
17. M. Luisier, A. Schenk, W. Fichtner, and G. Klimeck, Phys. Rev., **B 73**, 165319 (2006).
18. Sentaurus-Device User Guide, version 2014.09, Synopsys Inc., Mountain View, California (2014).
19. S. Sant and A. Schenk, IEEE Journal of the Electron Devices Society, 2015, DOI 10.1109/JEDS.2015. 2390971.

20. I. Vurgaftman, J. R. Meyer, and L. R. Ram-Mohan, J. Appl. Phys., **89**(11), 5815 (2001).

21. P. Philipe, P. Poulain, K. Kazmierski, and B. de Cremoux, J. Appl. Phys., **59**(5), 1771 (1986).

22. J. Waldrop, E. Kraut, C. Farley, and R. Grant, J. Appl. Phys., **69**(1), 372 (1991).

23. K. Uchida, H. Yamato, Y. Tomioka, A. Koizumi, and S. Nozaki, J. Crystal Growth **311**, 4011 (2009).

24. Wadehra, J. Nicklas, and J. Wilkins, Appl. Phys. Lett., **97**, 092119 (2010).

25. R. L. Anderson, IBM J. Res. Dev., **4**(3), 283 (1960).

26. P. Khomyakov, private communication

27. C. D. Bessire, *Semiconducting Nanowire Tunnel Devices - From All-Si Tunnel Diodes to III-V Heterostructure Tunnel FETs*, p. 66, Hartung-Gorre, Konstanz, (2014).

28. G. Paasch and H. Übensee, phys. stat. sol. (b), **118**(1), 255 (1983).

29. H. Ghoneim, P. Mensch, H. Schmid, C. D. Bessire, R. Rhyner, A. Schenk, Ch. Rettner, S. Karg, K. E. Moselund, H. Riel, and M. T. Björk, Nanotechnology, **23**, 505708, 2012, DOI 10.1088/0957-4484/23/50/505708.

30. H. Carrillo-Nunez, M. Luisier, and A. Schenk, Proc. 44th European Solid-State Device Research Conference (ESSDERC), 118 (2014).

31. A. Schenk, Solid-State Electronics, **35**(11), 1585 (1992).