Atomistic treatment of interface roughness in Si nanowire transistors with different channel orientations

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Nanowire transistors with a perfect crystal structure and a well-defined $Si-SiO_2$ interface cannot be grown with the actual technology. The shape of the semiconducting channel varies from source to drain. By self-consistently coupling the three-dimensional Schrödinger and Poisson equations, interface roughness (IR) effects are studied in Si triple-gate nanowire transistors with [100], [110], [111], and [112] oriented channels. The full-band electronic transport is computed in the nearest-neighbor $sp^3d^5s^*$ tight-binding model. IR is included by adding or removing atoms at the Si surface. A comparison of the different channel orientations is achieved by calculating the variations of the transistor threshold voltage. © *2007 American Institute of Physics*.
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Metal-oxide-semiconductor field-effect transistors could be replaced by nanowire transistors[1] in the future, if their promising performances are concretized. To explore the properties of these emerging devices, the recourse to quantum transport simulations becomes necessary. In this letter we investigate the full-band output characteristics of Si triple-gate nanowire transistors for different channel orientations such as [100], [110], [111], and [112]. The Schrödinger equation is solved in an atomic orbital basis using the $sp^3d^5s^*$ tight-binding method.[2] The semiempirical Si parameters are optimized to reproduce the complete bulk band structure and are assumed unchanged in nanostructures.[3] We compute the three-dimensional (3D) Poisson equation in the finite-element method (FEM) with charges localized around the atom positions.[4]

The SiO_2 oxide layers surrounding the Si channel are not subject to the transport calculation (only poor tight-binding representation is available) but are included to compute the 3D electrostatic potential from the Poisson equation. Consequently, the oxide grid points carry no charge, and hard wall boundary conditions are applied to the Si surface atoms. This means that the Si dangling bonds are passivated by increasing the on-site energies of the s and p orbitals.[5]

Interface roughness effects between the Si channel and the SiO_2 layers are expected to play an important role in nanowire transistors. They are generated by randomly distributing the atoms at the $Si-SiO_2$ interface according to an exponential autocovariance function $\Gamma_s(x)$,[6,7]

$$\Gamma_s(x) = \Delta_m^2 e^{-|x|/L_m}, \tag{1}$$

where Δ_m is the root mean square of the Si rough surface $s(\mathbf{r})$, x is the distance between two Si atoms at the $Si-SiO_2$ interface, and L_m is the correlation length of the roughness.

To construct $s(\mathbf{r})$, the positions $\mathbf{r}_i$ of the Si atoms at the nanowire surface are selected. Each nanowire face is treated separately. We assume that $s(\mathbf{r})$ is a stationary Gaussian process so that the specification of its autocorrelation function in Eq. (1) completely defines its probability density function (pdf).[8] If a nanowire face has N atoms, the pdf of its variations is given by

$$p(s(\mathbf{r}_1), \ldots, s(\mathbf{r}_N)) = \frac{1}{(2\pi)^{N/2}|\mathbf{C}|^{1/2}} \exp\left[-\frac{1}{2}\mathbf{S}^T\mathbf{C}^{-1}\mathbf{S}\right]. \tag{2}$$

The $N\times 1$ vector $\mathbf{S}=(s(\mathbf{r}_1), \ldots, s(\mathbf{r}_N))^T$ contains the variation of the surface at each atom position $\mathbf{r}_i$. The elements C_{ij} of the symmetric matrix $\mathbf{C}$ represent the correlation between $s(\mathbf{r}_i)$ and $s(\mathbf{r}_j)$,

$$C_{ij} = \langle s(\mathbf{r}_i)(s(\mathbf{r}_j)\ \rangle = \Delta_m^2 e^{-|\mathbf{r}_i-\mathbf{r}_j|/L_m}. \tag{3}$$

The variable $\mathbf{S}$ is randomly generated. Its elements $s(\mathbf{r}_i)$ are used to characterize the atomic surface at position $\mathbf{r}_i$. If $s(\mathbf{r}_i)$ is positive and larger than the distance between two atoms, atoms are added to the structure. In the case of a negative $s(\mathbf{r}_i)$, but with an absolute value larger than the distance between two atoms, atoms are removed from the structure. As an approximation, the surface atoms are not relaxed to minimize their energy.

The simulated transistor structure is presented in Fig. 1. It is composed of n-doped source and drain contacts ($N_D=10^{20}$ cm^{-3}, stoichiometric ratio $f=2\times10^{-3}$ of fully ionized donors) and a three-part gate (top, left, and right). The transistor is deposed on a buried oxide and is surrounded by three oxide layers ($t_{ox}=1$ nm). The x axis is the transport direction, and y and z are directions of confinement. A realization of the channel cross section is given in the lower part of the figure. Three different positions along x=[110] are shown. Points represent Si atoms, and lines model atomic bonds. The ideal Si cross section is a square of size 2.1×2.1 nm^2, delimited by the dashed lines. Such small dimensions are chosen because of computational limitations.[2] A potential V_g is applied to the gate (work function $\phi_m=4.25$ eV), $V_s=0$ V to the source, and $V_d=0.4$ V to the drain.

In this work the Si channels are oriented either with [100], [110], [111], or [112]. The root mean square of the Si rough surface $\Delta_m=0.14$ nm and the correlation length $L_m=0.7$ nm are assumed to be the same for all the surface types in order to make them comparable. Since all the nanowire slabs are different, a full 3D FEM mesh must be generated to calculate the electrostatic potential $V(\mathbf{r})$. The

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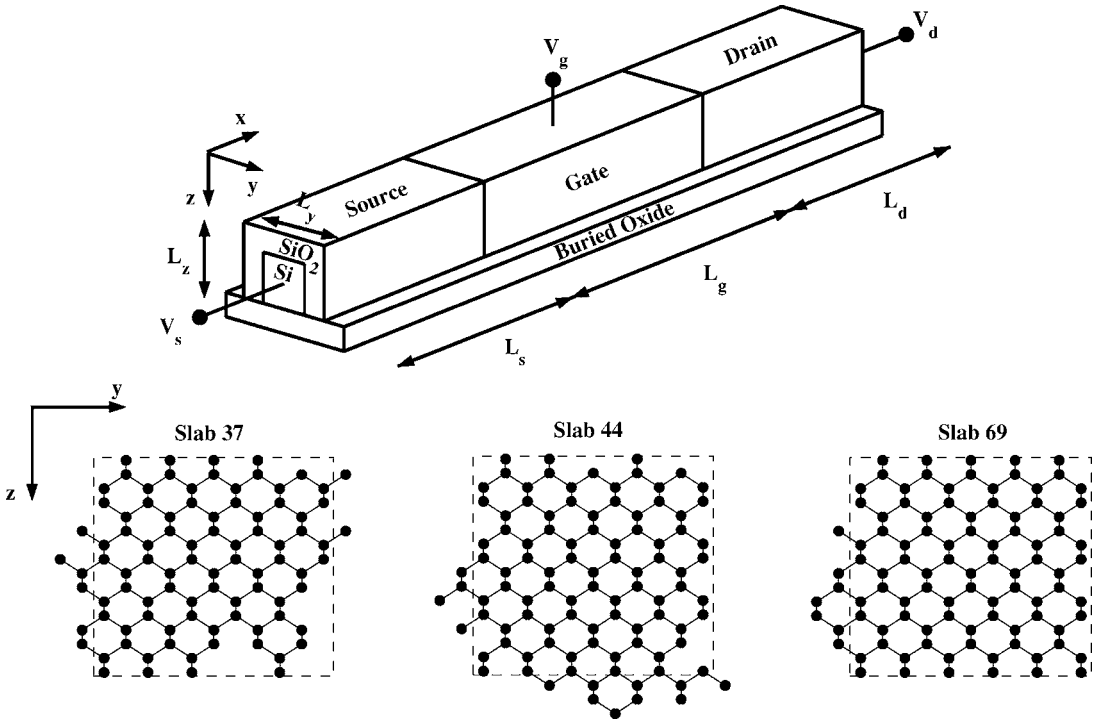

FIG. 1. Schematic view of a triple-gate nanowire transistor. The 2.1×2.1 nm^2 Si channel is surrounded by three oxide layers of thickness $t_{ox}=1$ nm and is deposed on a buried oxide. The source, the drain, and the gate have a length $L_s=L_d=9.7$ nm and $L_g=13$ nm, respectively. In transport direction x, the wire is composed of 60 slabs (wire unit cell) for $x=[100]$, 88 slabs for $x=[110]$, 34 slabs for $x=[111]$, and 49 slabs for $x=[112]$. A slab contains a different number of atomic layers for each crystal orientation. The lower part of the figure shows the projection into a single plane of three different slabs with interface roughness in the $x=[110]$ configuration. The dashed lines delimit the ideal 2.1×2.1 nm^2 channel.

mesh elements are finer around the atoms than in the oxide layers, where $V(\mathbf{r})$ varies linearly due to the absence of charge [the second derivative of $V(\mathbf{r})$ vanishes].

In Fig. 2, the full-band I_d-V_{gs} ($V_{ds}=0.4$ V) transfer characteristics of a [100] (solid line with circles and dotted line) and a [110] (solid and dashed lines) structure with interface roughness are compared to the results of ideal structures. For the simulated realizations of the random $Si-SiO_2$ interface, the [100] drain current I_d at $V_{gs}=0.4$ V is reduced to about 30% of its ideal value, and the [110] drain current at $V_{gs}=0.4$ to 65% of the ideal I_d. The drain current in the subthreshold region is seriously deteriorated by the variation of the nanowire cross section; the threshold voltage V_{th} increases, but the swing S remains close to $S=60$ mV/decade.

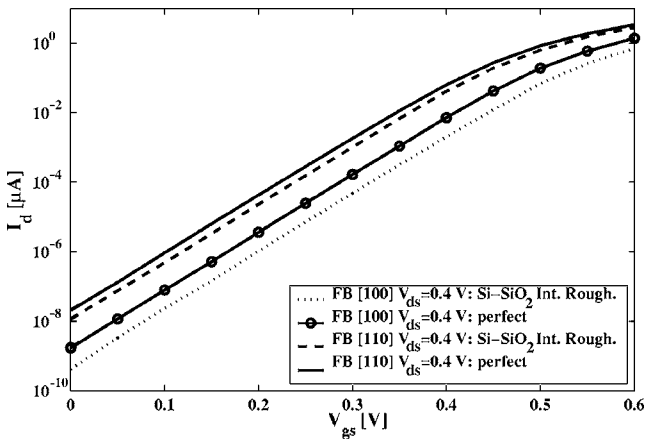

FIG. 2. Full-band transfer characteristics I_d-V_{gs} at $V_{ds}=0.4$ V for perfect [100] and [110] nanowires (solid lines) and for [100] and [110] nanowires with $Si-SiO_2$ interface roughness (dashed and dotted lines).

However, another random distribution of the interface atoms leads to a different transfer characteristics I_d-V_{gs}. Since the subthreshold swing S is not much affected by the interface roughness, we can calculate several I_d samples at a fixed V_{gs} and extrapolate from the results the variations of the threshold voltage V_{th}. For each channel orientation, 105 different $Si-SiO_2$ interface realizations are simulated, their mean drain current I_{dm} at $V_{gs}=V_{ds}=0.4$ V is

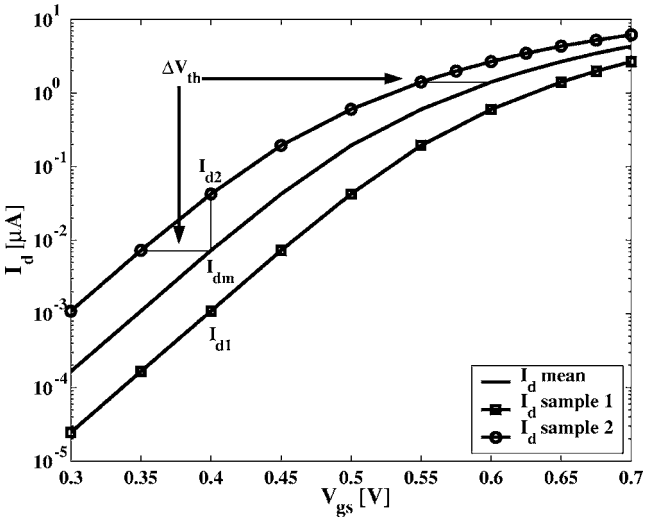

FIG. 3. Illustration of the calculation method for ΔV_{th}, the variation of the threshold voltage, in nanowires with different realizations of interface roughness. The line without symbols represents the mean drain current I_{dm} averaged over the 105 calculated samples. The lines with symbols are two possible currents I_{d1} and I_{d2} corresponding to two different roughness realizations. Only the current values at $V_{gs}=0.4$ V, for example, are needed to obtain ΔV_{th}.

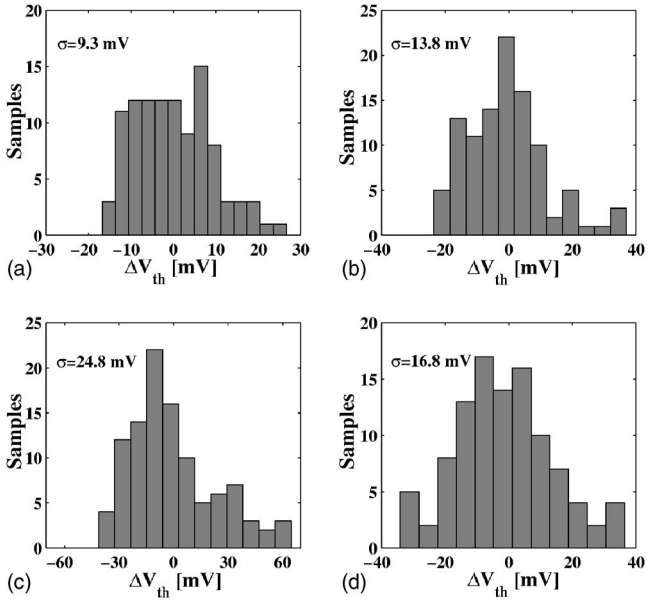

FIG. 4. Histogram distribution of the 105 samples representing the variation of the threshold voltage ΔV_{th} caused by interface roughness. The results for (a) the [110], (b) the [100], (c) the [111], and (d) the [112] Si nanowire transistors are plotted. σ is the standard deviation of ΔV_{th}.

calculated, and the variation of V_{th} is obtained for each sample I_{d} as

$$\Delta V_{\text{th}} = S \log_{10}(I_{\text{dm}}/I_{\text{d}}). \tag{4}$$

This principle is explained in Fig. 3. The histogram distributions of ΔV_{th} are shown in Fig. 4 for (a) the [110], (b) the [100], (c) the [111], and (d) the [112] nanowires. The standard deviation σ of ΔV_{th} is also given for each channel configuration.

To design a circuit, all the involved transistors should have the same characteristics, although they have slightly different structures. Hence the standard deviation of ΔV_{th} should be as small as possible. The lowest value of σ is obtained for a channel oriented along the [110] crystal axis (σ=9.8 mV). [100] follows with σ=13.8 mV, then [112] (σ=16.8 mV), and finally [111] (σ=24.8 mV). For such nanowire transistors, [110] is the best channel orientation, because it has the highest on current[4,9] and it is the least sensitive to structure variations.

In conclusion we simulated the full-band characteristics of Si nanowire transistors with interface roughness effects for different channel orientations. We found that [110] is the best transport direction regarding on current and process variations, but other effects such as the influence of the gate length, drain induced barrier lowering, and gate leakage are still under investigation.

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