Performance Projection of III-V Ultra-Thin-Body, FinFET, and Nanowire MOSFETs for two Next-Generation Technology Nodes

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***Abstract*— Using state-of-the-art simulation tools ranging from semi-classical Monte-Carlo to full-quantum atomistic approaches, the competitiveness of III-V compounds for next-generation high-performance logic switches is confirmed. A planar double-gate ultra-thin-body (DG-UTB), a triple-gate FinFET, and a gate-all-around nanowire (NW) transistor have been designed according to the ITRS specifications for two technology nodes with physical gate lengths of L_G=15 nm and 10.4 nm. A thorough performance comparison of digital and analog figures of merit at these nodes reveals that for L_G=15 nm, the performance of planar and 3-D architectures is comparable. At L_G=10.4 nm, the III-V NW promises the highest performance, especially when lowering the supply voltage from 0.59 V to 0.50 V. It also significantly outperforms its strained silicon counterpart. Finally, the effects of series resistance combined with interface traps, surface roughness, alloy scattering, and electron-phonon interactions have been found to deteriorate the III-V ballistic ON-current by 50-60%.**

I. Introduction

Due to their high electron mobility and injection velocity, III-V compounds based FETs rank among the most promising replacements for *n*-type strained Si MOSFETs at future technology nodes with shorter gate lengths than currently manufactured (20-25 nm) [1]. At ultra-scaled gate lengths, however, the very low effective masses of III-V's give rise to strong source-to-drain (S-to-D) tunneling leakage that might strongly deteriorate the sub-threshold swing and compromise possible advantages over strained Si.

This work presents a comprehensive computational study of planar and 3-D architectures to assess whether III-V MOSFETs can compete with strained silicon at not yet fabricated channel lengths. More specifically, the performance and scalability of the $In_{0.53}Ga_{0.47}As$ double-gate ultra-thin-body (DG UTB), triple-gate FinFET, and gate-all-around nanowire (GAA NW) field-effect transistors (FETs) depicted in Fig. 1 are evaluated in terms of digital and analog figures of merit at two future technology nodes labeled "A" and "B" and characterized by L_G = 15 nm at V_{DD} = 0.63V and L_G = 10.4 nm at V_{DD} =0.59V/0.50V, respectively. Their channel lengths, equivalent oxide thicknesses (EOT), and supply voltages follow the ITRS prescriptions, as summarized in Tables 1-2.

Studies predicting the performance of future III-V devices have been reported before [2][3], but this is the first time that three transistor types are compared to each other at two consecutive technology nodes, and where the influence of a wide set of non-ideal effects is carefully investigated.

At first, ballistic quantum transport simulations have been performed to extract the upper limit of the most relevant digital (ON-current, SS, DIBL, switching time, switching energy) and analog (cut-off frequency, intrinsic gain) figures of merit. Comparisons with strained silicon devices including electron-phonon interactions are provided for the NW case. The lateral dimensions have been chosen such that the sub-threshold swing of all devices lies in the vicinity of 70 mV/dec and the DIBL does not exceed 100 mV/V. Then, a multi-sub-band Monte-Carlo (MSMC) approach considering the effect of interface traps, scattering (surface roughness, alloy, and electron-phonon), and series resistance has been used to determine the ON-current losses of the DG-UTB as compared to the ideal structure operating in the ballistic limit. The physics-based models used in this analysis have been calibrated with experimental data of interface trap profiles and effective mobility.

II. Simulation Approaches

Ballistic simulations have been performed with a state-of-the-art NEGF quantum transport tool relying on either the effective mass approximation (EMA) [4] or the empirical nearest-neighbor tight-binding (TB) method [5]. In both schemes, source-to-drain tunneling is accurately captured. The planar structure has been simulated in the $sp^3d^5s^*$ TB formalism without spin-orbit coupling, with the parameters from Ref. [6]. Due to the heavy computational burden associated with 3-D structures, the EMA and mode-space decomposition have been used to simulate the FinFET and GAA NW. Their effective masses have been calibrated using full-band data and the strong non-parabolicity of $In_{0.53}Ga_{0.47}As$ has been taken into account [7], as shown in Fig. 2. The simulations of the strained silicon GAA NW with transport along <110> have been performed using the same EMA tool as before, but with electron-phonon scattering and the bulk phonon parameters of Ref. [8].

The MSMC simulator from Ref. [9] has been employed to extend the ballistic results of III-V compounds. It considers non-parabolic bands and includes the combined effects of electron-phonon interactions, alloy scattering, surface

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roughness, and interface traps. The trap [10] and the non-linear surface roughness [11] models have been calibrated by comparison with experimental interface trap profiles [12] and mobility data [13]. The effect of contact series resistance has been included directly in the self-consistent loop.

III. Results

The normalization methods for the current are detailed in Fig. 1. The OFF-currents have been set to 100 nA/µm in all cases. The I_D-V_{GS} characteristics reported in Fig. 3 indicate that the ON-current values of all devices at all nodes are relatively homogeneous at around 1.6 mA/µm (1.0 mA/µm at V_{DD} = 0.5 V). Tables 3-4 define and summarize the key figures of merit for digital and analog applications. At L_G = 15 nm (node A), all architectures are characterized by a similar performance level, although the GAA NW shows an at least two times higher intrinsic gain compared to the FinFET and DG-UTB. The advantage of the GAA NW over the other architectures manifests itself at L_G = 10.4 nm, particularly in terms of analog figures of merit, where a strong transconductance g_m leads to an almost two times higher cutoff frequency than in other devices. The GAA NW superiority becomes even more apparent at lower supply voltages, e.g. V_{DD} = 0.50 V (Table 3), where its switching energy reaches the lowest value by at least a factor of two and its cutoff frequency appears less sensitive to the V_{DD} decrease. The GAA is also the only device that significantly benefits from the dimension scaling between nodes A and B (19% faster T_{SW}, 27% lower E_{SW} and around 70% higher f_T). Further gate length reductions below 10.4 nm might therefore be realistic. Nevertheless, note that none of the ON-currents and switching times satisfy the ITRS requirements at L_G = 15 nm (I_{ON} = 2.2 mA/µm and T_{SW} = 0.13 ps).

The *I-V* characteristics in Fig. 3 have been supplemented by full-quantum simulations of strained Si GAA NW FETs with transport along the <110> crystal axis, the same dimensions as their III-V counterparts, but larger source and drain doping ($N_D = 10^{20}$ cm^{-3}), and including electron-phonon scattering. This effect plays a much more important role in Si than in III-V, as will be confirmed by the MSMC simulations hereafter. A ballisticity of 56 and 69% at L_G = 15 and 10.4 nm has been obtained, respectively.

The $In_{0.53}Ga_{0.47}As$ channels deliver higher ON-currents than strained Si at similar sub-threshold swings. To provide a quantitative comparison between the Si and III-V devices, their respective figures of merit for node B have been computed at V_{DD} = 0.5 V, a relevant supply voltage to benchmark new technologies (Table 3). The III-V device dominates, as it exhibits a more than two times smaller switching time, three times lower switching energy, thrice the cutoff frequency, and nearly twice the intrinsic gain of its Si counterpart. These very promising results highlight the clear advantages of III-V compounds at these very advanced nodes, where they sustain slightly higher currents than strained Si at much lower inversion charges.

To refine this study, the influence of electron-phonon scattering and non-ideal effects have been assessed using a MSMC approach to reduce the computational burden. In the III-V DG-UTB FET with L_G=15 nm, electron-phonon and alloy scattering reduce the ON-current by less than 10% with respect to the ballistic case (Fig. 4(c)). This justifies the previous comparison between ballistic III-V and strained Si with electron-phonon scattering. Adding the effect of surface roughness and traps significantly reduces the ON-current by an additional 35%. Finally, the series resistance (ITRS value of R_{SD} = 131 Ω•µm) further lowers I_{ON} by 30%. The total performance loss due to non-ideal effects is estimated to be roughly 60%. Applying this correction to the ballistic quantum simulations of the DG-UTB at node B (V_{DD} = 0.5 V) yields $I_{ON} \approx$ 0.45 mA/µm. This value is in the same range as similar experimental devices with longer channels [14], but well below the ITRS requirements (factor 4 to 5).

IV. Conclusions

In this work, three $In_{0.53}Ga_{0.47}As$-based device architectures have been investigated for potential application as next-generation high-performance logic switches at not yet manufactured nodes with L_G = 10.4 nm and L_G = 15 nm. Using full-quantum ballistic simulations, it has been demonstrated that for L_G = 15 nm, planar and 3-D architectures provide similar levels of performance. At L_G = 10.4 nm, however, the GAA NW emerges as the most promising device type, especially at low supply voltages. A detailed comparison with equivalent strained Si transistors at L_G = 10.4 nm has shown the significantly superior digital and analog capabilities of III-V. Although none of the ITRS target f.o.m could be reached (possibly too optimistic), further scaling below L_G = 10.4 nm can be expected from the GAA NW architecture only.

Additionally, semi-classical MSMC simulations carefully calibrated on experimental data made it possible to predict ON-current losses of around 50-60% after taking into account the combined effects of interface traps, various scattering mechanisms, and series resistances. The advent of the III-V technology will probably depend on rapid progresses towards low contact resistances and clean semiconductor-oxide interfaces with small trap densities and reduced roughness.

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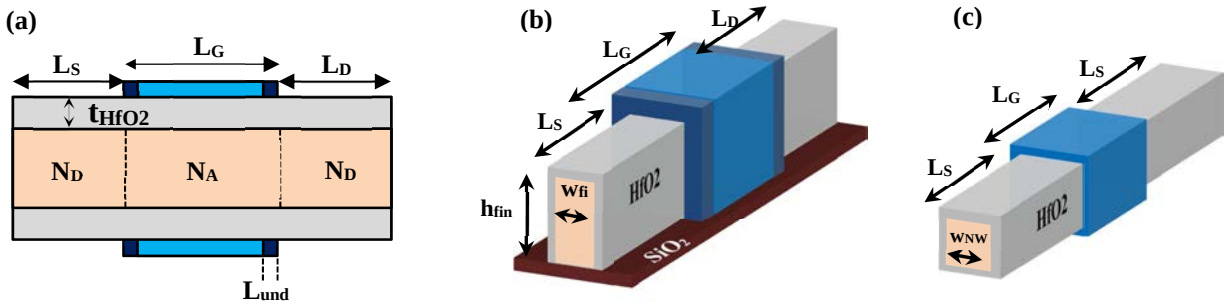

Figure 1: Schematic view of the **(a)** DG-UTB, **(b)** Tri-Gate FinFET, and **(c)** GAA NW architectures considered in this work. An $In_{0.53}Ga_{0.47}As$ channel has been chosen since it represents a good compromise between low transport effective masses and minimal band-to-band tunneling leakage. A gate underlap of 2 nm has been introduced in the DG-UTB and FinFET architectures to keep SS≈70 mV/dec, DIBL<100 mV/V and realistic lateral dimensions (see Table 2). The currents in the FinFET and GAA NW structures have been normalized by $2h_{fin}+w_{fin}$ and $4w_{NW}$, respectively. To ensure a meaningful comparison between 2-D and 3-D architectures, a normalization factor of 2 has been applied to the DG-UTB device.

L_S/L_D S/D length [nm]	**N_D** S/D donor conc. [cm^{-3}]	**N_A** Chann. doping [cm^{-3}]	**I_{OFF}** [nA/μm]
25	$5x10^{19}$	10^{17}	100

Table 1: Relevant design parameters common to all nodes and architectures (source and drain extensions, doping concentrations, and OFF-current).

Node	**L_G** [nm]	**V_{DD}** [V]	**EOT** **t_{HfO2}** [nm]	**t_B** DG-UTB body thickness [nm]	**w_{fin}xh_{fin}** FinFET cross sect. [nm^2]	**w_{NW}** GAA cross sect. [nm^2]
A	15	0.63	0.68 3.84	7	7 x 26	7 x 7
B	10.4	0.59 0.5	0.59 3.3	4	4 x 14	4 x 4

Table 2: Relevant design parameters in relation to the nodes A and B. While the gate lengths (L_G), equivalent oxide thicknesses (EOT), and supply voltages (V_{DD}) have been taken from ITRS, the lateral dimensions have been adjusted using full-quantum simulations to yield the desired SS and DIBL values.

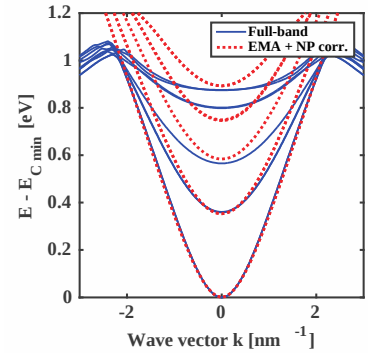

Figure 2: Lowest conduction sub-bands of the 4x4 nm^2 GAA NW architecture (Node B) as obtained by $sp^3d^5s^*$ tight-binding simulations (blue) and EMA with non-parabolicity correction (red dots).

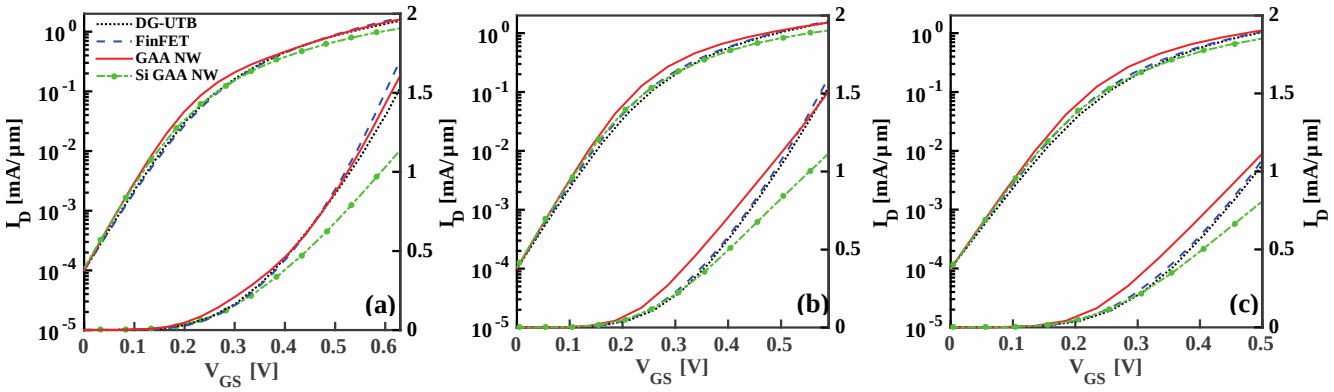

Figure 3: Full-quantum I_D-V_{GS} characteristics at $V_{DS} = V_{DD}$ (ballistic for III-V and with electron-phonon scattering for Si) for **(a)** node A **(b)** node B at V_{DD} = 0.59V and **(c)** node B at V_{DD} = 0.5V for the III-V DG-UTB (*dotted black*), III-V FinFET (*dashed blue*), III-V GAA NW (*dash-dotted red*), and strained Si GAA NW (*green*).

Read entries as Node A / Node B	**SS** [mV/dec]	**DIBL** [mV/V]	**I_{ON}** [mA/μm]	**T_{SW}** [ps]	**E_{SW}** [fJ/μm]	**g_m** [S/cm]	**g_{ds}** [S/cm]	**C_{tot}** [pF/cm]	**f_T** [GHz]	**A_V**
DG-UTB	74 72	73 58	1.53 1.54	0.16 0.19	0.15 0.165	22.85 21.3	1.67 1.3	4 3.55	906 952	14 16
FinFET	75 69	84 50	1.7 1.6	0.19 0.23	0.21 0.22	20.48 25.46	1.72 1.18	3.33 4.24	979 956	12 22
GAA NW	66 65	38 32	1.61 1.51	**0.22** **0.18**	**0.22** **0.16**	**21.57** **33.93**	0.77 1.07	3.5 3.2	**976** **1691**	**28** **32**

Table 3: Key digital and analog figures of merit of all III-V architectures (full-quantum ballistic simulations) at nodes A and B (read entries as $\frac{\text{Node A}}{\text{Node B}}$). I_{ON} is defined as the drain current at $V_{GS} = V_{DS} = V_{DD}$, the switching time T_{SW} as $\frac{Q_{ON}-Q_{OFF}}{I_{ON}}$, where Q_{ON} and Q_{OFF} are the total charge in the device at $V_{GS} = V_{DD}$ & $V_{DS} = 0$ V and $V_{GS} = 0$ V & $V_{DS} = V_{DD}$, respectively, and the switching energy E_{SW} as $V_{DD}(Q_{ON} - Q_{OFF})$. The transconductance g_m, the output conductance g_{ds}, and the total gate capacitance C_{tot} are extracted at $V_{GS} = V_{DS} = \frac{V_{DD}}{2}$ to give an estimate of the cutoff frequency f_T calculated as $\frac{g_m}{2\pi C_{tot}}$ and the intrinsic gain A_V defined as $\frac{g_m}{g_{ds}}$.

Read entries as node B $V_{DD} = 0.59V$ / $V_{DD} = 0.5V$	**SS** [mV/dec]	**DIBL** [mV/V]	**I_{ON}** [mA/μm]	**T_{SW}** [ps]	**E_{SW}** [fJ/μm]	**g_m** [S/cm]	**g_{ds}** [S/cm]	**C_{tot}** [pF/cm]	**f_T** [GHz]	**A_V**
DG-UTB	72 72	58 62	1.54 1.04	0.19 0.23	0.17 0.12	21.3 11.8	1.3 0.96	3.6 3.7	952 510	16 14
FinFET	69 69	50 53	1.6 1.07	0.22 0.29	0.22 0.16	25.46 17.19	1.18 0.86	4.24 4.0	956 682	22 20
GAA NW	65 65	32 33	1.51 **1.11**	0.18 **0.2**	0.16 **0.06**	33.93 25.44	1.07 0.86	3.2 3.1	1691 **1307**	32 **30**
Strained-Si GAA NW	- 64	- 42	- **0.81**	- **0.45**	- **0.18**	- 14.9	- 0.85	- 5.3	- **450**	- **17**

Table 4: Key digital and analog figures of merit of all III-V architectures (full-quantum simulations) and of the strained silicon GAA (full-quantum simulations with electron-phonon scattering) at node B at V_{DD} = 0.59 V and node B at V_{DD} = 0.5 V (read entries as node B $\frac{V_{DD}=0.59V}{V_{DD}=0.5V}$). The same extraction methods as in Table 2 have been used. The most relevant results have been highlighted in bold.

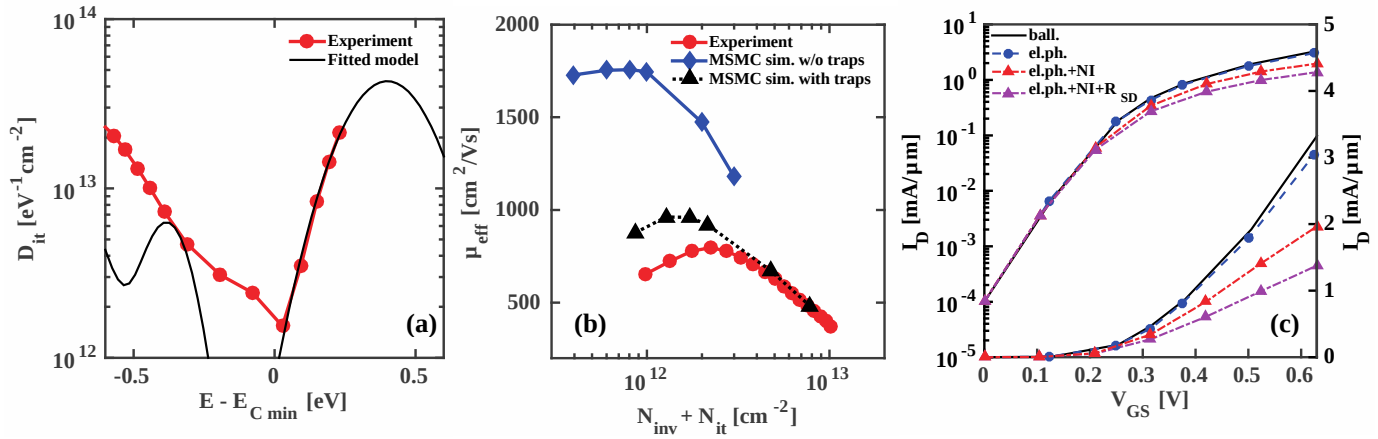

Figure 4: **(a)** Interface trap density (D_{it}) with respect to the energy difference to the bulk conduction band edge E_{Cmin}. Experimental data of Ref. [12] *(red)* has been used to calibrate the MSMC interface trap model (*black*). **(b)** Effective mobility with respect to $N_{inv} + N_{it}$, where N_{inv} is the inversion charge density and N_{it} the trapped charge density. Experimental data from Ref. [13] (*red*), MSMC simulations in the presence of electron-phonon interactions, alloy + Coulomb scattering, and surface roughness (*blue*), adding interface traps (*black*) **(c)** MSMC I_D-V_{GS} characteristics at V_{DD} = 0.63V for node A for the DG-UTB architecture with the same interface trap profile as in sub-plot (a): ballistic simulations *(black)*, with electron-phonon interactions and alloy scattering *(dashed blue)*, adding Coulomb scattering and surface roughness (non-ideal effects, i.e. NI) (*triangle red*), and adding the effect of series resistance R_{SD} = 131Ω•μm *(triangle magenta)*.