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Trap-Assisted Tunneling in Si-InAs Nanowire Heterojunction Tunnel Diodes

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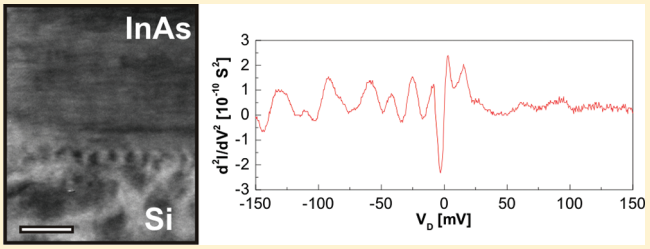
Supporting Information

ABSTRACT: We report on the electrical characterization of one-sided p^+-si/n-InAs nanowire heterojunction tunnel diodes to provide insight into the tunnel process occurring in this highly lattice mismatched material system. The lattice mismatch gives rise to dislocations at the interface as confirmed by electron microscopy. Despite this, a negative differential resistance with peak-to-valley current ratios of up to 2.4 at room temperature and with large current densities is observed, attesting to the very abrupt and high-quality interface. The presence of dislocations and other defects that increase the excess current is evident in the first and second derivative of the $I-V$ characteristics as distinct peaks arising from trap-and phonon-assisted tunneling via the corresponding defect levels. We observe this assisted tunneling mainly in the forward direction and at low reverse bias but not at higher reverse biases because the band-to-band generation rates are peaked in the InAs, which is also confirmed by modeling. This indicates that most of the peaks are due to dislocations and defects in the immediate vicinity of the interface. Finally, we also demonstrate that these devices are very sensitive to electrical stress, in particular at room temperature, because of the extremely high electrical fields obtained at the abrupt junction even at low bias. The electrical stress induces additional defect levels in the band gap, which reduce the peak-to-valley current ratios.



KEYWORDS: Nanowire, tunneling, diode, heterojunction, dislocations, traps

In 1958, Esaki measured the current of degenerately doped Ge diodes[1] and showed that charge transport at small biases is completely governed by the laws of quantum tunneling through the space charge region of the junction. In recent years, this interband tunneling in highly doped pn-junctions has attracted particular interest for low-power logic devices. By designing a transistor based on a gated *p-i-n* structure, it is theoretically possible to reach inverse subthreshold slopes below the thermal limit (60 mV/dec) at room temperature, which is encountered in conventional metal-oxide semiconductor field-effect transistors (MOSFETs). This would enable further supply voltage scaling[2] to reduce the surging power dissipation in logic circuits. However, a major drawback in these so-called tunnel field-effect transistors (TFETs) is the lack of high drive currents reported for homojunction transistors.[3] By taking advantage of band alignments in heterojunction transistors, this figure of merit can be drastically improved, as predicted theoretically.[4] Using semiconductor nanowires, a large freedom in combining different materials exists because of the efficient strain relaxation in reduced dimensions.[5] On the other hand, if the lattice mismatch is very high, these heterointerfaces could still suffer from defect formation such as dislocations. It is therefore important to understand how such defects affect the tunneling process in lattice mismatched heterojunctions.

In this Letter, we report on the electrical and structural characterization of Si-InAs nanowire heterojunction Esaki diodes, a new material combination not available in bulk systems because of the very high lattice mismatch (11.6%). It is shown that the low-temperature conductance has distinct features that are attributed to dislocations and other defects at the heterointerface. The number of such defects that mainly contribute to the excess current leads to a strong variation in the peak-to-valley current ratio (PVCR). Therefore device-to-device spread in excess currents indicates varying defect concentrations at the heterointerface. Furthermore, electrical stressing of the junction is demonstrated to induce more defects, which is readily observable in the diode conductance. In addition, our experiments provide further insight into the spatial occurrence of the tunnel generation rates in these Si-InAs heterojunction devices and their importance for the device characteristics.

The Si-InAs heterojunction Esaki diodes were fabricated by growing InAs nanowires using metal—organic chemical vapor deposition selectively in patterned silicon oxide openings on ⟨111⟩ p-type silicon substrates.[6] In all devices, the Si substrate boron doping was 1×10^{20} cm^{-3} and the n-type InAs was

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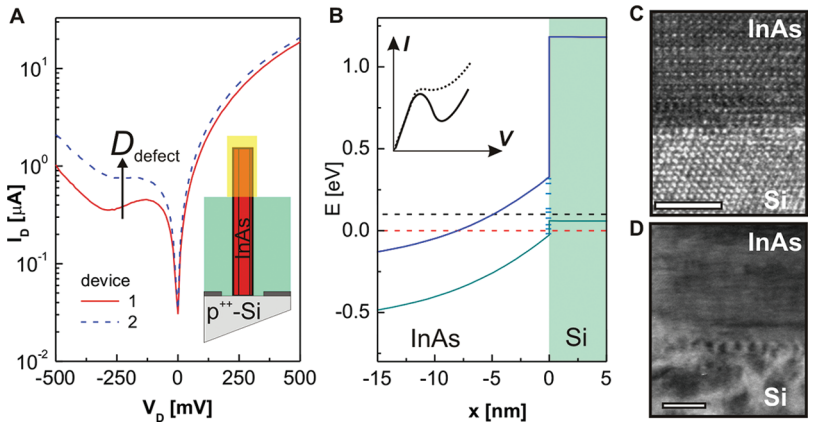

Figure 1. Defects in tunnel diodes. (A) $I-V$ characteristics of two Si-InAs heterojunction tunnel diodes. The spread in current in forward bias arises from different levels of excess current due to different interface defect state densities. The inset shows the schematic cross section of a Si-InAs diode. (B) Calculated band structure of the Si-InAs heterostructure under 100 mV forward bias. The quasi electron/hole Fermi level is represented by the black/red dashed line, respectively. At the interface, trap states are indicated that allow charge transport even when direct tunneling is prohibited, leading to an increased excess current as shown in the upper inset by the dashed line as compared to the solid line without defect states. (C) High-resolution transmission electron micrograph of the Si-InAs interface. Scale bar is 5 nm. (D) Tilted view of the interface seen in (C), showing the periodic strain contrast from the dislocation network at the interface formed because of the high lattice mismatch. Scale bar is 10 nm.

nonintentionally doped and had a resistivity of 20 mΩcm. All wires were 140 nm in diameter and had a length of 700 nm. After growth, an insulating benzocyclobutene (BCB) layer was spin-coated on the wafer and then back-etched using SF_6/O_2 reactive ion etching to reveal the top part of the wires. Subsequently UV lithography and Ti/Al metal deposition were performed to fabricate top contacts, thereby completing the individual wire devices (see inset of Figure 1A). The devices were finally wired and mounted on a chip carrier for low-temperature measurements.

The electrical characterization was performed at 4.2 K using standard DC measurements for the current−voltage ($I-V$) characteristics and lock-in techniques to measure the first and second derivative of the $I-V$ characteristics directly. In all measurements shown here, the p-Si substrate was grounded and the n-InAs (top contact) were biased, and therefore a negative bias implies a forward-biased junction.

In Figure 1A, the $I-V$ characteristics of two different tunnel diodes are shown, both having almost identical tunnel currents in reverse bias. In forward direction, an NDR region is typically observed (with PVCR of up to 2.4 as shown in the Supporting Information) after the initial low bias region, where direct tunneling predominates. The PVCR is limited by the magnitude of the excess current, which is the predominant current in this region and depends linearly on the density of defect states in the bandgap.[7] As can be seen in Figure 1A, there is a rather large spread in excess currents and thus in PVCR between the two devices, suggesting that the number of defects varies substantially. The InAs-Si band diagram in Figure 1B shows the band bending under a forward bias of 100 mV. In a device with few defects, fewer carriers are able to tunnel through the gap because less empty states are available and thus the excess current is low (see solid line in the inset of Figure 1B). However, for a larger defect density, more carriers may tunnel from the InAs region by coupling to localized phonon modes into a trap (defect) state[8] in the bandgap. By another multiphonon process, carriers then relax into the valence band, giving rise to an increased excess current and a reduced PVCR (corresponding to the dotted trace in the inset). This suggests that device 2 of Figure 1A has a higher defect density (D_{defect}) than device 1 does. A structural analysis using transmission electron microscopy (TEM) of the InAs-Si heterojunction (shown in Figure 1C) demonstrates that the materials are crystalline with a seemingly abrupt interface. The large lattice mismatch of 11.6% is known to force dislocation formation,[9] and by tilting the sample slightly off-axis, a typical periodic strain pattern with a 36 Å periodicity can indeed be observed at the heterointerface (Figure 1D). Dislocations are known to form acceptor states in the bandgap of semiconductors[10,11] and are most likely the main contributors, besides point defects, to the trap-assisted tunneling observed in our devices.

To study the excess currents and defect states in more detail, low-temperature measurements at 4.2 K were performed. Figure 2A shows the $I-V$ characteristics of device 1 at room temperature and at 4.2 K (data for more devices can be found in Supporting Information). In reverse direction, the current is decreased at lower temperatures, which is mainly due to a series resistance. In forward direction, it can be seen that direct tunneling is almost unchanged, but the PVCR is increased because of the temperature dependence of the excess currents as expected from theory.[7,12]

In the second derivative (Figure 2B), measured at low temperature, pronounced peaks emerge at distinct voltages. Such peaks were reported in Si and Ge tunnel diodes[7,12] and were attributed to different but pure phonon contributions in the tunneling process. Phonon peaks generally show up at the same voltages (for a specific material) and are symmetric for positive and negative bias voltages. In our devices, the peaks appear at different voltages in different devices and are never symmetric in bias. We therefore exclude single-phonon-assisted tunneling (as observed in indirect band gap homojunction tunnel diodes[7,12]) in the InAs-Si system. In addition, single-phonon-assisted tunneling is not expected because of the "direct" bandgap of this system, with both the Si valence band and the InAs conduction band being located at the Γ-point. However, phonon-assisted tunneling via trap states in the bandgap like those arising from dislocations gives rise to peaks in the second derivative at voltages corresponding to energy levels of the traps. Interestingly, the peaks observed in the second derivative (Figure 2B) are much more pronounced in both intensity and

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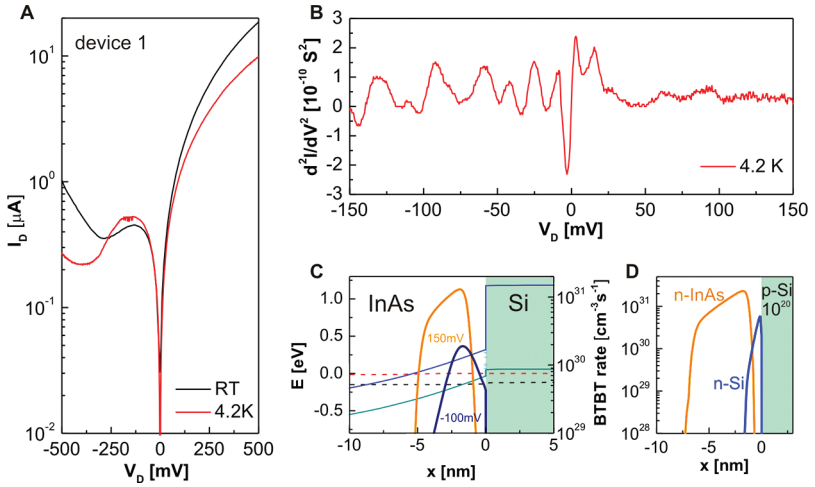

Figure 2. Trap-assisted tunneling in InAs-Si heterojunction tunnel diodes. (A) Comparison of $I-V$ characteristics of a Si-InAs tunnel diode at room temperature and 4.2 K. (B) The second derivative of current with respect to the voltage at 4.2 K exhibits pronounced peaks in forward bias originating from trap-assisted tunneling due to defect states in the bandgap. In reverse bias, the peaks are less distinct and only occur at low voltages. At higher voltages, the tunnel generation rate is pushed into InAs away from the interface, where the defect density is the highest. (C) Calculated band diagram (at 300 K) of the Si-InAs junction at 150 mV reverse bias. The electron quasi-Fermi level (black dashed line) indicates that valence band states in the InAs become available for the tunnel process. Thus the BTBT rate shifts away from the interface, into the InAs nanowire. The orange curve illustrates the shift of the generation rate into the InAs in reverse bias. It is also seen here that at this bias no more trap states are available for transport and consequently no structure (relating to interface defects) should be observed in the first and second derivative, which is in agreement with the experimental observations. The blue curve corresponds to the generation rate profile for 100 mV forward bias. Here it is seen that there still is a finite tunnel rate right at the interface. (D) Comparison of the calculated BTBT rates (at 300 K) for the Si-InAs tunnel heterostructure diode as used in the experiments with an all Si homojunction diode at a reverse bias of 300 mV; whereas the n-type doping in Si is 6×10^{19} cm^{-3} and in InAs 3×10^{18} cm^{-3}. The highly doped all-Si diode has a peaked BTBT rate at the interface because of the similar doping concentrations on both sides.

number in forward direction and are completely absent for reverse biases higher than ∼100 mV. This can be explained using the band diagrams of Figures 1B and 2C showing the InAs-Si heterojunction under forward and reverse bias conditions. In forward bias (Figure 1B), charge carriers tunnel from the conduction band in InAs into the valence band of Si. This process happens spatially at the interface of the two semiconductor materials. In addition, as soon as a trap state arises in the energy window between the two quasi Fermi levels, charge carriers can also tunnel into and out of this trap either via a two-step process or a phonon-assisted bound state-to-band transition.[8] Around 100 mV forward bias, where the energetic window for direct tunneling disappears, only tunneling via trap states remains and increases the excess current as discussed above. In contrast, under reverse bias conditions higher than 50−100 mV (Figure 2C), there are no more defect states left in the vicinity of the interface (related to dislocations) to tunnel via, and no more peaks in $\delta^2I/\delta V^2$ are observed. In addition, electron states become available even in the InAs valence band, and the tunnel generation probability increases in the InAs part of the junction. This leads to a spatial shift of the generation of charge carriers away from the metallurgical junction into the InAs as shown in Figure 2D for forward (blue) and reverse (orange) bias, respectively. This "one-sided" tunneling effectively suppresses the trap-assisted tunneling via the interface-induced bandgap states. The band-to-band generation rates are calculated using a band-to-band tunneling (BTBT) model implemented for InAs[13,14] and are peaked inside the InAs[15] for all biases, both forward and reverse and is due to the one-sided heterojunctions used. This supports the use of only InAs in the tunnel model. In case of higher doping in InAs, the generation rates would shift toward the heterointerface and a new BTBT model would have to be implemented that takes into account both materials. In Figure 2D, a comparison of the BTBT rates for an all-Si diode and the InAs-Si heterostructure diode was modeled for a reverse bias of 300 mV. The *n*-type doping concentration in these different types of pn-junctions is 6×10^{19} cm^{-3} in Si and 3×10^{18} cm^{-3} in InAs, respectively, with equal substrate doping type and level of 1×10^{20} cm^{-3}. In contrast to the hetero-junction case, the BTBT rate in the homojunction is peaked at the interface because of similar doping levels on both sides of the junction.

In tunnel diodes biased strongly in forward direction (>1.6 V), we observed that the excess currents increased irreversibly. Figure 3A shows such a case, where the diode was initially measured up to 0.5 V forward and negative bias, following a sweep to 1.7 V forward bias. Note that the reverse tunnel currents and the forward direct tunnel currents are almost unaffected by this stressing procedure in contrast to the excess current. This phenomenon can be observed also at room temperature, where the only difference is that smaller voltages are needed (>0.75 V) to cause the degradation. This stress effect first of all leads to a reduction of the PVCR as seen in the $I-V$ characteristics of Figure 3A and in the first derivative (Figure 3B). Another effect observed is that defect-related peaks that exist prior to the stressing became more pronounced (Figures 2B and C). New trap levels are also created, causing a broadening in energy of the trap levels that leads to an overall increase of the conductance, and in general, an increased noise level. If many traps are created that lie energetically close together, the structure in dI/dV gets smeared out as depicted in Figure 3B for voltages above 150 mV. This degradation effect was only observed in the most highly

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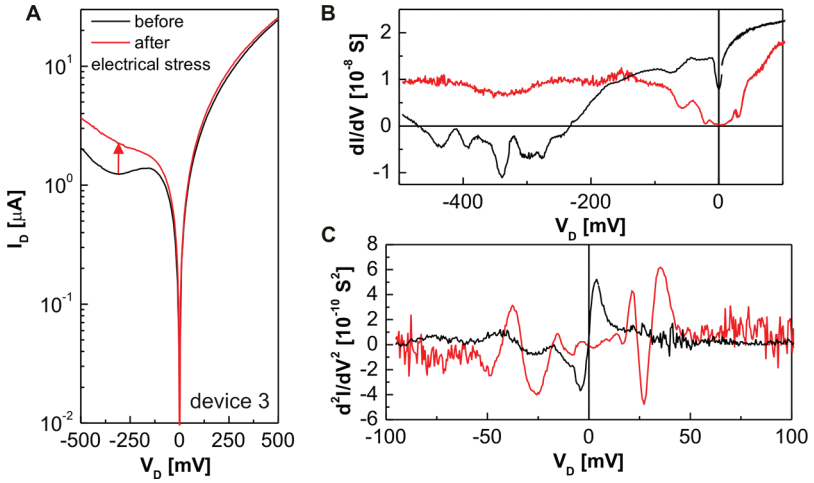

Figure 3. Electrical stress applied to tunnel diodes. (A) $I-V$ characteristics of a Si-InAs tunnel diode before (black) and after (red) electrically stressing the diode by applying 1.7 V forward bias at 4.2 K. (B) Conductance before and after having stressed the interface at 4.2 K. A loss of NDR and a broadening of the peaks are observed, which indicate the formation of additional trap states due to defects at the heterointerface. (C) In the second derivative, peaks are more pronounced after electrically stressing of the junction (red) and in the reverse bias new peaks show up, confirming the generation of new defects at the interface.

doped diodes (Si, 1×10^{20} cm^{-3}; InAs, $\sim 5 \times 10^{18}$ cm^{-3}),[6] indicating that the electric fields are very high and the tunnel distances extremely small. Hence the increase in excess current is interpreted as an increase in the number of defects at the interface caused by the voltage stress, producing heat and other high-field effects.

These results might impact TFETs because defect states inside the band gap allow tunneling to occur when the TFET would normally be in the off-state.[16] This leads to a degradation of the subthreshold slope and is detrimental to the switching characteristics. States induced by dislocations or point defects at the heterojunctions could therefore severely affect the subthreshold performance. One way of circumventing this problem would be to avoid the dislocations and defects altogether. This may be possible by scaling the InAs nanowire diameters below the critical size where dislocations will not form.[17] However, for a lattice mismatch of 11.6%, if at all possible extreme scaling far below 20 nm cross sections would be necessary.[18] At this point, quantum size effects would also change the band structure and affect the tunneling probabilities. Another solution consists of forcing the tunneling generation rates away from the heterojunction into one of the materials away from the trap levels to benefit from bulklike tunneling behavior of III−V materials, as demonstrated here.

In conclusion, we have shown that trap-assisted tunneling occurs in lattice-mismatched Si-InAs heterojunction tunnel diodes by studying the low-temperature conductance. The traps are located in the band gap and stem from dislocations, as confirmed by TEM, as well as from point defects at or close to the heterointerface. Furthermore, by electrically stressing the junctions more defects can be irreversibly induced at both room and low temperature. Finally, we have shown that for these one-sided junctions, the tunneling occurs at the interface for low voltages in forward direction but shifts into the InAs for higher reverse biases as predicted by modeling.[13]

■ ASSOCIATED CONTENT

Supporting Information. Additonal information and figures. This material is available free of charge via the Internet at http://pubs.acs.org.

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■ REFERENCES

(1) Esaki, L. *Phys. Rev.* **1958**, *109*, 603.
(2) Chang, L.; Frank, D.; Montoye, R. K.; Koester, S. J.; Ji, B. L.; Coteus, P. W.; Dennard, R. H.; Haensch, W. *Proc. IEEE* **2010**, *98*, 215.
(3) Choi, W. Y.; Park, B.-G.; Lee, J. D.; King, Lu, T.-J. *IEEE Electron Device Lett.* **2007**, *28*, 743.
(4) Verhulst, A. S.; Vandenberghe, W. G.; Maex, K.; De Gendt, S.; Heyns, M. M.; Groeseneken, G. *IEEE Electron Device Lett.* **2008**, *29*, 1398.
(5) Björk, M. T.; Ohlsson, B. J.; Sass, T.; Persson, A. I.; Thelander, C.; Magnusson, M. H.; Deppert, K.; Wallenberg, L. R.; Samuelson, L. *Appl. Phys. Lett.* **2002**, *80*, 1058.
(6) Björk, M. T.; Schmid, H.; Bessire, C. D.; Moselund, K. E.; Ghoneim, H.; Karg, S.; Lörtscher, E.; Riel, H. *Appl. Phys. Lett.* **2010**, *97*, 163501.
(7) Chynoweth, A. G.; Feldmann, W. L.; Logan, R. A. *Phys. Rev.* **1961**, *121* (3), 684.
(8) Schenk, A. *Solid-State Electron.* **1992**, *35* (11), 1585.
(9) Tomioka, K.; Motohisa, J.; Hara, S.; Fukui, T. *Nano Lett.* **2008**, *8* (10), 3475.
(10) Shockley, W. *Phys. Rev.* **1953**, *91*, 228.
(11) Read, W. T. *Philos. Mag.* **1954**, *45* (367), 775.
(12) Sah, C. T. *Phys. Rev.* **1961**, *123* (5), 1594. Chynoweth, A. G.; Logan, R. A.; Thomas, D. E. *Phys. Rev.* **1962**, *125* (3), 877.
(13) Schenk, A.; Rhyner, R.; Luisier, M.; Bessire, C. Analysis of Si, InAs, and Si-InAs Tunnel Diodes and Tunnel FETs Using Different Transport Models. *Proc. Int. Conf. SISPAD* **2011**.

(14) *Sentaurus Device User Guide*, version 2009.06; Synopsys, Inc.: Mountain View, California, 2009.
(15) The simulations were performed for 300 K to ensure convergence. Therefore the absolute BTBT rate deviates from the real tunnel rate at 4.2 K, but the trend of the spatial shifts of the generation profiles are correct.
(16) Mookerjea, S.; Mohata, D.; Mayer, T.; Narayanan, V.; Datta, S. *IEEE Electron Device Lett.* **2010**, *31* (6), 564.
(17) Ertekin, E.; Greaney, P. A.; Chrzan, D. C.; Sands, T. D. *J. Appl. Phys.* **2005**, *97*, 114325.
(18) Tomioka, K; Fukui, T. *Appl. Phys. Lett.* **2011**, *98*, 083114.

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