Performance predictions of single-layer In-V double-gate n- and p-type field-effect transistors

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***Abstract*—Through *ab-initio* quantum transport simulations the logic performance of single-layer InAs, InN, InP, and InSb III-V compounds is analyzed in this paper for n- and p-type applications. The key findings are that (i) the low electron effective masses of all these materials lead to very similar and attractive ON-currents in n-type transistors, but cause a rapid deterioration of their sub-threshold swing as the gate length shrinks to 10 nm and below, (ii) the p-type devices show much smaller and scattered current values that are too low to eventually challenge Si FinFETs, and (iii) the density-of-states bottleneck effect strongly influences the behavior of the n-type devices.**

INTRODUCTION

Over the last decade single-layer two-dimensional (2D) materials have emerged as new candidates to realize next-generation nanoscale logic switches. After the exfoliation of graphene [1] novel fabrications methods have made possible the discovery of alternative 2D materials such as hexagonal boron nitride (BN) [2], molybdenum disulfide (MoS_2) [3], and more recently phosphorene, i.e. single-layer black phosphorus [4]. The number of monolayer 2D crystals that have been isolated so far remains very low, thus leaving unexplored thousands of components with potentially exciting electrical, thermal, and/or optical properties.

In order to support the on-going experimental efforts computer simulations based on *ab-initio* methods, e.g. density-functional theory (DFT) [5], can be deployed to determine the stability of monolayer structures. Such studies have been applied to III-V compounds. Among them the family of InX (X = N, P, As, and Sb) has been predicted to exist at room temperature, either in a single-layer hexagonal honeycomb (InN) or buckled honeycomb (InAs, InP, and InSb) lattice, as illustrated in Fig. 1.

To date only material characterizations and electronic structure calculations have been reported for the aforementioned 2D materials [6]. With semiconductor-like band gaps in the range of 1.2 to 1.8 eV and small transport effective masses going from 0.07 to 0.13 m_0 the InX monolayers could find potential applications as future ultra-scaled transistors beyond Si FinFETs. This scenario has not been investigated so far. Here, we therefore go one step further and present the first *ab-initio* ballistic quantum transport simulations of single-layer n- and p-type double-gate field-effect transistors (FETs) with an InX channel. After a short summary of the modeling approach a detailed analysis of the device performance will be provided. While ON-current values larger than 5 mA/μm can be reached by all materials in the n-type configuration, the p-type results are more modest (I_{ON} below 1.8 mA/μm) and the scaling of the gate length below 10 nm, even with a double-gate contact, does not appear as a reasonable option.

SIMULATION APPROACH

The performed quantum transport simulations rely on the first-principles approach introduced in Ref. [7]. The whole process starts with the DFT calculation of the primitive unit cell of each semiconductor with the plane-wave code VASP [8]. The projector augmented wave (PAW) method and the generalized gradient approximation (GGA) with the Perdew-Burke-Ernzerhof (PBE) parametrization [9] have been used for the ionic structural relaxations, whereas the Heyd-Scuseria-Ernzerhof (HSE06) hybrid functionals [10] have been employed for the exchange-correlation potential and to compute the desired electronic bandstructures. A cutoff energy of 500 eV has been set to the plane-wave basis and a $8 \times 1 \times 8$ Γ k-point mesh has been utilized throughout all calculations. A vacuum spacing of 15 Å has been introduced to ensure that interactions between the single-layer and their images are negligible. The resulting structural parameters (lattice constant and buckling height) are listed in Table I.

As a next step the plane-wave outputs of VASP have been transformed into a set of maximally localized Wannier functions (MLWFs) with the WANNIER90 tool [11]. By considering four orbitals per In and "X" atom four valence and four conduction bands have been produced. The disentanglement of the subspace of the 8 Wannier functions has been done over an energy window that contains all valence bands and the two lowest conduction bands. The quadratic spread of each MLWFs has been found to be less than or approximately 3 Å^2. Finally, a tight-binding-like Hamiltonian has been constructed for the entire device structure based on the MLWFs of each primitive unit cell. It accurately reproduces the original DFT bandstructures, as can be seen in Fig. 2. After transferring the generated Hamiltonian into a state-of-the-art atomistic quantum transport simulator that self-consistently solves the Schrödinger and Poisson equations [12] the *I-V* characteristics of ultra-scaled single-layer InX transistors have been calculated and compared to each other.

RESULTS

The n- and p-type device structures examined in this work are schematized in Fig. 1. They are double-gate field-effect transistors with single-layer InX as channel

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materials, a nominal gate length L_g=15 nm, source and drain extensions of length L_s=L_d=15 nm with a doping concentration $N_{A/D}$=2e13 cm^{-2}, and two oxide layers of thickness t_{ox}=3 nm and relative permittivity ϵ_R=20. A supply voltage of V_{DD}=0.65 V has been chosen to be in line with future technology nodes. The hexagonal buckled honeycomb lattice and the DFT bandstructures of the InX components, as obtained from VASP and maximally localized Wannier functions, are given in Figs. 1 and 2, respectively, together with the corresponding electron and hole effective masses at the conduction and valence band extrema. The InX monolayers have an direct band gap between Γ (CB) and K (VB), except InN, for which CB_{min} and VB_{max} are at Γ.

The intrinsic transfer characteristics of the monolayer InSb n- and p-FET are plotted in Fig. 3 on a linear and logarithmic scale. The effect of the contact resistances has not been taken into account in these simulations. It is expected to significantly reduce the extracted currents. Consequently, the computed ON-currents should be much larger than 1 mA/μm, the typical Si FinFET value [13], to be competitive with this architecture. This is the case of single-layer InSb, which offers the best compromise between high n- and p-type performance although a strong asymmetry exists between them: the I_{ON} of the n-FET exceeds that of the p-FET by a factor of 2.5 (4.8 vs. 1.8 mA/μm), but also that of Si FinFETs by a factor of $\sim$5. A careful inspection of the electron m_e and hole m_h effective masses in Table II explains this inbalance, m_e being $\sim$9 times smaller than m_h.

The ON-current of 2-D InSb n-FETs certainly benefits from the underlying low electron transport effective mass, but the latter has a negative impact on the scalability of such devices because it contributes to a drastic increase of source-to-drain (S-to-D) tunneling. This effect can be clearly seen in Fig. 3(c): the OFF current rapidly increases as the gate length L_g goes down from 15 to 5 nm.

Fig. 4 reports the I_d-V_{gs} of the n- and p-type double-gate transistor with an InAs, InN, and InP channel and summarizes their ON-current and sub-threshold swing at L_g=15 nm. Note that the simulations of the p-FETs did not converge as well as their n-FET counterparts, explaining the larger noise in the *I-V* characteristics. Three important facts should be highlighted here: (i) the n-type ON-currents are almost identical with $\leq$10% deviations, much less than for the electron effective masses (50% difference between InSb and InN), (ii) the p-FETs see much larger ON-current discrepancies of roughly 40% between InP and InSb, and (iii) the sub-threshold swings at L_g=15 nm remain close to their ideal 60 mV/dec value due to limited S-to-D tunneling.

To understand the homogeneity (variability) in the n-(p-)FET ON-currents it is useful to inspect the charge density at the top-of-the-potential-barrier (ToB) in all simulated devices. These quantities are illustrated in Fig. 5, where the extraction method is also described. It can be observed that the slope of the electron concentration at the ToB, which is proportional to the gate capacitance, differs from one channel material to the other. The one with the largest effective mass (InN) has the steepest slope. This finding definitively indicates that the n-type switches operate close to their quantum capacitance limit so that the density-of-states (DOS) bottleneck plays a major role and compensates for the higher injection velocity of materials with a smaller effective mass, see Fig. 6(a) for the velocity and ToB charge results. This is not the case of the p-FETs, where the slope of the hole density at the ToB does not vary much from one monolayer to the other. Hence, the ON-current is inversely proportional to the hole effective mass and is not influence by the DOS bottleneck.

Finally, the scalability of the InX n- and p-type transistors is studied in Fig. 6(b-c). To do that, the gate length of all devices has been reduced from 15 to 10 and then 5 nm before the sub-threshold swing SS has been extracted. As mentioned above, at L_g=15 nm, the double-gate configuration provides an excellent electrostatic integrity and allows for a quasi-ideal behavior. When L_g reaches 10 nm, SS slightly increases to $\sim$80 mV/dec, which remains an acceptable value. In the shortest structures, the inflation of SS becomes so large that no proper switching operation is possible.

Conclusion

Transistors with a 2-D InX channel have been simulated with a fully *ab-initio* device modeling approach. It has been shown that the n-type transistor could reach ON-currents as high as 5 mA/μm, about 5$\times$ more than Si FinFETs, if the effect of the contact resistances is neglected. Nevertheless, this great advantage over Si that neither idealized single-layer MoS_2 [14] nor black phosphorus [15] could achieve might not be sufficient to justify the replacement of Si by 2-D InX.

Acknowledgment

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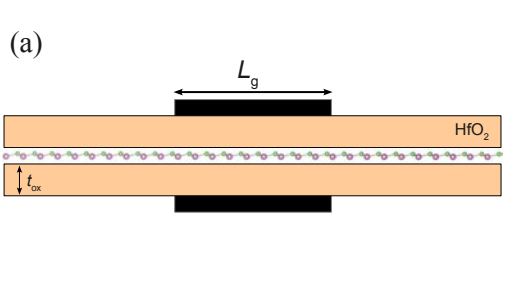
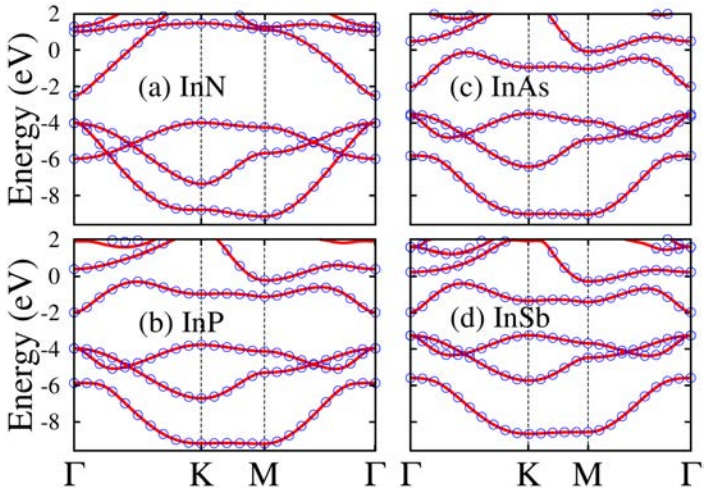


(c) Table I: Structural parameters

InX	Lattice constant a(Å)	Buckling Δ(Å)
InN	3.58	0
InP	4.25	0.54
InAs	4.35	0.60
InSb	4.70	0.77

Fig. 1. (a) Schematic view of the single-layer, double-gate, n- and p-type field-effect transistors with a 2-D InX channel considered in this work. The gate length is originally set to L_g=15 nm, while the source and drain regions extend over L_s=L_d=15 nm and are doped with a donor (acceptor) concentration N_D=2×10^{13} cm^{-2} (N_A=2×10^{13} cm^{-2}) in the n-type (p-type) conguration. The equivalent oxide thickness of all transistors is equal to EOT=0.58 nm (3 nm of HfO_2 with $\varepsilon_{\mathrm{high}-\kappa}$=20). In all devices the out-of-plane direction is assumed periodic and is modeled via 15 momentum points. (b) Top and side views of the atomic structure of a buckled honeycomb structure alternating atoms in two different parallels planes. The buckling Δ is the distance between these two planes. The lattice vectors for each structure are given with $|\mathbf{a_1}| = |\mathbf{a_2}| = a$. (c) Summary of the structural parameters for each of the InX materials.



(e) Table II: Electronic properties of the 2D InX materials

InX	m_e/m_0	$m_{h,K}/m_0$	$E_{g,\Gamma K}$(eV)	$\Delta E_{v,\Gamma K}$(eV)	ε
InN	0.13	--	1.46	-0.02	4.08
InP	0.11	0.97	1.79	0.19	3.64
InAs	0.08	0.65	1.43	0.02	4.74
InSb	0.07	0.67	1.26	0.01	5.80

Fig. 2. Electronic bandstructure as calculated with the VASP tool (red lines) [8] and as obtained after a transformation into the maximally localized Wannier function basis used in quantum transport simulations (blue circles). The results for (a) InN, (b) InP, (c) InAs, and (d) InSb are shown. (e) Summary of the InX material parameters extracted from the bandstructures (a)-(d): electron (hole) effective mass m_e ($m_{h,K}$), indirect band-gap energy $E_{g,\Gamma K}$, and the energy difference $\Delta E_{v,\Gamma K}$ between the valence band edges at the symmetry points Γ and K. Only in case of InN $\Delta E_{v,\Gamma K} < 0$ meaning that it is a direct band gap material. The macroscopic dielectric constant ε are taken from Ref. [6].

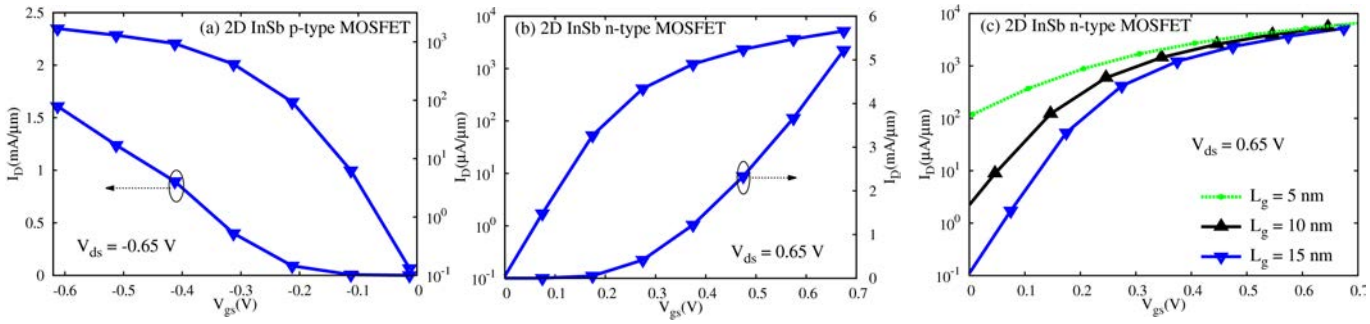
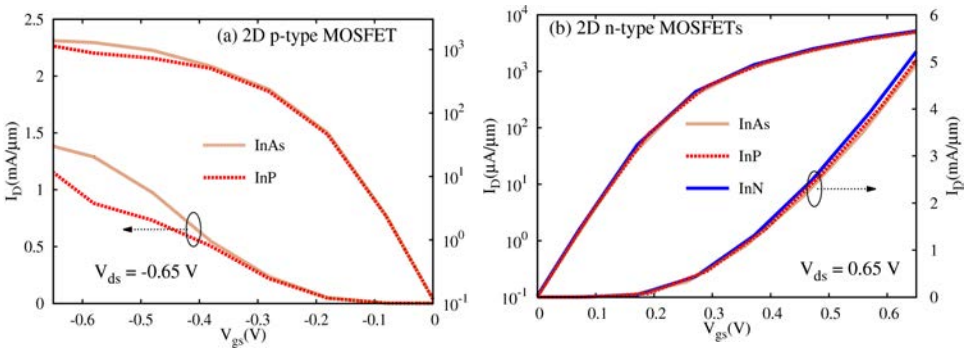


Fig. 3. Transfer characteristics I_d-V_{gs} at V_{ds}=V_{DD}=-0.65 V through a 2D monolayer InSb p-type FET with L_g=15 nm. The OFF-current is set to 0.1 μA/μm, while the ON-current is extracted at I_{ON}=I_d at V_{gs}=V_{ds}=V_{DD}. A linear and logarithmic scale are provided. (b) Same as (a), but for the n-type configuration. (c) Comparison of the transfer characteristics of 2D InSb n-type FETs with different gate lengths ranging from L_g=5 to 15 nm. The shorter L_g the higher is the current at V_{gs}=0 V, increasing the source-to-drain tunneling leakage current and deteriorating the sub-threshold swing of the device.



(c)	InX	I_{ON} (mA/μm)	SS(mV/dec)
n-type	InN	5.21	61.3
	InP	5.01	61.6
	InAs	4.95	62.0
	InSb	4.81	62.5
p-type	InP	1.10	61.4
	InAs	1.40	60.9
	InSb	1.81	60.0

Fig. 4. Transfer characteristics I_d-V_{gs} of 2D InX (a) p- and (b) n-type FETs with $L_g = 15$ nm. (c) Summary of the performance of 2D InX FETs. Three important facts should be highlighted: (i) the n-type ON-currents are almost identical with $\leq$10% deviations, much less than for the electron effective masses (50% difference between InSb and InN), (ii) the p-type FETs see much larger ON-current discrepancies of roughly 40% between InP and InSb, and (iii) the sub-threshold swings remain close to their ideal 60 mV/dec value due to limited S-to-D tunneling.

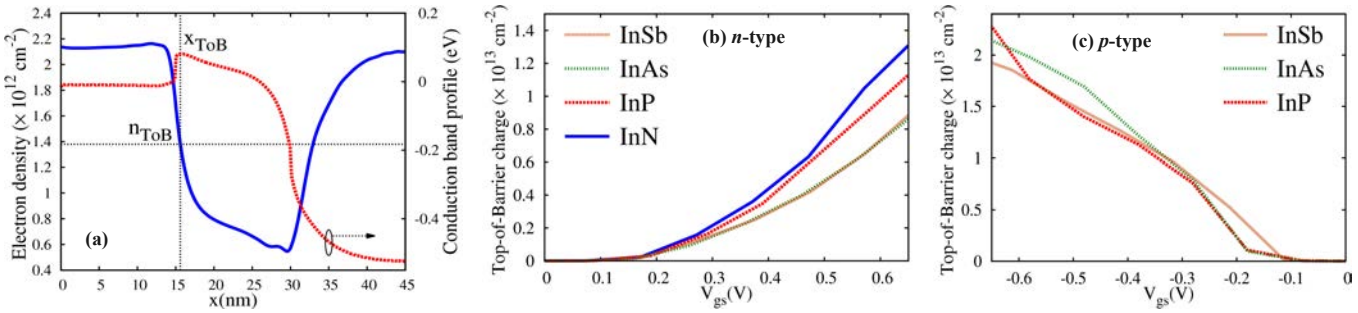


Fig. 5. (a) Electron density (blue line) and conduction band profile (red dashed-line) along the device at ON-state. The position (x_{ToB}) and electron density (n_{ToB}) at the top-of-barrier (ToB) are schematically marked by vertical and horizontal dashed-lines, respectively. (b) Electron and (c) hole (p_{ToB}) concentrations at ToB separating the source and drain extensions of 2D InX material FETs investigated in this work. They are reported as a function of the applied V_{gs}. It can be observed that the slope of the electron concentration at the ToB differs from one channel material to the other. The one with the largest effective mass (InN) has the steepest slope. This finding definitively indicates that the n-type switches operate close to their quantum capacitance limit so that the density-of-states (DOS) bottleneck plays a major role and compensates for the higher injection velocity of materials with a smaller effective mass for the velocity and ToB charge results. This is not the case of the p-FETs, where the slope of the hole density at the ToB does not vary much from one monolayer to the other. Hence, the ON-current is inversely proportional to the hole effective mass and is not influence by the DOS bottleneck.

(a)	InX	n_{ToB}/p_{ToB}(cm^{-2})	v_{inj} (cm/s)
n-type	InN	1.33×10^{13}	2.43×10^{7}
	InP	1.13×10^{13}	2.80×10^{7}
	InAs	8.59×10^{12}	3.59×10^{7}
	InSb	8.79×10^{12}	3.24×10^{7}
p-type	InP	2.2×10^{13}	3.10×10^{6}
	InAs	2.13×10^{13}	4.12×10^{6}
	InSb	1.95×10^{13}	5.79×10^{6}

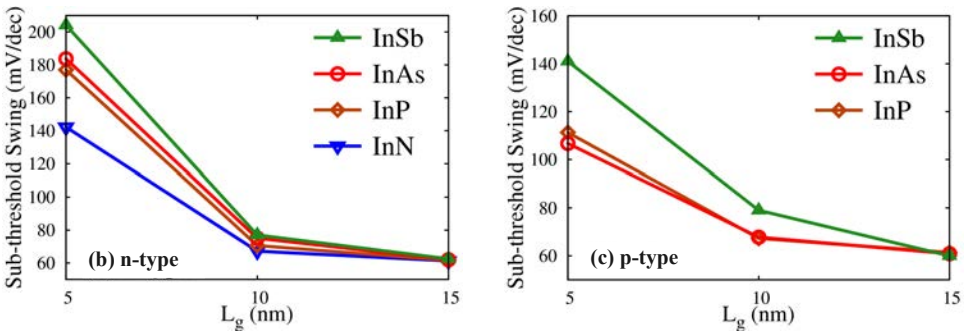


Fig. 6. (a) Summary of n_{ToB}, p_{ToB}, and injection velocity (v_{inj}) at the ToB in the ON-state of the 2D InX FETs. (b) Sub-threshold swing of the 2D InX n-type FET as a function of its gate length. (c) Same as in (b), but for a p-type FET. The gate length of all devices has been reduced from 15 to 10 and then 5 nm before the sub-threshold swing SS has been extracted. When L_g reaches 10 nm, SS slightly increases to ~80 mV/dec. In the shortest structures, the SS becomes so large that no proper switching operation is possible.