Design of High-Performance InAs–Si Heterojunction 2D–2D Tunnel FETs With Lateral and Vertical Tunneling Paths

Hamilton Carrillo-Nuñez, Mathieu Luisier, and Andreas Schenk

***Abstract*— Double-gate tunneling FETs (TFETs) exploiting the 2D density-of-state switch are studied. A full-band and atomistic quantum transport simulator based on the $sp^3d^5s^*$ tight-binding model is used to solve the quantum transport problem taking into account both lateral and vertical band-to-band tunneling paths. The tunneling paths are identified by means of the calculation of the electron and hole generation rates. They are computed with an in-house tool based on the Flietner imaginary dispersion and a non-local path band-to-band tunneling model. First, a InGaAs electron–hole bilayer TFET is investigated. It is found that the suppression of lateral tunneling components is crucial to obtain a steep slope in this device. On the other hand, the presence of both tunneling components can boost the ON-current of TFETs. The latter can be achieved by implementing an InAs–Si heterostructure as 2D–2D TFET. Such a combination offers a device solution with both steep subthermal subthreshold swing and high ON-current. In the best case of an extremely thin InAs–Si 2D–2D TFET, the minimal swing would be SS = 28 mV/decade and the ON-current would reach 240 μA/μm.**

***Index Terms*— 2D–2D density-of-state (DOS) switches, InAs–Si tunnel FETs, lateral and vertical band-to-band tunneling (BTBT).**

I. Introduction

BAND-TO-BAND tunneling (BTBT) FETs are being considered as promising candidates on the road toward energy-efficient transistors [1]. However, their ON-current is significantly lower compared with conventional MOSFETs. Fig. 1(b) shows the sketch of a tunneling FET (TFET) exploiting both, the source–channel lateral ("point") BTBT along the transport direction, and additional components known as "line tunneling" [2], [3] with tunneling paths almost perpendicular to the gate. TFETs with both lateral and vertical tunneling paths are expected to boost the ON-currents to much higher values than those resulting from lateral BTBT components alone. In the OFF-state, however, lateral tunneling components are dominant causing a high OFF-current. The lowering of the OFF-state leakage current is one of the challenges to make truly steep-slope TFETs become reality. By employing only line tunneling components in TFETs, the OFF-state current could be significantly reduced, since the lateral tunneling paths are diminished. But, as we will show later in this paper, blocking the lateral tunneling could negatively impact the performance of TFETs in their ON-state. The line tunneling in TFETs is an example for the matching of two density of states (DOS) with different dimensionalities, since the BTBT occurs from a 3D DOS of a bulk-like system to the 2D DOS of the confined carrier gas at the semiconductor–oxide interface. TFETs featuring DOSs with reduced and/or different dimensionalities are also called *DOS switches* [4]. Roughly speaking, a reduction of the dimensionality of the DOS will make it "sharper" and, therefore, will yield a very low subthreshold swing (SS). The latter has aroused interest for other dimensionality combinations in TFETs. Recently, a new architecture known as electron–hole bilayer TFET (EHBTFET) [5] with vertical BTBT between a 2D electron gas and a 2D hole gas has been proposed. Although the idea of the EHBTFET is to enhance the BTBT current, so far, both experimental and numerical results agree upon a reduced ON-current [6], mainly due to size- and bias-induced quantization. Indeed, a 1-DEG and a 2-DEG can only be formed by strong geometrical confinement which inevitably increases the bandgap, i.e., the height of the tunnel barrier, with the consequences of a higher onset voltage and a reduced ON-current.

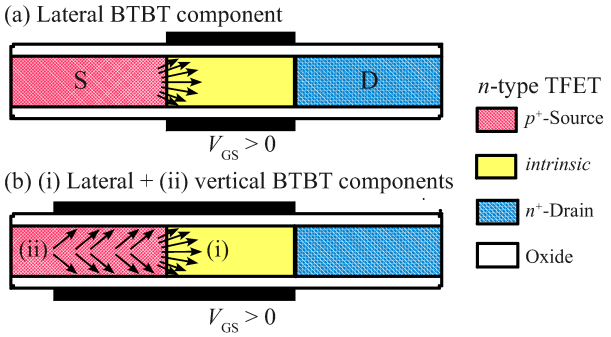

Fig. 1. Schematic of a double-gate n-type TFET exploiting (a) lateral BTBT, e.g., from source (S) to the intrinsic/drain (D) region, and (b) both lateral and vertical BTBT components. Notice that the vertical BTBT components occur under and almost perpendicular to the gate in the source.

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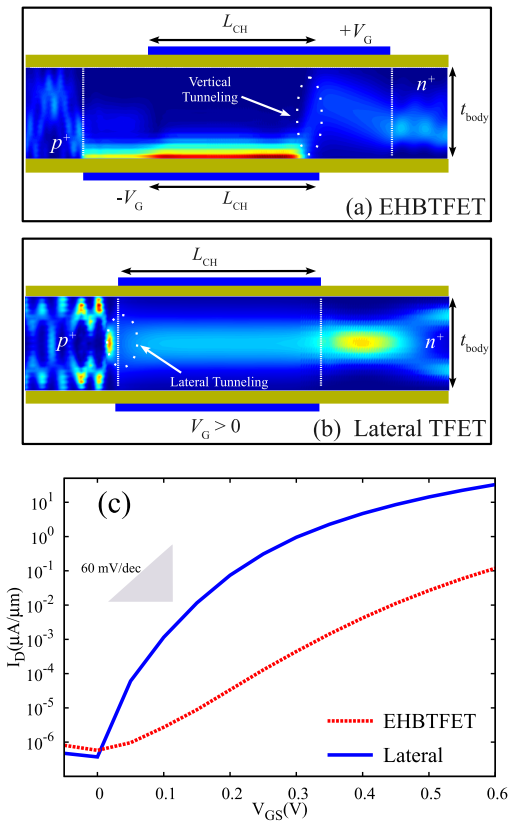

Fig. 2. (a) Schematic of a 2D–2D InGaAs TFET known as EHBTFET and the spatial current distribution at $V_{GS} \approx 0.5$ V. Notice that the applied gate voltage on the top is positive ($+V_{GS}$) and negative ($-V_{GS}$) in the bottom. (b) Schematic of a conventional InGaAs n-type lateral TFET and the spatial current distribution at $V_{GS} \approx 0.5$ V computed with OMEN. The white circles mark the regions where vertical and lateral tunneling occur in (a) and (b), respectively. (c) Corresponding I_D–V_{GS} characteristics of devices (a) and (b) at room temperature. The source–drain bias is $V_{DS} = 0.5$ V. The curves have been shifted to match approximately the same OFF-current.

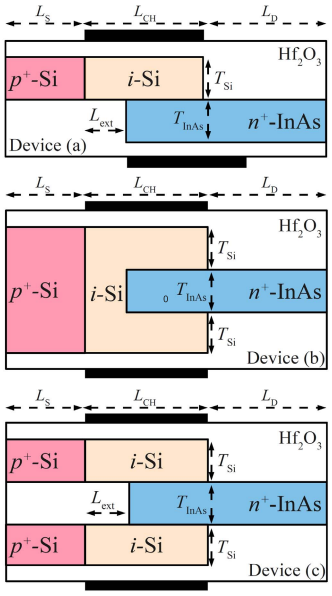

Fig. 3. Schematic of 2D–2D TFETs studied in this paper. $L_S = 15$ nm, $L_{CH} = 30$ nm, and $L_D = 25$ nm. The oxide thickness under the gate region is $T_{ox} = 1$ nm, whereas the doping concentrations for the source (n^+-type InAs region) and drain (p^+-type Si region) are $N_D = N_A = 5 \times 10^{19}$ cm^{-3}. $L_{ext} = 15$ nm for devices (a) and (c). The temperature in the devices is assumed to be 300 K.

In this paper, we investigate the performance of 2D–2D TFETs. First, we study the case of an InGaAs double-gate n-type TFET in lateral and EHBTFET configuration (see Fig. 2). The aim is to highlight, by the comparison of both devices, the benefits of each tunneling component. The corresponding findings will help to understand more sophisticated devices such as InAs–Si heterostructure 2D–2D TFETs considered later on. InAs–Si [3], [7]–[9] heterojunction TFETs have been identified over the last years as promising architectures to attain respectable ON-current when compared with MOSFETs. However, to date, there are no experimental demonstrations of InAs–Si TFETs that provide the desired characteristics. Trap-assisted tunneling (TAT) has been found to be dominant in InAs–Si TFETs resulting in SSs higher than 100 mV/decade [3], [9]. Equally important is the impact of phonon scattering on TFET performance. In the InAs–Si material configuration the BTBT is mainly direct, no phonon-assisted tunneling (PAT) is needed to transfer electrons from the valence band (VB) of Si into the conduction band (CB) of InAs. No PAT was observed in Esaki bulk-like diodes [10]. However, more recently, the impact of electron–phonon interactions on InAs–Si extremely narrow nanowire TFETs has been studied [11]. It has been reported that phonon scattering has no effect on the ON-state of the TFET, whereas in the OFF-state of the device, electron–phonon interactions have a detrimental impact, increasing the OFF-current and affecting the TFET performance by leading to less steep subthreshold slopes. Although the inclusion of TAT and PAT in the simulations is necessary for a more realistic assessment of device performance, they are not considered here. The goal of this paper is to shed light on the important role of lateral tunneling components for realizing high-performance TFETs.

Combining heterostructures with a 2D–2D DOS matching may lead to a tradeoff in the performance, i.e., in the I_{ON}/I_{OFF} ratio. To maximize the performance, a high ON-current and a steep (subthermal) SS are required. The InAs–Si 2D–2D TFETs under study are shown in Fig. 3. The full-band and atomistic quantum transport tool OMEN [12], which is based on an $sp^3d^5s^*$ tight-binding representation of the band structure, has been employed for the device simulations. Despite the TB efficiency to compute semiconductor band structures, as any other empirical model ($\mathbf{k} \cdot \mathbf{p}$, pseudopotentials), it suffers from several deficiencies, e.g., the unspecified wave function in the confinement direction or the proper description of the VB and CB offset in case of heterostructures. As for the first one, wave functions can be always computed in a postprocessing step if needed, whereas, the band alignment in heterostructures should be an input of the TB model. For InAs and Si, we used the value extracted by IBM in the case of bulk-like InAs–Si nanowires as a reference [3], [9]. This is how Si and InAs bands align in the bulk configuration of the TB model. Then, the results will depend on the choice of the initial band alignment. The impact of the variation of VB/CB offset is studied in Section III.

2D–2D TFETs based on metal-dichalcogenides (MoS_2 for the n-side and WTe_2 for the p-side) had already been investigated with OMEN [13]. Its multidimensional capabilities make it a suitable tool to analyze 2D–2D TFETs taking into account the strong impact of quantization effects on the BTBT along all the possible paths. In order to identify the tunneling paths, we have also implemented an analytic model into an in-house tool to compute the electron/hole BTBT generation rate, based on a non-local path BTBT model and the two-band Flietner model of the imaginary dispersion [14]. Details are given in the Appendix. As this tool just serves for visualization purposes, we neglected channel quantization and geometrical confinement in the computation of the rates. Direction and location of the tunneling paths are not essentially changed by this simplification and the general conclusions of this paper are preserved.

II. InGaAs 2D–2D TFETs

In Fig. 2, an $In_{0.53}Ga_{0.47}As$ n-type lateral TFET and the 2D–2D TFET called EHBTFET [5] are compared with each other. $In_{0.53}Ga_{0.47}As$ has been chosen, contrary to InAs used in Section III, due to its larger gap that reduces the OFF-state leakage currents. For both devices, the gate length and the body thickness are $L_{CH} = 50$ nm and $t_{body} = 5$ nm, respectively. The source and drain regions are highly doped with $N_A = N_D = 4 \times 10^{20}$ cm^{-3}. The oxide thickness is 3 nm with a permittivity $\varepsilon_{high-k} = 20$.

Opposite voltages are applied to both EHBTFET gate contacts, i.e., a positive bias ($+V_{GS}$) to the top-gate and a negative one ($-V_{GS}$) to the bottom-gate, as shown in Fig. 2(a). In EHBTFETs, a 2-DEG and a 2-DHG are formed at the top and bottom semiconductor–oxide interfaces, respectively. By turning ON the source-to-drain voltage $V_{DS} > 0$, it is expected that holes in the VB tunnel to the CB perpendicular to the gates. This is observed in the spatial current distribution of the EHBTFET at $V_{GS} = 0.5$ V and $V_{DS} = 0.5$ V. The lateral tunneling paths are diminished due to the wider potential barrier in front of the gate-underlap regions.

In lateral TFETs, the same gate voltage (V_{GS}) is applied to both gates. Fig. 2(b) shows the schematic of a n-type lateral TFET and its corresponding spatial current distribution at $V_{GS} = 0.5$ V and $V_{DS} = 0.5$ V computed with OMEN. Contrary to EHBTFETs, the BTBT occurs at the p-source/intrinsic-channel interface parallel to the gates as observed in the spatial current distribution of the lateral TFET in Fig. 2(b).

Fig. 2(c) shows the corresponding I_D–V_{GS} characteristics of the InGaAs n-type lateral TFET and EHBTFET. When comparing both I_D–V_{GS} curves, it is observed that the lateral TFET performs better, yielding higher currents, and a steeper subthreshold slope than the EHBTFET. The lateral TFET ON-current is at least two orders of magnitude higher than the one of the EHBTFET. As shown in Fig. 2(c), the EHBTFET is not being abruptly switched ON, contrary to what is expected in theory for this kind of devices. In reality, 2D–2D TFETs cannot be abruptly switched ON due the parasitic lateral leakage tunneling paths that always persist. In case of the EHBTFET shown in Fig. 2(a), the lateral leakage current in the OFF-state is dominant and takes place mainly under the gate underlap regions of the channel. In the ON-state, the vertical tunneling is dominant and the lateral tunneling paths disappear. However, EHBTFET performance could be optimized by reaching a compromise between the device dimension, material parameters, and by applying sophisticated techniques to create underlap counterdoping regions that could significantly reduce the lateral leakage tunneling improving the subthreshold slope, as reported recently in [15].

The presence of both tunneling components would boost the ON-state current of the TFET but is also detrimental in its OFF-state due to the lateral leakage current. In order to obtain very low OFF-currents, lateral tunneling paths should be suppressed in the subthreshold regime to allow only vertical tunneling paths to be dominant. In Section III, we present some examples of InAs–Si 2D–2D TFETs where the latter has been achieved.

III. InAs–Si 2D–2D TFETs

Fig. 3 shows the design of InAs–Si heterojunction 2D–2D TFETs, which are studied in this paper: a 2D n^+-InAs quantum well (QW) (source) laid [devices (a) and (c)] or embedded [device (b)] on a 2D $\langle 111 \rangle$ Si QW. The gate length is 30 nm and the total device length is 65 nm. T_{InAs} and T_{Si} are the InAs and Si thicknesses, respectively. The doping concentrations are $N_D = N_A = 5 \times 10^{19}$ cm^{-3}, whereas the effective oxide thickness is 0.43 nm. The work function of the gates is set to 4.05 eV for all the devices. Ballistic device simulations were performed with OMEN and an in-house postprocessing tool for the electron and hole generation BTBT rates. Contrary to the EHBTFET, the same $V_{GS} < 0$ V is applied on both bottom and top gates of the devices in Fig. 3.

The values for SS are the minimal swing and the ON-currents are the maximal currents found for a given source–drain bias. Note that only in semiclassical simulations, the onset voltage can be determined by a threshold BTBT current, which exceeds the Shockley–Read–Hall generation current of the reversed-biased diode. This allows a proper averaging of SS over a few orders of magnitude in the current and a proper definition of the ON-current based on a given "overdrive" voltage. Here, as only ballistic BTBT currents are calculated, one has to use the (practically meaningless) point slope to compare the different structures and can only extract the "ON-current" at a particular V_{GS}, i.e., at $V_{GS} = -1$ V.

Fig. 4 compares the I_D–V_{GS} characteristics of the three different InAs–Si 2D–2D pTFETs with $T_{InAs} = T_{Si} = 2$ nm in all cases and $V_{DS} = -0.5$ V. As can be seen, the device (b) offers a better tradeoff than its counterparts, with higher ON-current ($>10^2$ μA/μm) and SS = 28 mV/decade. Although the device (a) presents a higher ON-current than the device (c), its subthreshold slope is the less steep with SS $>$ 60 mV/decade. Therefore, device (a) will be disregarded from now on in this paper, and we will focus our analysis on the two device structures (b) and (c) which look more promising.

From the comparison of the I_D–V_{GS} characteristics of devices (b) and (c) in Fig. 4, one can indirectly distinguish

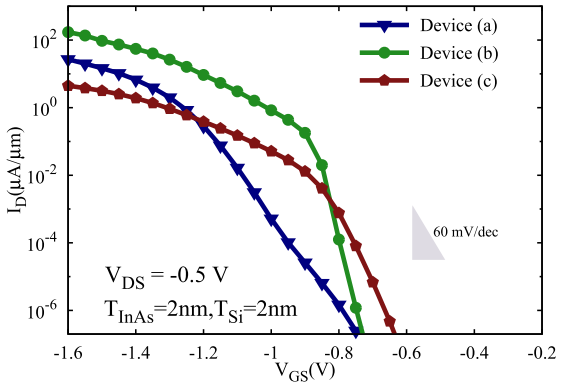

Fig. 4. Room-temperature I_D–V_{GS} characteristics of InAs–Si 2D–2D pTFETs at $V_{DS} = -0.5$ V for devices (a)–(c). The thicknesses are $T_{InAs} = T_{Si} = 2$ nm in all cases.

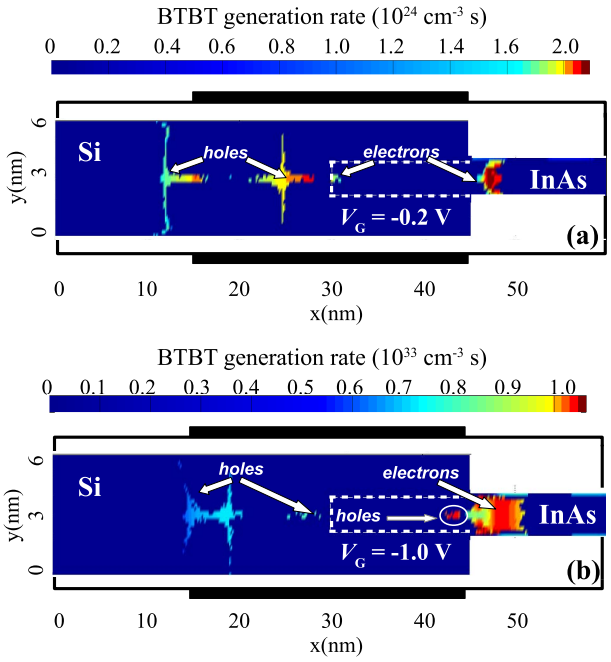

Fig. 5. Device (b): BTBT generation rate of an extremely thin InAs–Si 2D–2D pTFET with $T_{InAs} = T_{Si} = 2$ nm at (a) $V_{GS} = -0.2$ V and (b) $V_{GS} = -1$ V. The source–drain bias is $V_{DS} = -1$ V.

the impact and the contribution of lateral and vertical tunneling components. For instance, at the lowest gate voltages, the difference between the currents is around two orders of magnitude. The current of the device (b) is much higher due to lateral intermaterial tunneling components, which are not present in the device (c) when both InAs and Si layers are extremely thin, i.e., $T_{InAs} = T_{Si} = 2$ nm. However, they have in common their steep slope as the result of the compromise between the energy gap (E_g) in InAs and the 2D–2D feature of the devices.

The lateral intermaterial tunneling paths can be better observed in Fig. 5 where the BTBT generation rates of an extremely thin InAs–Si 2D–2D pTFET with $T_{InAs} = T_{Si} = 2$ nm at $V_{GS} = -0.2$ V (OFF-state) and $V_{GS} = -1$ V (ON-state) are plotted for a higher source–drain

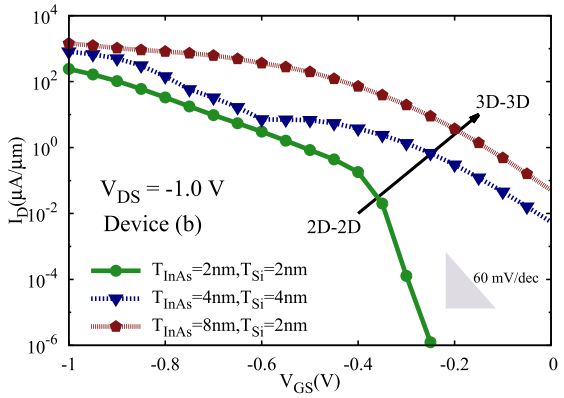

Fig. 6. Device (b): room-temperature I_D–V_{GS} characteristics of InAs–Si 2D–2D pTFETs with $V_{DS} = -1$ V.

bias $V_{DS} = -1$ V. Similar results are expected for lower V_{DS}, e.g., $V_{DS} = -0.5$ V. In a postprocessing step, the converged potential from OMEN is used as input for the computation of the BTBT generation rate. Observe that in the ON-state of the 2D–2D InAs–Si TFET in Fig. 5(b), there is an additional lateral tunneling component due to hole generation inside the InAs region boosting the current to higher values. In Fig. 5(a), only tunneling from Si to InAs can be identified in the OFF-state. For the latter, the material parameters have been extracted from full-band structures at source and drain computed with OMEN. For a Si QW with $T_{Si} = 6$ nm, the light-hole (m_v) and electron (m_c) effective masses, that fit the parabolic curvature of band edges, and energy gap are, respectively, $m_v = 0.147\,m_0$ and $E_g = 1.37$ eV. For an InAs QW with $T_{InAs} = 2$ nm, they are $m_v = 0.078\,m_0$, $m_c = 0.064\,m_0$, and $E_g = 0.93$ eV. The valence (conduction) band offset [$\Delta E_{v(c)}$], which is changed by geometrical confinement, was also extracted from the atomistic and full-band simulations: $\Delta E_v = 0.24$ eV ($\Delta E_c = 0.68$ eV). The band offsets are obtained as the energy difference of the highest valence (lowest conduction) subbands at the drain and source, i.e., $\Delta E_{v(c)} = E_{Dv(c)} - E_{Sv(c)}$, in ideal conditions without any external potential and doped regions. Since there is no consensus about the bulk value of the VB offset, we have arbitrarily varied ΔE_v in the range of 0.14–0.34 eV. However, no significant qualitative and quantitative changes in the I_D–V_{GS} characteristics were observed. For instance, if $\Delta E_v = 0.34$ eV, the ON-current is 6.4% higher than in the case of $\Delta E_v = 0.24$ eV, with a slightly smaller SS of 23 mV/decade. Therefore, the uncertainty in the bulk value of the valance band offset should not change the conclusions of this paper.

Another important feature to investigate is how sensitive 2D–2D TFETs are to a variation of their thickness.

Fig. 6 shows I_D–V_{GS} characteristics of device (b) with different thicknesses of InAs and Si: $T_{InAs} = T_{Si} = 2$ nm (circles), $T_{InAs} = T_{Si} = 4$ nm (triangles), and $T_{InAs} = 8$ nm, $T_{Si} = 2$ nm (pentagons). The thicker devices exhibit much higher ON-currents with the drawback of an increased SS. The maximum current they can reach is of the order of $10^3\,\mu$A/μm, while the SS is found to be 147 mV/decade for the device with $T_{InAs} = T_{Si} = 4$ nm

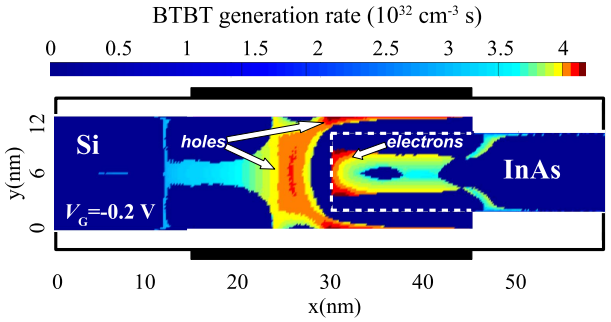

Fig. 7. Device (b): BTBT generation rate of an InAs–Si 2D–2D p-TFET with $T_{\mathrm{InAs}} = 8$ nm and $T_{\mathrm{Si}} = 2$ nm at $V_{\mathrm{GS}} = -0.2$ V and $V_{\mathrm{DS}} = -1$ V.

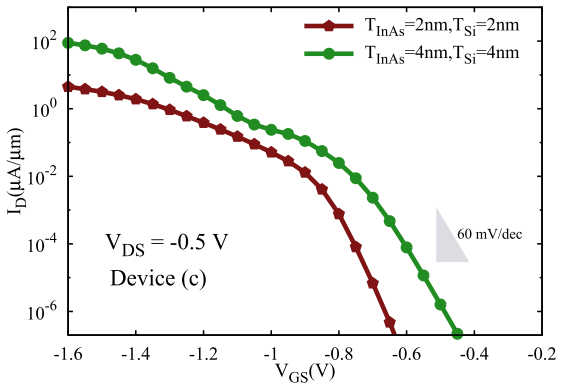

Fig. 8. Device (c): room-temperature I_{D}–V_{GS} characteristics of InAs–Si 2D–2D pTFETs at $V_{\mathrm{DS}} = -0.5$ V for $T_{\mathrm{InAs}} = T_{\mathrm{Si}} = 2$ nm and $T_{\mathrm{InAs}} = T_{\mathrm{Si}} = 4$ nm.

and 131 mV/decade for the device with $T_{\mathrm{InAs}} = 8$ nm and $T_{\mathrm{Si}} = 2$ nm. Fig. 6 also shows that by increasing the size of the device the advantages of 2D–2D TFETs vanish. In fact, the thicker the device, the more it behaves like a 3D–3D TFET. Thus, the subthreshold slopes should become less steep as reported earlier.

In order to better understand why the current within the subthreshold regime is much higher in the case of "the most 3D–3D-like DOS switch," the BTBT generation rate at $V_{\mathrm{GS}} = -0.2$ V is shown in Fig. 7. The material parameters were also extracted from full-band structures computed with OMEN. For a Si QW with $T_{\mathrm{Si}} = 12$ nm, the effective mass and the effective energy gap, are, respectively, $m_v = 0.147\, m_0$ and $E_g = 1.34$ eV. For an InAs QW with $T_{\mathrm{InAs}} = 8$ nm they are $m_v = 0.061\, m_0$, $m_c = 0.04\, m_0$, and $E_g = 0.58$ eV. The VB and CB offsets are $\Delta E_v = 0.23$ eV and $\Delta E_c = 1$ eV, respectively. As can be observed, both intermaterial tunneling components (point and line tunneling) are present, the first one being dominant and also the cause for the strong leakage current. This parasitic effect is reduced in the architecture of device (c) where the lateral tunneling components at the center of device (b) are blocked, or eliminated, by replacing part of the Si region by an oxide layer.

Fig. 8 shows the I_{D}–V_{GS} characteristics of device (c) for $T_{\mathrm{InAs}} = T_{\mathrm{Si}} = 4$ nm (circles) and $T_{\mathrm{InAs}} = T_{\mathrm{Si}} = 2$ nm (pentagons). Due to the lower energy gap, the thicker device presents a higher ON-current, but unlike device (b), the leakage intermaterial lateral tunneling has vanished. As a consequence,

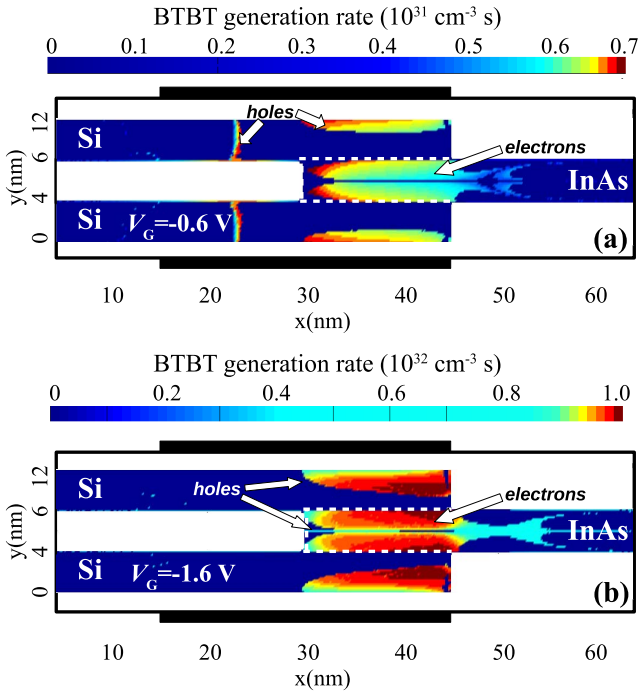

Fig. 9. Device (c): BTBT generation rate of an InAs–Si 2D–2D pTFET with $T_{\mathrm{InAs}} = T_{\mathrm{Si}} = 4$ nm at (a) $V_{\mathrm{GS}} = -0.6$ V and (b) $V_{\mathrm{GS}} = -1.6$ V. The source–drain bias is $V_{\mathrm{DS}} = -0.5$ V.

SS = 54 mV/decade is comparable with its counterpart SS = 36 mV/decade of the thinner device with the advantage of performing better (higher ON-current and lower onset voltage). The subthermal slopes are due to the fact that in these devices, only the line (or vertical) tunneling components occur in the subthreshold regime. This can be better observed in Fig. 9(a), where the BTBT generation rate is plotted for the thicker device (c) at $V_{\mathrm{GS}} = -0.6$ V and $V_{\mathrm{DS}} = -0.5$ V. Here, only intermaterial line tunneling takes place and no point tunneling component can be seen. Using OMEN for the full-band structures, the following parameters were extracted: $m_v = 0.147\, m_0$ and $E_g = 1.34$ eV for Si, and $m_v = 0.0656\, m_0$, $m_c = 0.048\, m_0$ and $E_g = 0.68$ eV for InAs. The VB offset is $\Delta E_v = 0.23$ eV, whereas the CB offset is $\Delta E_c = 0.93$ eV.

Fig. 9(b) shows the BTBT generation rate in the ON-state of the thicker device (c). At first glance, it looks very similar to the BTBT generation rate at the OFF-state. However, besides that the BTBT generation is higher, there is an additional hole generation region highly localized at the center of the InAs QW under the gate. The generated holes are due to intramaterial lateral tunneling components that appear in the ON-state of the device. As shown in Fig. 8, these new lateral tunneling components beneficially impact the current causing a second saturation regime, for $V_{\mathrm{GS}} < -1$ V, that reaches a higher ON-current up to $10^2\,\mu$A/μm. One can then conclude that for a higher ON-current, both lateral and vertical tunneling paths are necessary.

IV. Conclusion

Double-gate TFETs exploiting the 2D–2D DOS switch with different architectures have been simulated employing

a full-band and atomistic quantum transport solver. First, an InGaAs electron–hole bilayer TFET was compared with its lateral TFET counterpart. We found that lateral tunneling components are detrimental to a high performance of the bilayer TFET. Then, in order to exploit both lateral and vertical tunneling paths, we have investigated different geometries of an InAs–Si 2D–2D TFET.

In the best case, the I_D–V_{GS} characteristics exhibit a very steep minimum slope, $SS = 28$ mV/decade, with a reasonably high ON-current of 240 μA/μm. The latter is due to an additional intramaterial BTBT component in the InAs region that boosts the ON-current. Thicker versions of 2D–2D TFETs could provide much higher ON-currents, but their corresponding SS will degrade. This is caused by the leakage current due to lateral intermaterial tunneling, which decreases with shrinking width of the 2D–2D TFET. Therefore, a compromise between tunnel gap and 2D–2D nature of the heterostructure has to be found. By increasing the thickness, the advantages of 2D–2D TFETs vanish, since the device is getting closer to a 3D–3D TFET.

APPENDIX

A. Flietner Imaginary Dispersion

Within two-band analytical models, the Flietner model [14] describes the imaginary band structure of small-gap materials with high accuracy. In the Flietner model, the imaginary dispersion has the following form:

$$\frac{\hbar^2\kappa_x^2}{2m_c} = E\left(1-\frac{E}{E_g}\right)\left[1-\alpha+\alpha\left(\frac{E}{E_g}-1\right)\right]^{-2} + E_{c,\mathbf{k}_\perp} \tag{1}$$

$$= \frac{\hbar^2\kappa^2}{2m_c} + \frac{\hbar^2\mathbf{k}_\perp^2}{2m_c}. \tag{2}$$

Here, $E_{c(v),\mathbf{k}_\perp} = \hbar^2\mathbf{k}_\perp^2/2m_{c(v)}$ is the electron (hole) energy related to each transverse mode $\mathbf{k}_\perp$ with effective mass $m_{c(v)}$. For sake of convenience, the VB and CB edges are set to $E_v = 0$ and $E_c = E_g$, respectively. In (1), $\alpha = 1-\sqrt{m_c/m_v}$, whereas in (2)

$$\kappa = \sqrt{\frac{2m_c}{\hbar^2}}\sqrt{E\left(1-\frac{E}{E_g}\right)}\left[1-\alpha+\alpha\left(\frac{E}{E_g}-1\right)\right]^{-1}. \tag{3}$$

The Flietner model can be extended to the case of intermaterial tunneling processes by treating the effective masses and energy gaps as position-dependent quantities [10], i.e., $m \to m(x, y)$ and $E_g \to E_g(x, y)$, respectively.

B. Non-Local Path BTBT Model

Assuming that transport occurs only in the x-direction of a bulk-like semiconductor, the BTBT generation rate G can be obtained from the steady-state version of the continuity equation

$$\frac{\partial J}{\partial x} = eG(x) \tag{4}$$

where J is the current density, i.e., current per unit area, as a function of x. A relation with the tunneling probability T can be established when the Landauer formula

$$J = \frac{2e}{h}\int dE \int \frac{d\mathbf{k}_\perp}{4\pi^2} T(E,\mathbf{k}_\perp)(f_v(E)-f_c(E)) \tag{5}$$

is implemented to compute the current density. $\mathbf{k}_\perp$ is the wave vector related to the transverse modes, and $f_{c(v)}$ is the Fermi–Dirac distribution function for the conduction (valence) band.

Making the energy E position-dependent, (4) can be written as

$$\frac{dE}{dx}\frac{dJ}{dE} = eG(x) \tag{6}$$

from which an expression for G can be found by replacing (5)

$$G(x) = \frac{F(x)}{4\pi^3\hbar}\int d\mathbf{k}_\perp T(E(x),\mathbf{k}_\perp)(f_v(E(x))-f_c(E(x))) \tag{7}$$

$F(x) = dE/dx = dU/dx$ is the electric field due to the external potential $U(x)$. With the position-dependent energy $E(x) = E_{c(v)} + U(x)$, (7) can be used to compute the electron (hole) BTBT generation rate. The BTBT probability $T(E,\mathbf{k}_\perp)$ can be computed by means of the WKB approximation

$$T(E,\mathbf{k}_\perp) = e^{-2\int_{x_v}^{x_c} dx\,\kappa_x(x,E,\mathbf{k}_\perp)} \tag{8}$$

$$\approx e^{-2\int_{x_v}^{x_c} dx\,\kappa(x,E)} e^{-\mathbf{k}_\perp^2\int_{x_v}^{x_c} dx\,\kappa^{-1}(x,E)}. \tag{9}$$

The imaginary wave vector in the argument of the exponential in (8) has been expanded as $\kappa_x = (\kappa^2+\mathbf{k}_\perp^2)^{1/2} \approx \kappa + \mathbf{k}_\perp^2/2\kappa + \cdots$ to obtain (9). In ultrathin body or nanowire TFETs, the system is no longer 1-D. Then, the tunneling probability in (9) and the BTBT generation rate in (7) have to be computed in the direction of the electric field. Finally, by inserting (9) into (7), one can straightforwardly obtain the *non-local path BTBT model* formula used by the commercial device simulator S-Device [16].

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Authors' photographs and biographies not available at the time of publication.