Research Projects

IC and System Design and Test

Coordinator:

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The demand for smaller and cheaper products with ever more functionality asks for integration of large systems on a single chip. New technologies support this demand by drastically enhancing transistor density, but long development cycles for such systems contradict the hard requirement of short time-to-market. The key to resolve this contradiction is modular design, re-use of approved functional blocks, and the application of purchased virtual components. While the increase in area and operation speed already make clock distribution difficult, the multitude of clock frequencies and design strategies of the modular units prohibit any global clocking solution. The Globally-Asynchronous Locally-Synchronous design methodology (GALS) is a possible answer to the problem. It enables systems consisting of several independent modules, each of which has been designed independently, with available, well known methodologies and tools. GALS design encloses each module by a wrapper which handles the interfacing between synchronous islands in a self-timed manner. The local clocks are generated inside the wrappers, in a way to enable metastability-free data exchange between GALS modules.

In Globally-Asynchronous Locally-Synchronous (GALS) Systems the interfacing between a functional module and its self-timed environment is handled by the self-timed wrapper. A library of predesigned technology-independent elements simplifies the assembly of such wrappers. So far, wrappers for point-to-point connections can be generated almost automatically.

In many applications however, a shared system bus or other forms of multi-point data exchange are key components for modularly designed Systems-on-a-Chip (SoC). Different interconnection topologies are being considered to enhance the current GALS technique. Two versions are studied in more detail within this project:

The first one is a shared bus solution. It is realized by extending the port controllers that manage the self-timed data transfers between different GALS modules. The ability of proper arbitration for the shared bus resources is added in order to support multiple transmitters and receivers. Arbitration as well as address decoding are handled centrally for sake of area and power efficiency.

The second variant is a ring topology. All nodes are connected by a circular path. At each node local address decoders decide whether a received data word is allotted to the local synchronous module or whether it is to be passed on to the successor node. Dedicated self-timed GALS ring transceivers are developed which are able to decouple the synchronous island from the ring’s timing.
Testability of Globally-Asynchronous Locally-Synchronous Wrapper Modules

Personnel: Frank Gürkaynak

Funding: KTI-4897.1 IRRQ, Philips Zurich

Partners: Philips Zurich

Globally-Asynchronous Locally-Synchronous (GALS) architectures have the potential to overcome clock distribution and synchronization problems associated with the design of large Systems on a Chip (SoC). This project addresses the testability problem of GALS-based systems which has not been solved so far.

A new functional test methodology has been developed to provide testability for the GALS system. In this methodology, each GALS module is augmented by a test extension element, that allows a centralized test controller to access the GALS module. The test controller can activate individual data transfer channels between GALS modules. Testing is achieved by observing correct data transfers between GALS modules.

This methodology calls for customized test extension elements for all GALS modules within a system. This is achieved by a design and test automation script that automatically generates all test related hardware and assembles the entire GALS system.

Clock Generators for Globally-Asynchronous Locally-Synchronous Wrapper Modules

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Funding: KTI-4897.1 IRRQ, Philips Zurich, Infineon

Partners: Philips Zurich, Infineon

One of the major advantages of Globally-Asynchronous Locally Synchronous (GALS) systems is the reduction of power consumption by avoiding the global clock tree, which can be responsible for dissipating up to 30 per cent of the chip’s total power consumption. While the pausable ring oscillator used in our first GALS designs certainly met the requirements of low power dissipation, it could not fulfill the expectations on frequency resolution which is necessary to get optimum performance.

In this project, a test chip has been developed which contains 24 different oscillator architectures. The oscillators consist of standard cells routinely available in any standard cell library. Some newly developed standard cells are applied too. The implemented variants are designed to achieve sub gate-delay resolution. They include delay-banks of tristatable inverters, cascaded phase blender circuits, digitally controlled capacitive loads, and several delay slice alternatives. The oscillators can be configured individually either over an RS232 interface or directly through multiplexed pins. In conjunction with an FPGA this chip can therefore be used to develop adaptive delay adjustment strategies based on reference clocks and PLLs. The picture shows a simulation of a cascaded phase blender, considering the interconnect capacities.
Multimedia Network Chips

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Funding: KTI-4957.2 LANWAN, BridgeCo

Partners: BridgeCo, TIK-ETHZ

Multimedia networks that transport real-time digital audio and video content require special network devices. This KTI project consists of several sub-projects investigating the problems of such network devices.

Two sub-projects focus on the problems of reference-time distribution over the network and clock recovery: To provide high-quality real-time transportation of audio and video data very precisely synchronized clock sources are indispensable. The problems of transporting time information over the network are investigated in the first, those of their application by means of low-cost, low-jitter clock generation circuits in the second sub-project.

The third topic concerns run-time reconfigurable hardware accelerator engines. They aim at providing high processing performance for decoding, encoding, encryption and signal processing. The hardware accelerator consists of several small signal processors with adaptable instruction sets. Each processor contains reconfigurable hardware structures and is retargetable to a specific task at run-time.

In the fourth sub-project the software development environment for complex multimedia network devices with host CPU and reconfigurable hardware accelerators is developed. The problems of integrating a host CPU and reconfigurable hardware accelerators in one user-friendly programming environment are investigated.

Reconfigurable Hardware Accelerator for Real-time Multimedia Data Processing

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Funding: KTI-4957.2 LANWAN, BridgeCo

Partners: BridgeCo, TIK-ETHZ

Multimedia data processing devices have to deal with high data bandwidth and processing-intensive tasks like decompression, compression, ciphering and signal processing. This requires dedicated high-performance ASICs. At the same time the huge amount of different and changing algorithms, the high development risk and high cost of dedicated chip designs ask for programmable solutions.

In this project run-time reconfigurable hardware accelerators together with a general purpose host-CPU are foreseen to provide superior performance and flexibility for multimedia network devices. The host CPU is used to run the operating system, to control the dataflow, and to configure the accelerators. The hardware accelerators operate on the data streams and deliver the required signal processing performance.

The hardware accelerator consists of several small reconfigurable signal processors with dynamically reconfigurable instruction sets. Each processor can be reconfigured at run-time and optimized for a specific task by adding new specialized instructions to the basic instruction set. A reconfigurable hardware mesh within the processor performs operations previously defined and configured by the programmer. A high-bandwidth shared memory is used to buffer the data streams and to interconnect the processors and the on-chip bus.

![Multimedia Network](image1)

![Host-CPU and reconfigurable hardware accelerators on a System-on-Chip](image2)
Synchronization of an IEEE-1394 Network for Audio and Video

Personnel: Eric Roth
BridgeCo: Georg Dickman

Funding: KTI-4957.2 LANWAN, BridgeCo
Partners: BridgeCo, TIK-ETHZ

Its Quality-of-Service capabilities has established the IEEE-1394 bus (FireWire™) as the superior technology for multimedia content transportation. In order to stream audio data, data rates at the sending nodes and the receiving nodes must be aligned to prevent buffer overflows and underflows. The goal of this project is to investigate and develop synchronization methods that align phase and frequency of all sample clocks on the network.

Timing information is broadcast through the IEEE-1394 network such that bus nodes can adjust their sampling rates to a common reference. Variable transmission latency of timing packets causes jitter that must be removed before timing information can be used as audio clock. Several approaches have been analyzed for different network configurations with respect to time accuracy, jitter performance, and reliability.

To analyze the problems and verify the feasibility a very flexible clock recovery circuit has been realized. It draws the precision from a quartz oscillator and uses a (so far partially) on-chip phase-locked loop to re-generate the high-quality audio clock.

All-Digital Standardcell-Based PLL for Audio and Video

Personnel: Eric Roth

Funding: KTI-4957.2 LANWAN, BridgeCo
Partners: BridgeCo, TIK-ETHZ

The growing popularity of digital multimedia consumer equipment such as video cameras, DVD players, and Hi-Fi systems increases the demand for an interconnectivity network between these devices. Distribution of real-time multimedia data over such a network requires alignment of data rates at the sending and receiving nodes in order to prevent data losses due to buffer overflows and underflows.

Phase-locked loops (PLL) are commonly used to synchronize phase and frequency of clocks to a reference clock. Classical PLLs deploy an analog VCO that often cannot be integrated on standard digital CMOS ASICs. The goal of this project is the development of a digital PLL that has a jitter performance comparable to the analog counterpart and that consists exclusively of standard cell library elements available in any digital CMOS technology.

The most critical element of a digital PLL is the digitally controlled oscillator DCO. A new DCO principle has been developed to gain high frequency resolution and low jitter. The edges of a fixed-frequency input clock are constantly shifted using a digitally controlled delay line. The amount of the phase shift defines the frequency offset of the output clock relative to the input clock.

Typical IEEE-1394 network application with transmission of audio data (top) and jitter of timing packets (bottom) when transmitted through the network.

Circuit diagram of digital PLL (top) and principle of developed DCO (bottom).
Mobile Communication is gaining importance in today's societies, markets, as well as in the research community. To meet the new requirements posed by future multimedia telecommunication services, data rates need to be increased. Since the radio bandwidth available remains constant while the number of users is ever increasing, the network capacity must be enhanced.

Exploring space- and time diversity allows to develop new algorithms to optimize the data rate and estimate the current channel quality between the transmitter and receiver. One major field to investigate are MIMO (Multiple Input Multiple Output) techniques, which allow to increase the data rates drastically while truly enhancing the capacity of wireless networks. These systems are characterized by multiple antennas on both the receiver and transmitter side. The goal is to develop and demonstrate a working real-time prototype of a MIMO system based on the UMTS standardization framework.

The basic modulation techniques investigated are CDMA (Code Division Multiple Access) as used for UMTS, as well as OFDM (Orthogonal Frequency Division Multiplexing) as a possible candidate for fourth generation mobile telecommunication systems.

Investigations are focused on VLSI feasibility. The research is conducted in collaboration with partners outside as well as inside the ETH. IIS’ first experiences with adaptive receiver antenna arrays stem from a project that resulted in an efficient architecture well suitable for ASIC implementations (see page 49 left).

The upcoming Universal Mobile Telecommunications Standard (UMTS) is the first step towards truly mobile multimedia communication. However the latest studies show that it will not provide enough capacity to support high-bandwidth applications for a large number of users in real environments. Spatial multiplexing is a new technique that uses multiple antennas at both the transmitter and receiver to directly increase data rates in rich scattering environments. This technique is often referred to as MIMO (Multiple Input/Multiple Output).

In this project which is a collaboration with the Lucent/Bell-Labs Wireless Research group in New Jersey (USA), MIMO concepts have been integrated into the UMTS downlink. In a first step the necessary modifications to the UMTS standard were investigated and simulations were carried out for initial performance assessments. These showed promising results, giving raise to the hope that the theoretically predicted gains could actually be realized. In the next phase of the project a prototype of such a system was developed. It consists of an RF frontend, a digital multi-antenna receiver frontend and the MIMO decoder. The latter two parts were realized on FPGAs and DSPs. The implementation uses four antennas at the transmitter and at the receiver side. This configuration is theoretically able to increase the throughput by a factor of four compared to a standard UMTS downlink with a single transmit and receive antenna.

The main project parts of IIS were the realization and optimization of the complete receiver frontend and contributions to the optimization of the MIMO decoder for real-time operation. The system has been completed and is currently being used for real-time measurements under real-world conditions.
IP Core for Real-Time Solution of Least Squares Problems using CORDIC and QRD-RLS

Personnel: Boris Glass

Funding: ETHZ

Partners: Ascom

A frequent problem in science and engineering is to fit a theoretical model to observations that suffer from errors. The Least Squares Method is the most common approach to an optimal solution. Mathematicians investigated the problem for over 200 years. Nowadays image processing, robotics or communications are demanding real-time solution of least squares problems.

The combination of QR (triangular) Decomposition and Recursive Least Squares computation is known as the QRD-RLS algorithm. It is robust and effective. And it is well suited for an efficient VLSI implementation based on a systolic array of CORDIC processors.

The developed CORDIC processor array is reusable as Virtual Component (VC) in other applications since it is largely scalable. A graphical user interface has been developed to easily handle all parameters during design: Transformations from fully parallel to fully sequential processing can be selected for one or several cascadable chips. This enables customizations that closely meet the requested throughput with minimal area consumption. A preview shows the resulting architecture as well as the arrays’ overall area. Finally, the systolic CORDIC array can be exported as Matlab and VHDL source.

Lower Bounds on Power Dissipation in Digital VLSI

Personnel: Jürgen Wassner

Funding: KTI-5025.1 DSP, Bernafon

Partners: Bernafon

With ongoing advances of semiconductor technology, power dissipation has been moving higher on the list of VLSI design constraints. Today it is at or near the top of this list, notably for ICs in portable equipment where battery lifetime is of major concern.

An compelling question arising in this context is the existence of an absolute lower bound on power dissipation. Besides its theoretical significance such a lower bound would also provide useful guidance for practical low-power design. Knowing the minimum dissipation achievable for certain operations would allow to rate the energy efficiency of state-of-the-art implementations for these operations. Implementations with poor energy efficiency should then be prime candidates for future optimization efforts.

To tackle the lower bound problem, a systematic view of minimum power dissipation in consideration of data statistics has been developed, which culminates in a classification of this problem. The lower bound for data transmission is directly related to the minimum switching activity achievable by proper encoding, and, can be given analytically using information-theoretic arguments (see figure). On the other hand, it has been shown that a useful lower bound on the dissipation of an arbitrary data processing task can not be derived without knowledge of its optimal implementation, which in general is unknown. In this case, existing information-theoretic bounds do not provide adequate means for solving the problem of a lower bound on power dissipation.

Illustration of the QR Decomposition (top), graphical user interface of the systolic array generator (middle), a graph representation of the scheduling and binding problem (bottom), and a chip photograph in the background.
Control of Combined Parallel/ Series-Connected IGBTs

Personnel: Jan Thalheim

Funding: ETHZ, KTI-3367.1 SIGU

Partners: CONCEPT

For high-voltage high-current power converters, it may be necessary to realize a switch by connecting smaller devices in parallel and series. Beyond higher voltage and current capability, this approach also helps to achieve high availability, high-frequency operation, and low cost due to built-in redundancy, reduced dynamic losses, and the use of modular standardized units. Insulated Gate Bipolar Transistors (IGBTs) are very convenient to realize such units because of their quasi-linear controllability via a gate terminal.

In this project it has been proposed to provide each IGBT driver with a primary local control which is monitoring and adjusting the IGBT’s static and dynamic behavior. Secondary control is then realized to synchronize the operation of multiple IGBTs. The discovery of a globally synchronous signal, that can be derived locally, makes it possible to use low-cost low-bandwidth data links between series-connected units. Furthermore, a flexible master-slave approach can avoid the need of a dedicated global controller. That is, the entire system becomes manageable by the local gate drive circuitry.

A prototype ASIC has been fabricated in CMOS technology with high-voltage extension. The gate driver is partitioned into fourteen clusters with a measured gate current capability of 1A each. It allows for real-time reconfiguration of the structure to optimize the dynamic response of the system.

ASIC for dynamic control of series-connected IGBTs.