

# RESEARCH PROJECTS

## IC and System Design and Test

Coordinator:

**Norbert Felber**

## ITRASYS STM-1 Multiplexer: Realization of Complex Systems On a Chip

**Personnel:** Markus Thalmann (Siemens Schweiz);  
Manfred Stadler, Thomas Röwer

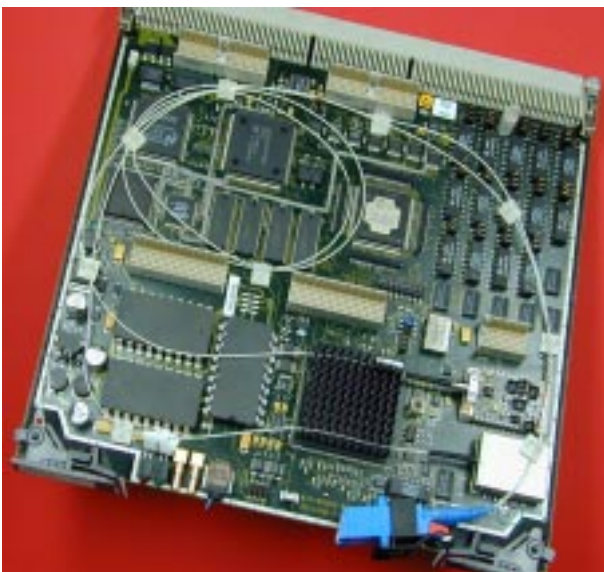
**Funding:** ETHZ, KTI-3297.2 ITRASYS,  
Siemens Schweiz

**Partners:** Siemens Schweiz

ITRASYS is an ultra-compact Add/Drop multiplexer for digital telecommunication networks. Beside the system controller (top left on the lower picture) all digital components are integrated in one very large ASIC (bottom middle on lower picture).

This ASIC houses the complete data-path of the network node including the switch matrix and an "Application-Specific Instruction set Processor" (ASIP).

The ASIP is used to compute many complex but slow tasks which formerly required dedicated hardware. This approach saves silicon, adds flexibility to the product, and allows concurrent engineering of ASIC and firmware.



Bottom: ITRASYS printed circuit board featuring the main ASIC, the optical interface, and 21 ISDN primary surge protections. Top: Daughter board with additional 42 surge protections.

## Intellectual Property Module of a Highly Parametrizable Embedded Stack Processor

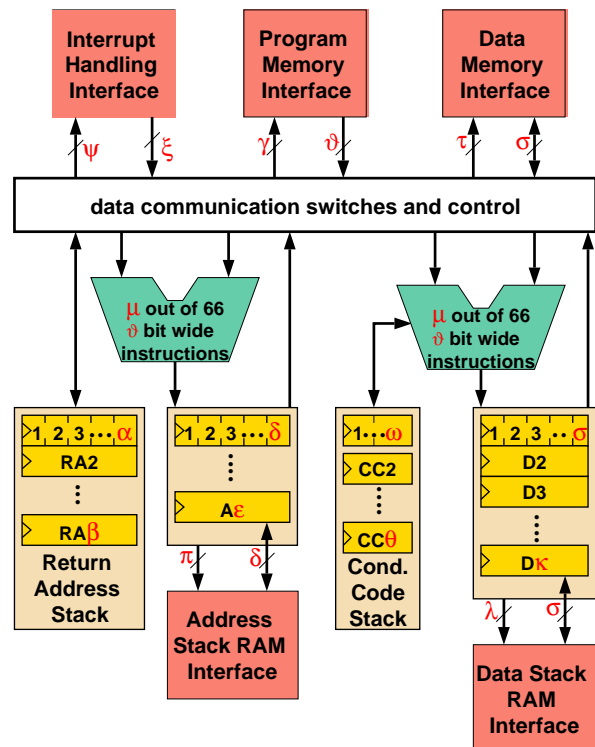
**Personnel:** Thomas Röwer, Manfred Stadler;  
Markus Thalmann (Siemens Schweiz)

**Personnel:** ETHZ, KTI-3297.2 ITRASYS,  
Siemens Schweiz

**Partners:** Siemens Schweiz

Customizable microprocessors pose numerous design problems that arise from application-specific needs for data operations, word widths, storage capacities, and interfaces. A stack processor that features a customizable instruction set, extensive parameterization, and a synthesis model with separate core and interface modules has been designed in this work. It can be tuned to the application-specific needs of the user by means of 100 parameters.

Application- or customer-specific scalability and programmability, however, introduce severe difficulties into the functional verification flow. For this IP a two-step functional verification flow has been developed. In the first step a configuration-independent behavioral model is applied to generate the test pattern using assembler code as stimuli. In the second simulation run the expected responses, generated by the behavioral model, are compared against the output of the parameterized RTL model of the IP module, and a report is generated.



Application-Specific Instruction set Processor (ASIP) IP module with customizable parameters shown as Greek letters.

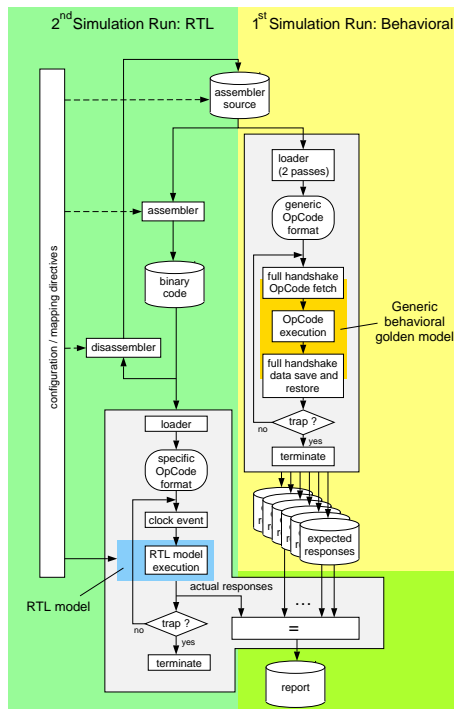
# Functional Verification of Virtual Components: a Simulation-Based Method for an ASIP

**Personnel:** Manfred Stadler, Thomas Roewer; Markus Thalmann (Siemens Schweiz)

**Funding:** ETHZ, KTI-3297.2 ITRASYS, Siemens Schweiz

**Partners:** Siemens Schweiz

Scalability and customization properties of Virtual Components (VC) demand new solutions in functional verification. A novel simulation-based approach for an Application-Specific Instruction-set Processor (ASIP) is introduced. Existing assembler code, preselected by VC-configurable constraints, forms the verification data base (reference stimuli). A behavioral "golden model" of the VC is used to derive expected responses suitable for any possible configuration of the final ASIP (RTL) implementation. Cycle-based verification is performed by stimulating the RTL model with the assembled reference stimuli and by comparing the outputs (actual responses) against the expected responses. Primary input stimulation is accomplished by reading back interface data prior written to a memory (model) under control of the reference stimuli. The synchronization of the configuration-dependent actual responses to the non-cycle-related expected responses is achieved by a mechanism based on "interface-specific activity scheduling", which further more reduces the number of vectors efficiently, resulting in a significant simulation speed-up.



Flow of the ASIP Virtual Component verification.

# ADAMO — ADaptive Antenna for MOBiles: Adaptive Antenna Training Engine

**Personnel:** Boris Glass, Bruno Haller

**Funding:** ESPRIT-27001 ADAMO, BBW

**Partners:** Ascom, ENSTA, IMST, Thomson

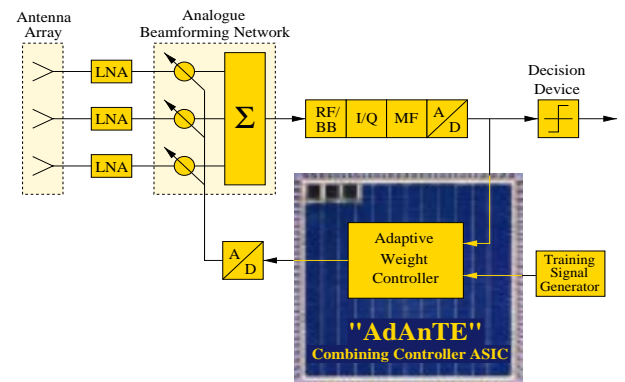
The objective of the ADAMO project is to validate the potential of small, low-cost adaptive antennas for HIPERLAN (= ESTI standard for wireless LANs) modems. Improvement of performance and reduction of power consumption are the expected benefits of adaptability.

Instead of using a complex, high-speed (47 Msample/s) adaptive equalizer (= digital transversal filter) to mitigate the detrimental effects of intersymbol interference caused by multipath propagation, spatial filtering is applied by appropriately weighting and combining the RF signals from three independent antennas.

This "beam-forming network" realized with analog phase shifters and amplifiers consumes considerably reduced power compared to a digital equalizer-based solution.

IIS' contribution is the implementation of the digital signal processing algorithm for the computation of the combiner coefficients of the adaptive antenna. A dedicated ASIC - the AdAnTE chip - has been designed. Due to the fact that this processor is only active to compute the new weights during the training header of each data packet, and is set idle when actual information is transmitted, the average current consumption is minimal despite the instantaneous high-speed digital switching activity of the 780,000 transistors.

The 7 by 7 mm<sup>2</sup> chip calculates the set of coefficients on a linear systolic array of pipelined CORDIC (COordinate Rotation Digital Computer) processor elements in less than one microsecond.



Block diagram of an adaptive antenna with RF beam-forming network and digital weight controller ASIC AdAnTE.

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## Compact High-Resolution One-CCD Camera with High Color Fidelity

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**Personnel:** Daniel Doswald, Jürgen Hertle; Jürg Häfliger (IBT), Yves Lehareinger (IBT)

**Funding:** MINAST 5.01 EIM, ETHZ

**Partners:** IBT-ETHZ, Volpi

Medical minimally invasive video applications require hand-held endoscopes with integrated video camera. To satisfy the ergonomic requirements of such an instrument small camera head dimensions are imperative. This requirement can only be fulfilled with a single CCD sensor with color filter array (CFA). Non the less the color fidelity should approximate the quality of a 3-CCD camera and still give better resolution.

The solution is to split the camera into a head containing all sensitive electronics, and into the back-end which performs the power consuming processing. The transmission of the image data occurs in insensitive digital format at high speed.

The task of the camera is to reconstruct the "true RGB" image with best possible resolution and color fidelity. Due to a highly integrated custom ASIC (see following contributions) all components of the back-end fit on a short PCI card.



Miniaturized head of the 1-Megapixel CCD video camera. In the background: PCI card containing the image signal processor ASIC (open package), an FPGA with PCI interface, and SD RAMs for intermediate storage.

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## ZATHRAS - Programmable CCD Pulse Generator with On-Chip 400Mbit/s Transmitter

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**Personnel:** Daniel Doswald

**Funding:** MINAST 5.01 EIM

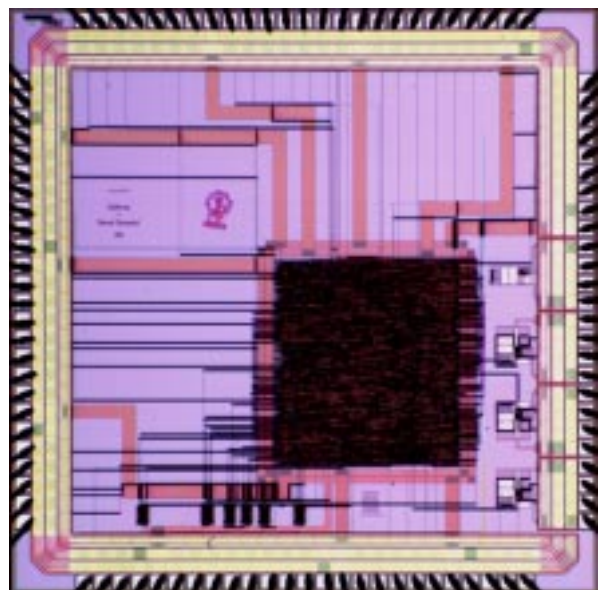
**Partners:** IBT-ETHZ, Volpi

For the miniaturized high-resolution CCD camera a chip set has been developed by the Integrated Systems Laboratory. ZATHRAS is one of the ASICs for the camera head. It contains a clock receiver, a CCD pulse generator, a parameter link interface, and a high-speed image data transmitter.

The ZATHRAS ASIC is a configurable, fully digital pulse generator with an on-chip 400 Mbit/s image data transmitter for use with a Kodak KAI-1010 series CCD image sensor and two CCD signal digitizers (either Burr-Brown VSP2101, Exar XRD98L60 or Analog Devices AD9803). Through the additional off-chip driver stages, the ASIC supplies the signals required for correct operation of the sensor. Furthermore ZATHRAS generates all necessary control signals for the CCD signal digitizers. Over a parameter link all registers of the camera head can be configured and the auto focus can be actively controlled.

### *Chip data and measured characteristics:*

Technology	CMOS 0.35 $\mu$ m
Clock frequency	100 or 200 MHz
Supply voltage	3 V
Current consumption @ 3 V supply	33.6 mA
Core size	1.6 x 1.6 mm <sup>2</sup>
Die size	3.5 x 3.5 mm <sup>2</sup>
Programmable-delay step	501 to 512 ps



Die microphotograph of the ZATHRAS ASIC.

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## LEELOO - A Megapixel 30 Frames/s Real-Time CMOS Image Processor

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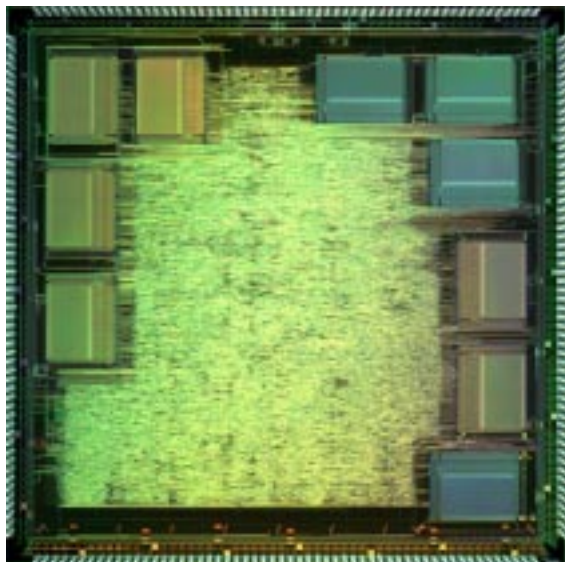
**Personnel:** Daniel Doswald;  
Balz Schreier, Stephan Oetiker  
(students)

**Funding:** MINAST 5.01 EIM, ETHZ

**Partners:** IBT-ETHZ, Volpi

Real-time motion pictures providing image quality superior to standard video in terms of resolution and color fidelity are often required. In many applications, e.g. in biomedicine or machine vision, only cameras with a single charge-coupled device (CCD) sensor can satisfy the stringent space requirements. The reconstruction of the RGB image from the CCD with a Bayer color filter array requires an extremely high computation effort if reasonable frame rates and artefact-free interpolation quality is to be achieved.

The LEELOO ASIC performs this task for 1024 by 1024 pixel images at 30 frames per second. The raw image data from the camera head is received by on-chip low-voltage differential signaling receivers. Prior to interpolation, this data is processed by a pixelwise black-current and white-gain balancing. The interpolation algorithm is based on complex algorithms over nine CCD lines which are stored on-chip. To achieve best color fidelity with different scene illuminations, a 6x3 matrix transformation is performed on the interpolated RGB data for color space adjustment. Additional highlights of the ASIC are scan conversion for a PAL video encoder and two-dimensional focus criterion calculation on a sizable window. Two synchronous DRAM controllers enable cost-efficient intermediate data storage and the hardware-assisted parallel interface provides easy configuration access to all units.



Die micrograph of the LEELOO image processor.

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## Video Scan Converter for High- Resolution CCD Camera

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**Personnel:** Oliver Pfister, Giorgio Weston (students);  
Norbert Felber, Daniel Doswald

**Funding:** ETHZ

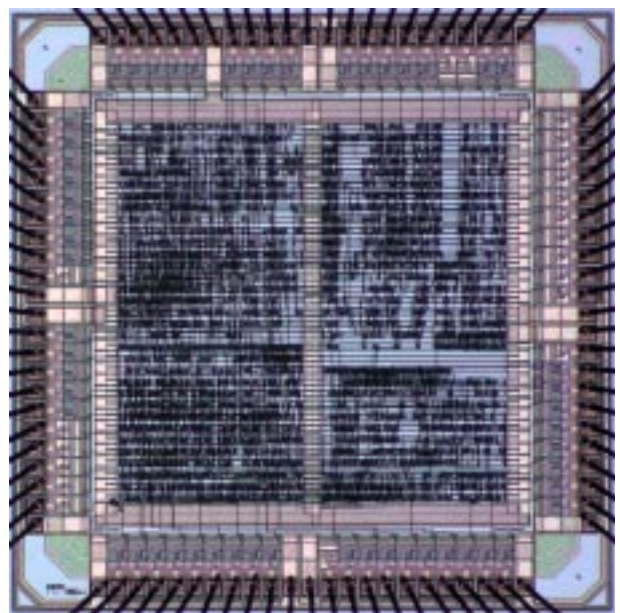
**Partners:** IBT-ETHZ, Volpi

The CCD video camera for medical minimally invasive operation (compare previous projects) delivers excellent video pictures. However, documentation of operation sessions on video tape and distribution to remote rooms with video equipment is a problem. A standard video output for these purposes is a highly desirable feature of the camera system. Due to different resolution and frame timing, scan conversion is required.

The scan converter algorithm has been implemented by two 7th semester VLSI students (for other student projects see chapter "Education Program"). The task of this algorithm is resolution reduction, intermediate frame storage, pixel frequency adaptation, even/odd field generation, and interfacing to a Harris video encoder IC HMP8156A.

The main challenges to solve were the large amount of data storage and the totally asynchronous frequencies of the camera (40 Mpixels/s, 30 frames/s progressive scan) and the video encoder in PAL mode (14.7 Mpixels/s, 50 interlaced fields/s). Storage in a single external IC became possible with an SD Ram running at 100 MHz.

The design has been integrated as student chip and included into the LEELOO design (see previous page). It is fully functional and provides very good standard video images.



Micrograph of scan converter prototype ASIC.

# GALS Simplify Systems on Silicon

**Personnel:** Thomas Villiger, Jens Mutersbach

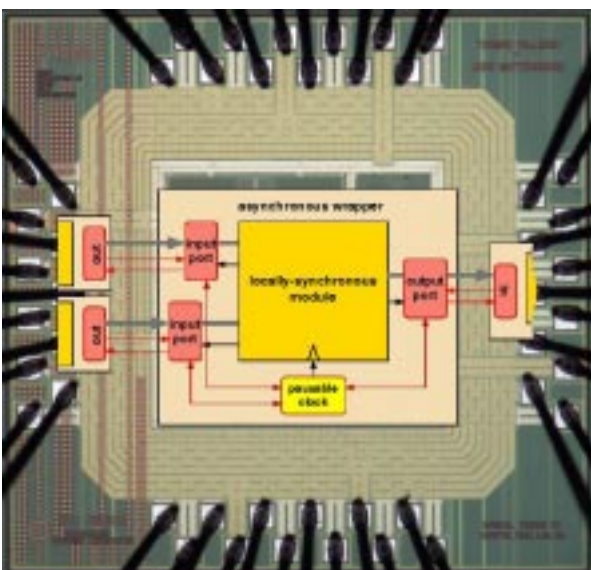
**Funding:** Infineon

**Partners:** Infineon

The technical progress in CMOS technologies, increase in available die size, and the demand for short time-to-market ask for integration of large systems on a single chip. Higher clock frequency and larger area make proper clock distribution difficult. Complex systems often require a multitude of clocks on a common die, therefore asking for reliable synchronizers between independent clock domains.

A Globally Asynchronous Locally Synchronous (GALS) design methodology facilitates clocking of large systems on silicon as it partitions a system into several independently clocked modules which communicate in self-timed fashion. Every synchronous module is surrounded by a so-called asynchronous wrapper that manages all the data transfers. The actual functionality remains unchanged inside the locally synchronous blocks, such that well established design flows can be used. The local clocks are generated within the wrappers and are stopped when there is no data to process in the synchronous block. The partitioning into modules results in enhanced modularity and reusability, and the decoupled timing constraints between modules leave more options for optimization.

FANGO, a cipher chip performing the SAFER-K64 algorithm has been implemented to validate the feasibility of GALS.



Block diagram of an asynchronous wrapper overlaid on the microphotograph of the FANGO chip.

# A Design Flow for Globally Asynchronous Locally Synchronous Systems

**Personnel:** Jens Mutersbach, Thomas Villiger

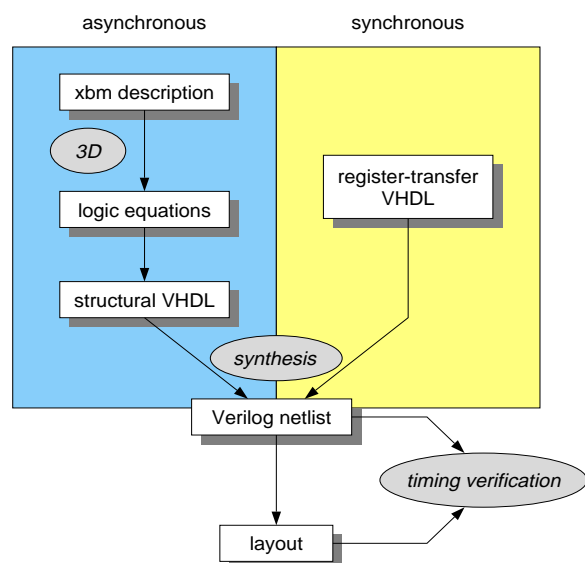
**Funding:** ETHZ, KTI-3650.1 DSP, Philips

**Partners:** Philips

One of the key challenges in implementing a Globally-Asynchronous Locally-Synchronous (GALS) system is to integrate design methodologies and tools for both synchronous and asynchronous parts. The flow for the synchronous blocks is well established and tools are available.

Construction of asynchronous finite state machines starts with a graph-based extended burst mode (xbm) specification. This description was developed by Yun et al. and can be synthesized using the 3D tool set. The resulting set of equations gets translated into a structural VHDL description. At this stage other components (e.g. clock generation circuitry) can be added to the structural VHDL code. Subsequent synthesis requires careful distinction between structural descriptions whose topology must not be changed and behavioral descriptions that require extensive optimization.

Correct operation of asynchronous circuits and GALS systems depends on a number of timing conditions which need to be met. As available timing verification tools focus either on synchronous or asynchronous designs, much emphasis was put on the concept and establishment of a smooth timing verification routine.



Simplified design flow for GALS systems.

# Approximation of Signal Correlation for Probabilistic Power Estimation

**Personnel:** Jürgen Wassner

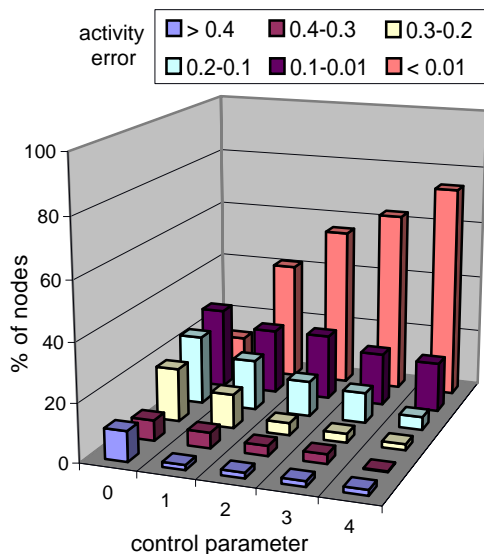
**Funding:** ETHZ, KTI-3650.1 DSP, Philips

**Partners:** Philips

Gate-level power optimization depends upon accurate switching activity information for each node in the logic network. As the circuit structure changes during the optimization process, node activities have to be recalculated. It seems plausible to use probabilistic techniques in this procedure. However, in the presence of complex signal correlations, probabilistic techniques require exponentially increasing computing power for exact activity calculation.

A new approximation method has been developed. As opposed to existing approaches the new method is able to approximate spatio-temporal correlation of input signals as well as correlation due to reconvergent fanout paths. The user can control the approximation of all types of correlations by means of a single parameter. The new method employs a polynomial representation for Boolean functions to achieve monotonously varying estimation accuracy with respect to the control parameter, which is essential for application in CAD tools. The polynomial form is instrumental because the significance of individual terms can be easily evaluated.

Since the worst-case computational complexity of the algorithm remains exponential, accuracy improvements must be attained for small values of the control parameter. This fact, as well as the monotonous behavior have been verified by simulation.



Activity error histograms versus control parameter for a 32-bit carry-look-ahead adder.

# Low-Power Digital Signal Processing of Speech Data

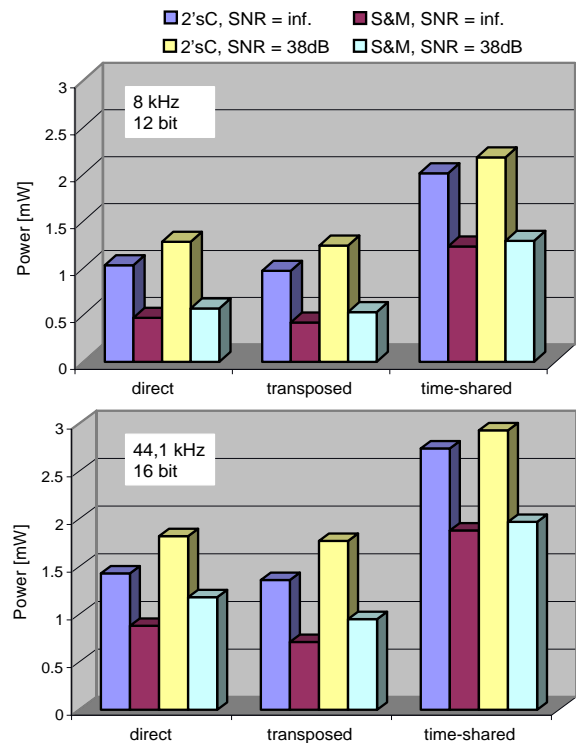
**Personnel:** Jürgen Wassner

**Funding:** ETHZ, KTI-3650.1 DSP, Philips

**Partners:** Philips

Two major statistical properties of speech signals affect average power consumption in applications like mobile phones or digital hearing aids: The high dynamic range asks for large word width if the signal is linearly quantized. In the long term, small absolute values are more likely than large values. This type of signal with frequent sign changes results in unreasonable bit toggling if 2's-complement representation is used. The sign-and-magnitude representation prevents this problem but requires more gates for the implementation of the extra addition.

Experiments with different FIR filter architectures have been conducted to quantify possible power savings. Input stimuli comprised male and female speech segments with a variety of noise shapes and levels. The results revealed a potential power reduction of up to 60% for low sample rates and isomorphic architectures, smaller relative savings for increasing sample rate, and insensitivity of average power with respect to noise forms.



Power consumption of 2's-complement vs. sign-and-magnitude FIR-filters for different noise levels, sample rates, word widths and filter architectures.

## Timing Correlation in Deep-Submicron Designs

**Personnel:** Matthias Brändli, Thomas Röwer, Hubert Kaeslin

**Funding:** Microswiss TR-EL-016

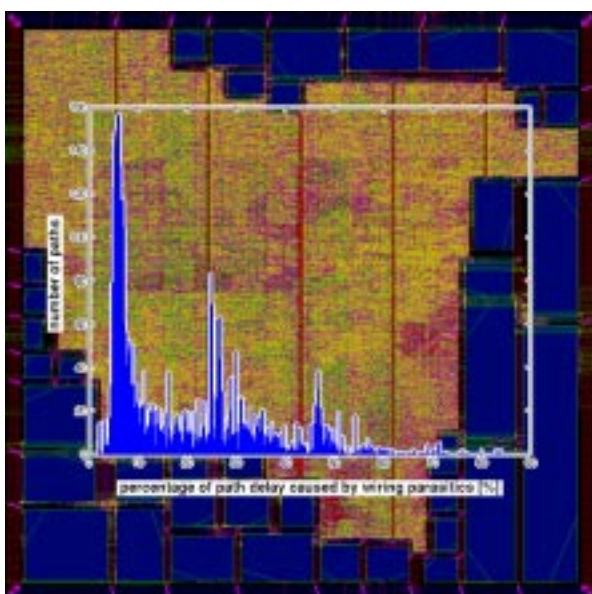
**Partners:** Infineon

The vehicle for the exploration of deep-submicron design methods was a synchronous SDH (Synchronous Digital Hierarchy) add-drop multiplexer with substantial complexity in order to expose the technical peculiarities of VLSI design in deep-submicron technologies. The original circuit is fabricated in a  $0.35\ \mu\text{m}$  sea-of-gates technology and has a circuit complexity of approximately 640 kGE logic and 360 kGE RAM. Our objective was to redesign this circuit as a cell-based full-custom IC in a deep-submicron technology ( $0.25\ \mu\text{m}$ , 3 LM, 2.5 V CMOS).

Notwithstanding many difficulties, the full design cycle from VHDL source code to a fully routed core has been completed (see background figure). The floor-plan illustrates that all the random logic has been placed and routed within a single standardcell area with no physical partitioning.

Depending on the net analyzed, the impact of wiring parasitics on propagation delay was found to make up between 2 and 83 % of the total delay figure, with an average of 18 % (see overlaid figure).

Although the wiring delay of  $0.5$  to  $0.25\ \mu\text{m}$  technologies becomes considerable the overall design flow is by no means to be revolutionized. It just becomes somewhat more complicated as a consequence of the required extra timing estimation and logic re-optimization steps.



Routed chip core and impact of wiring parasitics.

## Reconfigurable Control of IGBTs

**Personnel:** Jan Thalheim, Robert Reutemann

**Funding:** ETHZ, KTI-3367.1 SIGU

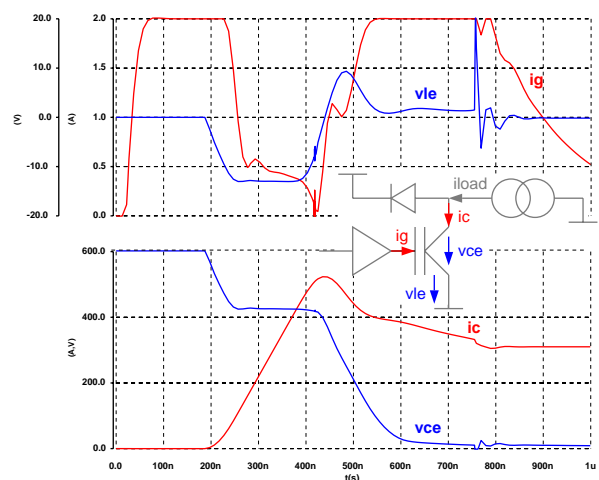
**Partners:** CONCEPT

In order to enhance system performance and robustness, a novel power system architecture based on Insulated Gate Bipolar Transistors (IGBTs) has been introduced. Objective of this project is to develop a hierarchical controller architecture which enables balancing and on-line reconfiguration of high-frequency systems utilizing parallel- and series-connected IGBT/diode modules.

To optimize the switching transients of IGBTs, nonlinear feedback control techniques are being investigated. Implementations for such local gate controllers are being studied, which are suitable for integration in a  $0.8\ \mu\text{m}$  standard CMOS process.

A driver is being developed which satisfies the gate current demand of IGBTs of the 1200 V/300 A to 3300 V/1200 A classes. To comply with the required gate current dynamics, a real-time reconfiguration is implemented in this gate drive.

A secondary control loop is required to manage global timing and parameter scheduling. To enable dynamic balancing of fast switching series-connected devices, a technique providing high timing resolution has been presented. A new approach for static balancing of parallel-connected semiconductors has been introduced. The latter methods can be applied not only to IGBTs, but to all types of power switches.



Gate current required for turn-on control of a 1200 V/300 A IGBT/diode module.